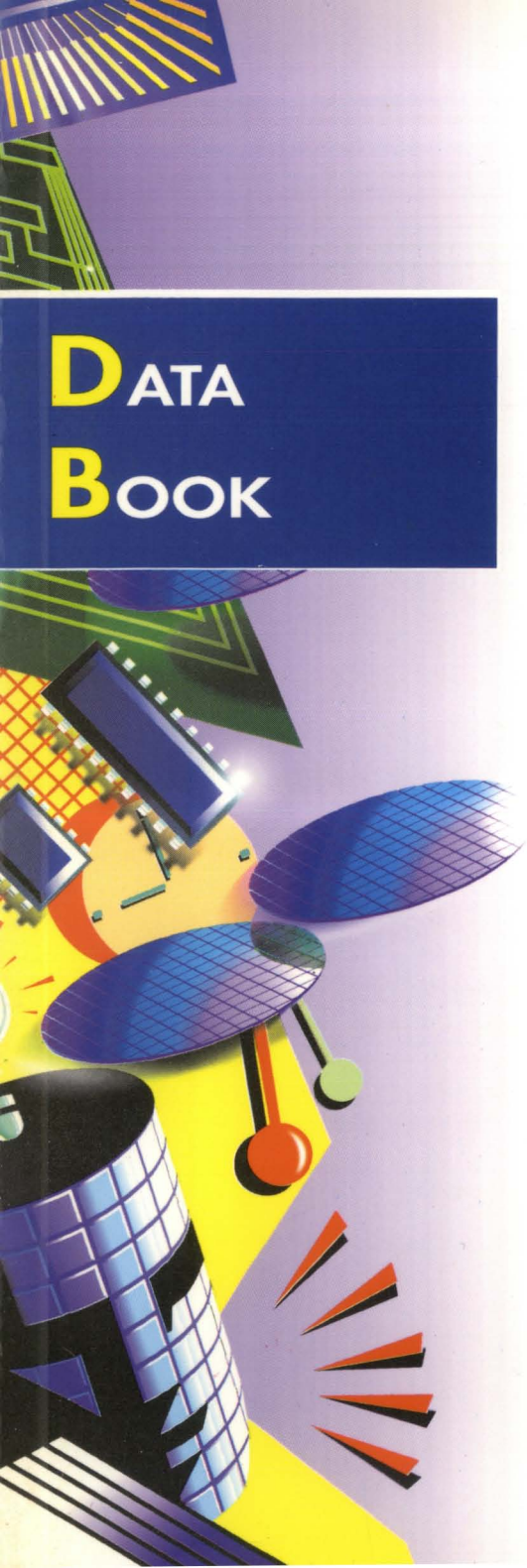
DATA BOOK

LINEAR MIXED-SIGNAL DESIGN SEMINAR '95



TEXAS INSTRUMENTS

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TEXAS INSTRUMENTS

LINEAR PRODUCTS
DOCUMENTATION QUICK REFERENCE GUIDE

TITLE	DOCUMENT No.
Operational Amplifiers & Comparators Volume A	SLYD011 1995
Operational Amplifiers & Comparators Volume B	SLYD012 1995
Linear Circuits Volume 2 Data Acquisition & Conversion	SLYD004A 1992
Linear Circuits Volume 3 Voltage Regulators & Supervisors	SLYD005A 1992
Linear Circuits Volume 4 Power+, Peripheral Drivers/Power Actuators, Display Drivers	SLYD010 1993
Data Transmission Circuits	SLLD001 1993

(As of April 1995)

1995
LINEAR MIXED-SIGNAL DESIGN SEMINAR

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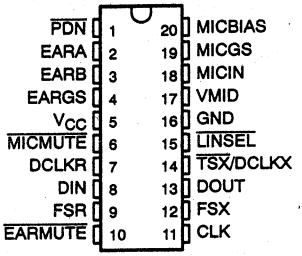
This Data supplement is intended as a companion to the 1995 Linear Mixed-Signal Design Seminar, therefore it only contains specifications for products covered in the seminar. In some instances, where there is a family of products, only one member of that family has been included. Full specifications for the entire linear product range are contained within the specific data manuals listed at the front of this supplement.

ALPHANUMERIC CONTENTS

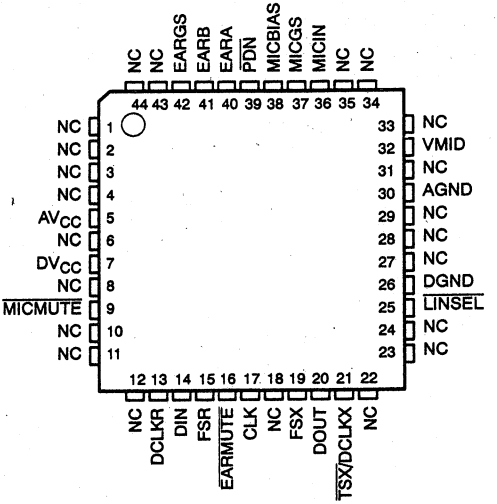
SLWS003 – D4031, MAY 1992 – REVISED MAY 1993

- **Single 5-V Operation**
- **Low Power Consumption:**
  Operating Mode . . . 40 mW Typ
  Standby Mode . . . 5 mW Typ
  Power-Down Mode . . . 1.25 mW Typ
- **Combined ADC, DAC, and Filters**
- **Extended Variable-Frequency Operation**
  Sample Rates up to 24 kHz
  Pass-Band up to 10 kHz
- **Electret Microphone Bias Reference Voltage Available**
- **Directly Drives a Piezo Speaker**
- **Compatible With All DSPs**
- **Selectable Between 8-Bit Companded and 13-Bit (Dynamic Range) Linear Conversion:**
  TCM320AC36 . . . μ-Law and Linear Modes
  TCM320AC37 . . . A-Law and Linear Modes
- **Programmable Volume Control in Linear Mode**
- **Designed for Standard 2.048-MHz Master Clock for U.S. Analog, U.S. Digital, CT2, DECT, GSM, and PCN Hand-Held Battery-Powered Telephones**

DW OR N PACKAGE
(TOP VIEW)



FR PACKAGE
(TOP VIEW)



NC – No internal connection

description

The voice-band audio processor (VBAP) circuits are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) together with transmit and receive filtering for voice-band communications systems. In particular, cellular telephone systems are targeted; however, this integrated circuit can function in several systems, including digital audio, telecommunications, and data acquisition.

The converted data is available in two formats. The formats are pin selectable between companded and linear. When the device is in the companded mode, data is transmitted and received in eight-bit words. When the linear mode is selected, 13 bits of data are sent and received, padded with zeros to provide a 16-bit word.

Caution. These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TEXAS INSTRUMENTS

description (continued)

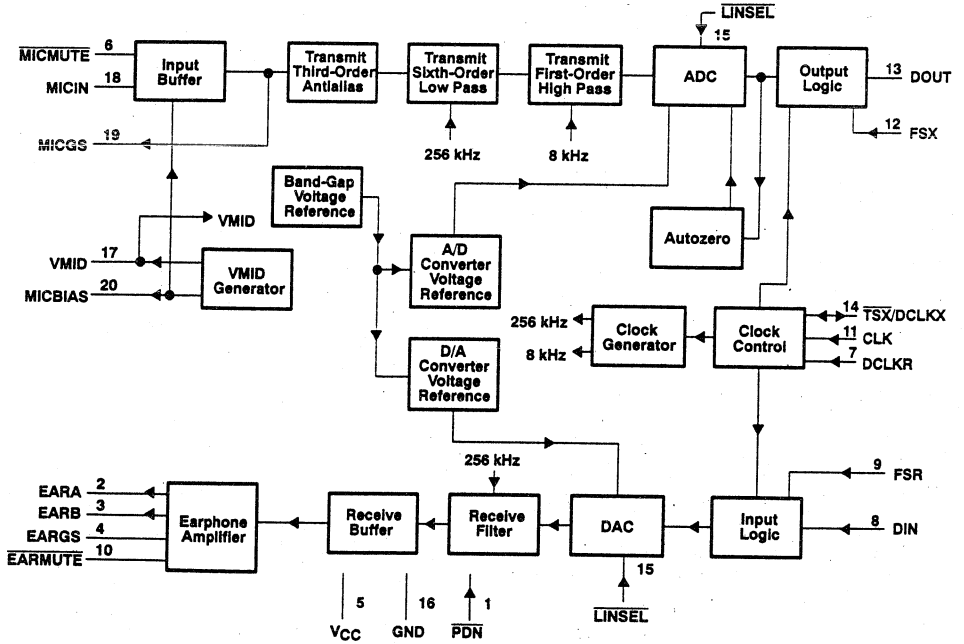
The transmit section is designed to directly interface with an electret microphone element. A reference voltage equal to $V_{CC}/2$, called VMID, is used to develop the midlevel virtual ground for all the amplifier circuits and the microphone bias circuit. A reference voltage called MICBIAS can be used to supply bias current for the microphone. The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through antialiasing and band-pass filters. The filtered signal is then input to a compressing analog-to-digital converter (COADC) if companded mode is selected; otherwise, the analog-to-digital converter performs a linear conversion.

The receive section takes a frame of serial data on DIN and converts it to analog through an expanding digital-to-analog converter (EXDAC) if the companded mode is selected; otherwise, a linear conversion is performed. The analog signal then passes through switched capacitor filters, which provide out-of-band rejection, (sin x)/x correction functions, and smoothing. The filtered signal is sent to the earphone amplifier. The earphone amplifier has a differential output with adjustable gain that is designed to minimize static power dissipation.

A single on-chip, high-precision band-gap circuit generates all voltage references, eliminating the need for external reference voltages.

The TCM320AC3_C devices are characterized for operation from 0°C to 70°C. The TCM320AC3_I devices are characterized from −40°C to 85°C.

functional block diagram



Pin numbers shown are for the DW and N packages.

Terminal Functions

PIN NAME	PIN NO. DW, N	PIN NO. FR	I/O	DESCRIPTION
AGND	—	30		Ground return for all internal analog circuits
AV_{CC}	—	5		5-V supply voltage for all internal analog circuits
CLK	11	17	I	In the fixed-data-rate mode, CLK is the master clock input as well as the transmit and receive data clock input. In the variable-data-rate mode, CLK serves only as the master clock input.
DCLKR	7	13	I	Selects fixed- or variable-data-rate operation. When DCLKR is connected to V_{CC}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{CC}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock.
DGND	—	26		Ground return for all internal digital circuits
DIN	8	14	I	Receive data input. Input data is clocked in on consecutive negative transitions of the receive data clock, which is CLK for a fixed data rate and DCLKR for a variable data rate.
DOUT	13	20	O	Transmit data output. Transmit data is clocked out on consecutive positive transitions of the transmit data clock, which is CLK for a fixed data rate and DCLKX for a variable data rate.
DV_{CC}	—	7		5-V supply voltage for all internal digital circuits
EARA	2	40	O	Earphone output. EARA forms a differential drive when used with the EARB signal.
EARB	3	41	O	Earphone output. EARB forms a differential drive when used with the EARA signal.
EARGS	4	42	I	Earphone gain set input of feedback signal for the earphone output. The ratio of an external potential divider network connected across EARA and EARB adjusts the power amplifier gain. Maximum gain occurs when EARGS is connected to EARB. Minimum gain occurs when EARGS is connected to EARA. Earphone frequency response correction is performed using an RC approach.
$\overline{\text{EARMUTE}}$	10	16	I	Earphone output mute control signal. When $\overline{\text{EARMUTE}}$ is low, the output amplifier is disabled and no audio is sent to the earphone.
FSR	9	15	I	Frame synchronization clock input for receive channel. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby state when FSR is TTL low for five frames or longer. The device enters a production test-mode condition when either FSR or FSX is held high for five frames or longer.
FSX	12	19	I	Frame synchronization clock input for transmit channel. FSX operates independently of, but in an analogous manner to, FSR. The transmit channel enters the standby state when FSX is low for five frames or longer. The device enters a production test-mode condition when either FSX or FSR is held high for five frames or longer.
GND	16	—		Ground return for all internal circuits
$\overline{\text{LINSEL}}$	15	25	I	Linear selection input. When low, $\overline{\text{LINSEL}}$ selects linear coding/decoding. When high, $\overline{\text{LINSEL}}$ selects companded coding/decoding. Companding code on the 'AC36 is μ-law, and companding code on the 'AC37 is A-law.
MICBIAS	20	38	O	Bias voltage equal to VMID for the electret microphone
MICGS	19	37	O	Output of the internal microphone amplifier. MICGS is used as the feedback to set the microphone amplifier gain. If sidetone is required, it is accomplished by connecting a series network between MICGS and EARGS.
MICIN	18	36	I	Electret microphone input to the internal microphone amplifier
$\overline{\text{MICMUTE}}$	6	9	I	Microphone input mute control signal. When $\overline{\text{MICMUTE}}$ is active (low), the input amplifier is disabled, the microphone current is switched off, and zero code is transmitted.
$\overline{\text{PDN}}$	1	39	I	Power-down input. When low, the device powers down to reduce power consumption.
$\overline{\text{TSX}}$/DCLKX	14	21	I/O	Transmit time slot strobe (active-low output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this is an open-drain output that pulls to ground and is used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock input.
V_{CC}	5	—		5-V supply voltage for all internal circuits
VMID	17	32	O	$V_{CC}/2$ bias voltage reference. An external, low-leakage, high-frequency 1-μF capacitor should be connected to VMID for filtering.

general information

system reliability features

The device should be powered up and initialized as follows:

1. GND is applied.
2. V_{CC} is applied.
3. All clocks are connected.
4. TTL high is applied to $\overline{PDN}$.
5. FSX and/or FSR synchronization pulses are applied.

Even though the VBAP is heavily protected against latch-up, it is still possible to cause it to latch-up under certain improper power conditions where excess current is forced into or out of one or more terminals. To ensure that latch-up does not occur, it is good design practice to put a reverse-biased Schottky diode between V_{CC} (power supply) and GND.

On the transmit channel, digital outputs DOUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 μs) after power up or application of V_{CC}. After this delay, DOUT, $\overline{TSX}$, and signaling are functional and occur in the proper time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. To further enhance system integrity, DOUT and $\overline{TSX}$ are placed in the high-impedance state after an interruption of CLK.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 1.25 mW.

The standby modes give the user the options of putting the entire device on standby, putting only the transmit channel on standby, or putting only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation, FSX is pulsed and FSR is held low. For receive-only operation, FSR is pulsed and FSX is held low. In the standby mode with both transmit and receive on standby, power consumption is reduced to 5 mW. See Table 1 for power-down and standby procedures.

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{PDN}$ = high, FSX = pulses, FSR = pulses	40 mW	Digital outputs active but not loaded
Power down	$\overline{PDN}$ = low, FSX/FSR = X/X	1.25 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Entire device on standby	FSX = low, FSR = low, $\overline{PDN}$ = high	5 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Only transmit on standby	FSX = low, FSR = pulses, $\overline{PDN}$ = high	20 mW	$\overline{TSX}$ and DOUT in the high-impedance state within five frames
Only receive on standby	FSR = low, FSX = pulses, $\overline{PDN}$ = high	20 mW	Digital outputs active but not loaded

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{CC}. It uses the master clock (CLK), frame synchronization clocks (FSX and FSR), and the $\overline{TSX}$ output. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR. A D/A conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter. The data word is eight bits long in the companded mode and sixteen bits long in the linear mode.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the receive data clock. In this mode, the master clock (CLK) controls the switched-capacitor filters, while data transfer into DIN and out of DOUT is controlled by DCLKR and DCLKX, respectively. This allows the data to be transferred into and out of the device at any rate up to the frequency of the master clock. DCLKR and DCLKX must be synchronous with CLK.

While the FSX input is high, data is transmitted from DOUT on consecutive positive transitions of DCLKX. Similarly, while the FSR input is high, the data word is received at DIN on consecutive negative transitions of DCLKR. The transmitted data word at DOUT is repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the data word to be transmitted more than once per frame, is available only with variable-data-rate timing.

asynchronous operations

In order to avoid crosstalk problems associated with special interrupt circuits, the design includes separate converters, filters, and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame.

precision voltage references

A precision band-gap reference voltage is generated internally and is used to supply all the references required for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This process ensures very accurate, stable gain performance over variations in supply voltage and device temperature.

conversion laws

The TCM320AC36 provides μ-law companding operation as specified by CCITT G.711 recommendation.

The TCM320AC37 provides A-law companding operation as specified by CCITT G.711 recommendation.

The linear mode of operation is the same for both the TCM320AC36 and the TCM320AC37. The linear mode utilizes a 13-bit 2s complement format.

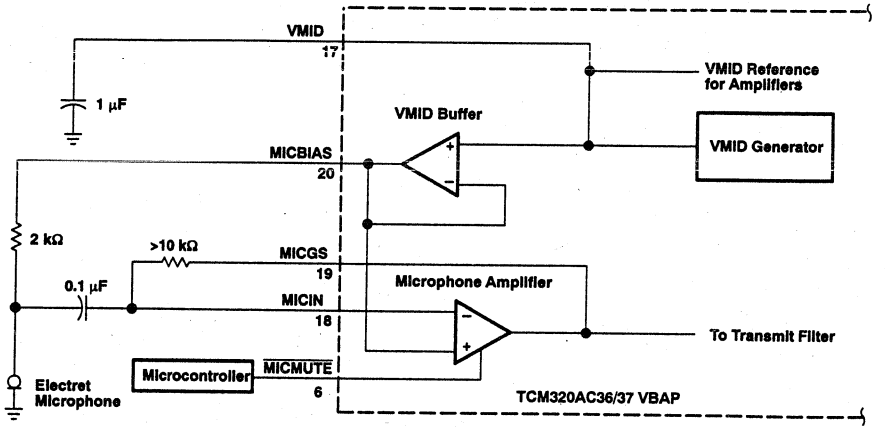
transmit operation

microphone input

The microphone input amplifier is specifically designed to interface to electret-type microphone elements as shown in Figure 1. The VMID buffer circuit provides a voltage (MICBIAS) equal to 1/2 V_{CC} as a reference for the microphone amplifier and a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network to the amplifier inverting input (MICIN) to set the amplifier gain. VMID is brought out to provide a place to filter the VMID voltage.

microphone mute function

The $\overline{\text{MICMUTE}}$ input disables the microphone amplifier and attenuates the signal on the MICGS output to a level that is 80 dB or more down from the signal on the MICIN input. $\overline{\text{MICMUTE}}$ also causes the digital circuitry to transmit all zero code on DOUT.



Pin numbers shown are for the DW and N packages.

Figure 1. Typical Microphone Interface

transmit filter

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first eight or 16 data clock cycles of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder.

data word structure

The data word is eight bits long in the companded mode. All eight bits represent one audio data sample. The sign bit is the first bit transmitted.

The data word is 16 bits long in the linear mode. The first 13 bits comprise the audio data sample, and the last three bits are volume control in the receive direction (DIN) and zeros in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

In the companded mode, the serial data word is received at DIN on the first eight clock cycles in fixed-data rate and on the last eight clock cycles in variable-data rate. The serial data word is received at DIN on the first 13 clock cycles in the linear mode. Digital-to-analog conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive buffer

The receive buffer contains the volume control.

earphone amplifier

The earphone amplifier has a balanced output to allow maximum flexibility in output configuration. The output amplifier is designed to directly drive a piezo earphone in the differential configuration without any additional external components. The output can also be used to drive a single-ended load with the output signal voltage centered around $V_{CC}/2$.

The receive-channel output level can be adjusted between specified limits by connecting an external resistor network to EARGS.

receive data format

Eight bits of data are received in the companded mode and are valid. The sign bit is the first bit received (see Table 2).

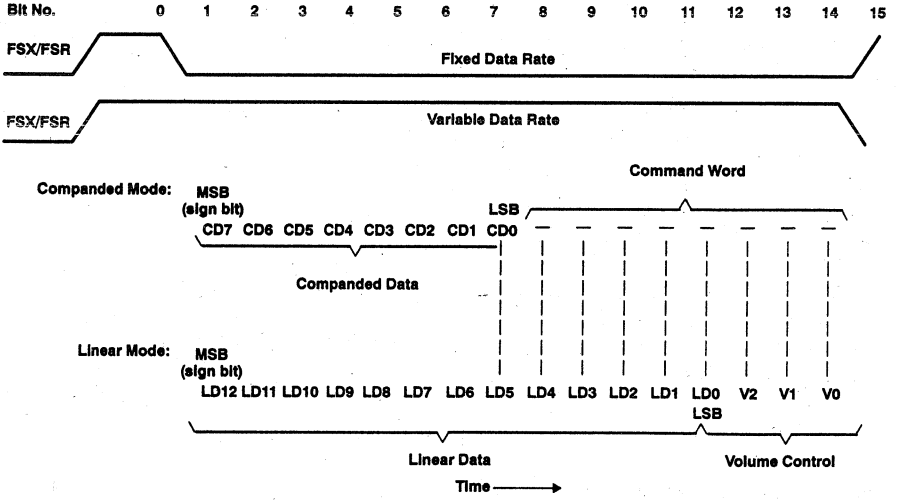
Sixteen bits of data are received in the linear mode. The first 13 bits are the D/A code, and the remaining three bits form the volume control word (see Table 2). The volume control function is actually an attenuation control where the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps, giving a maximum attenuation of 21 dB when all bits are 1s. The volume control bits are not latched into the VBAP and must be present in each received data word.

Table 2. Receive Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
0	CD7	LD12
1	CD6	LD11
2	CD5	LD10
3	CD4	LD9
4	CD3	LD8
5	CD2	LD7
6	CD1	LD6
7	CD0	LD5
8	–	LD4
9	–	LD3
A	–	LD2
B	–	LD1
C	–	LD0
D	–	V2
E	–	V1
F	–	V0

relationship between data word and frame sync

Volume control and other control bits always follow the PCM data in time:



where:

CD7–CD0 = Data word when in companded mode
— = Unused bits in companded mode
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 3 dBm0
111 = minimum volume, –18 dBm0
LD12–LD0 = Data word when in linear mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Output voltage range at DOUT, V_O ..... −0.3 V to 7 V
Input voltage range at DIN, V_I ..... −0.3 V to 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: C-suffix ..... 0°C to 70°C
I-suffix ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage value is with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
FR	1075 mW	7.1 mW/°C	756 mW	649 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)		4.5	5.5	V
High-level input voltage, V_{IH}		2.2		V
Low-level input voltage, V_{IL}			0.8	V
Load resistance between EARA and EARB, R_L (see Note 4)		600		Ω
Load capacitance between EARA and EARB, C_L (see Note 4)			113	nF
Operating free-air temperature, T_A	TCM320AC36C, TCM320AC37C	0	70	°C
	TCM320AC36I, TCM320AC37I	−40	85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the following sequence should be followed when applying power:
1. Connect to GND.
2. Connect V_{CC}.
3. Connect the input signals.

When removing power, follow the preceding steps in reverse order.

3. Voltages at analog inputs and outputs and V_{CC} are with respect to GND.
4. R_L and C_L should not be applied simultaneously.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

supply current, f_{DCLKR} or f_{DCLKX} = 2.048 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating	$\overline{PDN}$ is high with CLK signal present		9.2	mA
		Power down	$\overline{PDN}$ is low for 500 µs		0.8	
		Standby – both	$\overline{PDN}$ is high with FSX and FSR missing for 500 µs		1.8	
		Standby – one	$\overline{PDN}$ is high with FSX and FSR missing for 500 µs		6	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	I_{OH} = −3.2 mA, V_{CC} = 5 V	2.4	4.6		V
V_{OL}	Low-level output voltage		I_{OL} = 3.2 mA, V_{CC} = 5 V		0.2	0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	μA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	μA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

microphone interface‡

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage at MICIN		V_I = 0 to 5 V			±5	mV
I_{IB}	Input bias current at MICIN					±200	nA
B_1	Unity-gain bandwidth, open loop at MICIN				1		MHz
C_i	Input capacitance at MICIN					5	pF
A_V	Large-signal voltage amplification at MICGS					10000	V/V
	Output level at MICGS with $\overline{\text{MICMUTE}}$ active		V_I = 4 V			−80	dBm0
$I_{O(max)}$	Maximum output current	VMID		1			μA
		MICBIAS		1			mA

speaker interface‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	Peak-to-peak ac output voltage				3	V_{PP}
V_{OO}	Output offset voltage at EARA, EARB (single-ended)	Relative to GND			80	mV
I_{IL}	Input leakage current at EARGS	V_I = 0 to 5 V			±200	nA
$I_{O(max)}$	Maximum output current	R_L = 600 Ω			±5	mA
r_o	Output resistance at EARA, EARB			1		Ω
A_V	Large-signal voltage amplification			4		V/V
	Gain change	$\overline{\text{EARMUTE}}$ low, max level when muted	−80			dB

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ All parameters are measured between MICIN and GND (unless otherwise noted).

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

transmit gain and dynamic range, companded or linear mode, μ-law or A-law, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted) (see Notes 5 and 6)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit reference-signal level (0 dB) (see Note 7)	Companded mode selected, μ-law ('AC36)		0.982	Vrms
	Companded mode selected, A-law ('AC37)		0.985	
	Linear mode selected ('AC36 and 'AC37)		1.001	
Overload-signal level	Companded mode selected, μ-law ('AC36)		4	V_{PP}
	Companded mode selected, A-law ('AC37)		4	
	Linear mode selected ('AC36 and 'AC37)		4	
Absolute gain error	0-dB input signal		±1	dB
Gain error with input level relative to gain at −10 dB	MICIN to DOUT at 3 dBm0 to −40 dBm0		±0.5	dB
	MICIN to DOUT at −41 dBm0 to −50 dBm0		±0.8	
	MICIN to DOUT at −51 dBm0 to −55 dBm0		±1.5	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

transmit filter transfer, linear mode selected, μ-law or A-law, over recommended ranges of supply voltage and free-air temperature, CLK = 2.048 MHz, FSX = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output signal at MICIN is 0 dB	Input signal = 50 Hz	−10	0	dB
		Input signal = 200 Hz	−1.8	0	
		Input signal = 300 Hz to 3 kHz		±0.15	
		Input signal = 3.3 kHz	−0.35	0.03	
		Input signal = 3.4 kHz	−1	−0.1	
		Input signal = 4 kHz		−14	
		Input signal ≥4.6 kHz		−32	

transmit idle channel noise and distortion, companded mode, μ-law or A-law, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, psophometrically weighted	MICIN connected to MICGS through a 10-kΩ resistor		−71	dBm0p
Transmit noise, C-message weighted	MICIN connected to MICGS through a 10-kΩ resistor		10	dBrnC0
Transmit signal-to-distortion ratio with sine-wave input MICIN to DOUT	MICIN to DOUT at 0 dBm0 to −30 dBm0	36		dB
	MICIN to DOUT at −31 dBm0 to −40 dBm0	30		
	MICIN to DOUT at −41 dBm0 to −45 dBm0	20		
Intermodulation distortion, 2-tone CCITT method, composite power level −13 dBm0	CCITT G.712 (7.1), R2	49		dB
	CCITT G.712 (7.2), R3	51		

NOTES: 5. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
6. The input amplifier is set for inverting unity gain.
7. The reference-signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 2 V.
8. Transmit noise, linear mode: 200 μVrms is equivalent to −74 dB (referenced to device 0-dB level).

transmit idle channel noise and distortion, linear mode, over recommended ranges of supply voltage and operating free-air temperature (see Notes 6 and 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 10-kΩ resistor	200		μVrms
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –6 dBm0	54		dB
	MICIN to DOUT at –7 dBm0 to –12 dBm0	48		
	MICIN to DOUT at –13 dBm0 to –18 dBm0	42		
	MICIN to DOUT at –19 dBm0 to –24 dBm0	35		
	MICIN to DOUT at –25 dBm0 to –45 dBm0	20		

receive gain and dynamic range, companded or linear mode, μ-law or A-law, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive reference-signal level (0 dB) (see Note 11)	Companded mode selected, μ-law ('AC36)		0.736	Vrms
	Companded mode selected, A-law ('AC37)		0.739	
	Linear mode selected ('AC36 and 'AC37)		0.751	
Overload-signal level	Companded mode selected, μ-law ('AC36)		3	V_{PP}
	Companded mode selected, A-law ('AC37)		3	
	Linear mode selected ('AC36 and 'AC37)		3	
Absolute gain error	0-dB input signal		±1	dB
Gain error with output level relative to gain at –10 dBm0	DIN to EARA and EARB at 3 dBm0 to –40 dBm0		±0.5	dB
	DIN to EARA and EARB at –41 dBm0 to –50 dBm0		±0.8	
	DIN to EARA and EARB at –51 dBm0 to –55 dBm0		±01.2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature, FSR = 8 kHz (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at DIN is 0 dBm0	< 200 Hz		0.15	dB
		200 Hz	–0.5	0.15	
		300 Hz to 3 kHz		±0.15	
		3.3 kHz	–0.35	0.03	
		3.4 kHz	–1	–0.18	
		4 kHz		–14	
		> 4.6 kHz		–30	

receive idle channel noise and distortion, companded mode, μ-law or A-law, over recommended ranges of supply voltage and operating free-air temperature (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise, psophometrically weighted	DIN = 11010101 (A-law)		–75	dBm0p
Receive noise, C-message weighted	DIN = 11111111 (μ-law)		5	dBrnc0
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –30 dBm0	36		dB
	DIN to EARA and EARB at –31 dBm0 to –40 dBm0	30		
	DIN to EARA and EARB at –41 dBm0 to –45 dBm0	25		

NOTES: 6. The input amplifier is set for inverting unity gain.
8. Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).
9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
10. Unless otherwise noted, the digital input is a word stream generated by passing a 0-dB sine wave at 1020 Hz through an ideal encoder where 0 dB is defined as the zero reference.
11. This reference-signal level is measured at the speaker output of the receive channel with the gain of the output speaker amplifier set to unity.

receive idle channel noise and distortion, linear mode, over recommended ranges of supply voltage and operating free-air temperature (see Notes 9 and 12)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise	DIN = 00000000		200	μV
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –6 dBm0	52		dB
	DIN to EARA and EARB at –6 dBm0 to –12 dBm0	48		
	DIN to EARA and EARB at –13 dBm0 to –18 dBm0	42		
	DIN to EARA and EARB at –19 dBm0 to –24 dBm0	35		
	DIN to EARA and EARB at –25 dBm0 to –45 dBm0	20		
Intermodulation, 2-tone CCITT distortion method, composite power level –13 dBm0	CCITT G.712 (7.1), R2	50		dB
	CCITT G.712 (7.2), R3	54		

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
12. Receive noise, linear mode: 200 μVrms is equivalent to –71 dB (referenced to device 0-dB level).

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply voltage rejection ratio, transmit channel	Idle channel, supply signal = 100 mVrms, f = 0 to 30 kHz (measured at DOUT)		–30		dB
Supply voltage rejection ratio, receive channel	Idle channel, supply signal = 100 mVrms, EARGS connected to EARB, f = 0 to 30 kHz (measured differentially between EARA and EARB)		–30		dB
Crosstalk attenuation, transmit-to-receive (differential)	MICIN = 0 dB, f = 1.02 kHz, unity transmit gain, EARGS connected to EARB, measured differentially between EARA and EARB	68			dB
Crosstalk attenuation, receive-to-transmit	DIN = 0 dBm0, f = 1.02 kHz, unity transmit gain, measured at DOUT	68			dB

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 2, 3, 4, and 5)

		MIN	TYP†	MAX	UNIT
t_t	Transition time, CLK and DCLK			10	ns
	Duty cycle, CLK	45%	50%	55%	
	Duty cycle, DCLK	45%	50%	55%	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

transmit timing requirement over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX	20	468	ns
$t_{h(FSX)}$	Hold time, FSX	20	468	ns

receive timing requirement over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 2)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR	20	468	ns
$t_{h(FSR)}$	Hold time, FSR	20	468	ns
$t_{su(DIN)}$	Setup time, DIN	20		ns
$t_{h(DIN)}$	Hold time, DIN	20		ns

transmit timing requirement over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 5)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX	40	$t_{c(DCLKX)}-40$	ns
$t_{h(FSX)}$	Hold time, FSX	35	$t_{c(DCLKX)}-35$	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR	40		ns
$t_{h(FSR)}$	Hold time, FSR	35	$t_{c(DCLKR)}-35$	ns
$t_{su(DIN)}$	Setup time, DIN	30		ns
$t_{h(DIN)}$	Hold time, DIN	30		ns

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode, C_L = 0 to 10 pF, (see Figures 2 and 3)

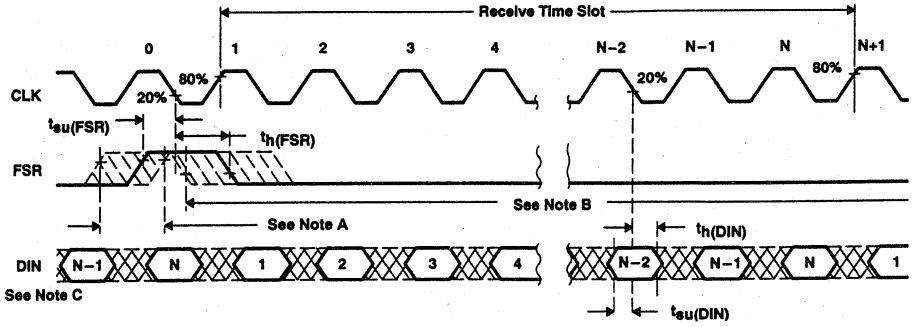
		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From CLK bit 1 high to DOUT bit 1 valid			35	ns
t_{pd2}	From CLK high to DOUT valid, bits 2 to n			35	ns
t_{pd3}	From CLK bit n low to DOUT bit n Hi-Z		30		ns
t_{pd4}	From CLK bit 1 high to $\overline{TSX}$ active (low)	R_{pullup} = 1.24 kΩ		40	ns
t_{pd5}	From CLK bit n low to FSX inactive (high)	R_{pullup} = 1.24 kΩ	30		ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Figures 4 and 5)

		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	FSX high to DOUT bit 1 valid	C_L = 0 to 10 pF		30	ns
t_{pd7}	DCLKX high to DOUT valid, bits 2 to n	C_L = 0 to 10 pF		40	ns
t_{pd8}	FSX low to DOUT bit n HI-Z		20		ns

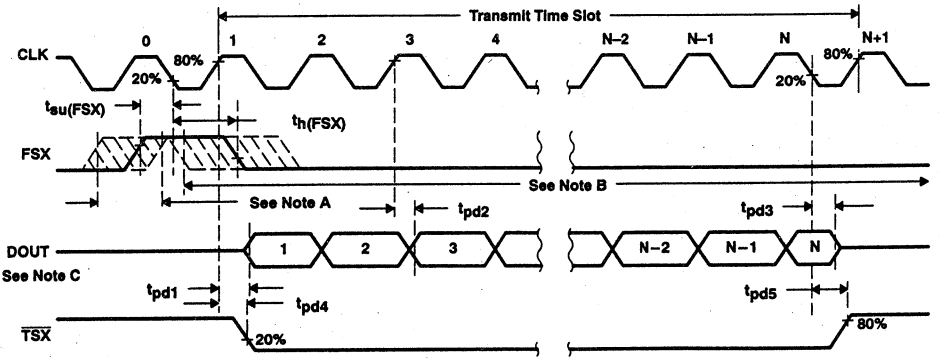
PARAMETER MEASUREMENT INFORMATION

All timing parameters are referenced to V_{IH} and V_{IL}. Bit 1 = MSB (most significant bit) and is clocked in first on DIN or clocked out first on DOUT. Bit n = LSB (least significant bit) and is clocked in last on DIN or is clocked out last on DOUT. N = 8 for the companded mode, and N = 16 for the linear mode.



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

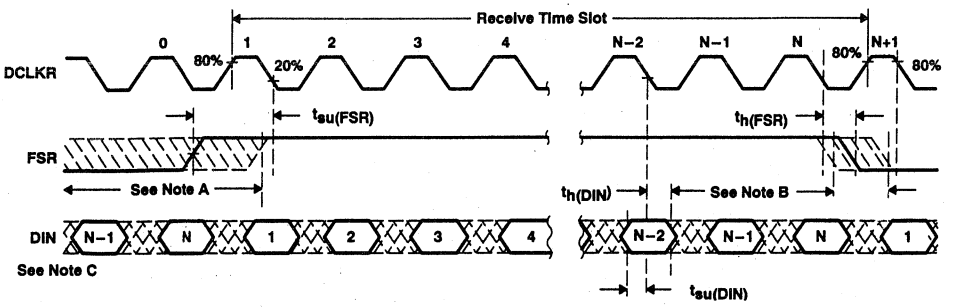
Figure 2. Fixed-Data-Rate, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low ($t_{h(FSX)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.

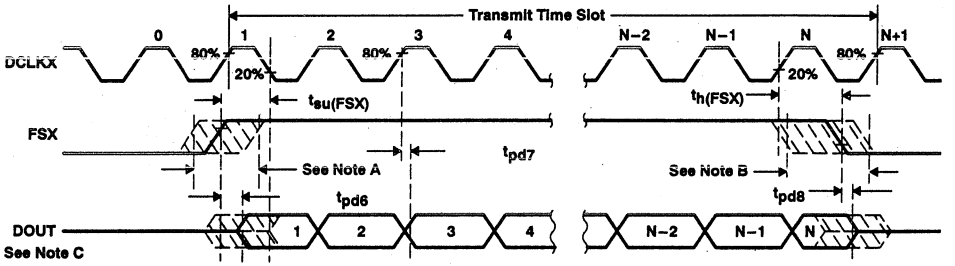
Figure 3. Fixed-Data-Rate, Transmit Side Timing Diagram

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for FSR high ($t_{su(FSR)}$ max determined by data collision considerations).
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 4. Variable-Data-Rate, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low without data repetition.
C. Transitions are measured at 50%.

Figure 5. Variable-Data-Rate, Transmit Side Timing Diagram

APPLICATION INFORMATION

output gain set design considerations (see Figure 6)

EARA and EARB are low-impedance complementary outputs. The voltages at the nodes are:
V_{O+} at EARA
V_{O-} at EARB
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to EARGS.

A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

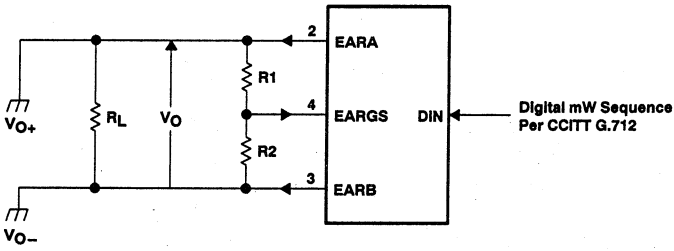
The parallel combination R1 + R2 and R_L sets the total loading. The total capacitance at EARGS and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital mW output response (V_A = 0.751 Vrms).

V_A represents the maximum available digital mW output response (V_A = 0.751 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$



Pin numbers shown are for the DW and N packages.

Figure 6. Gain-Setting Configuration

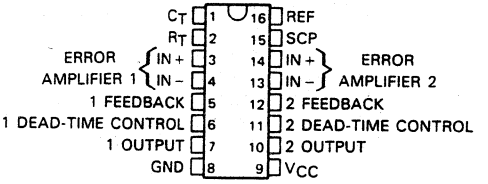
higher clock frequencies and sample rates

The VBAP is designed to work with sample rates up to 24 kHz where the frequency of the frame sync determines the sampling frequency. However, there is a fundamental requirement to maintain the ratio of master clock frequency, f_{CLK}, to frame sync frequency, f_{FSR}/f_{FSX}. This ratio for the VBAP is 2.048 MHz/8 kHz, or 256 master clocks per frame sync. For example, to operate the VBAP at a sampling rate of f_{FSR} and f_{FSX} equal to 16 kHz, f_{CLK} must be 256 times 16 kHz, or 4.096 MHz. If the VBAP is operated above an 8-kHz sample rate, however, it is expected that the performance will be somewhat degraded. Exact parametric specifications for rates up to 24-kHz sample rate are not specified at this time.

D2730, FEBRUARY 1983 – REVISED OCTOBER 1988

- **Complete PWM Power Control Circuitry**
- **Completely Synchronized Operation**
- **Internal Undervoltage Lockout Protection**
- **Wide Supply Voltage Range**
- **Internal Short-Circuit Protection**
- **Oscillator Frequency . . . 500 kHz Max**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 2.5-V Reference Supply**

D OR N PACKAGE
(TOP VIEW)



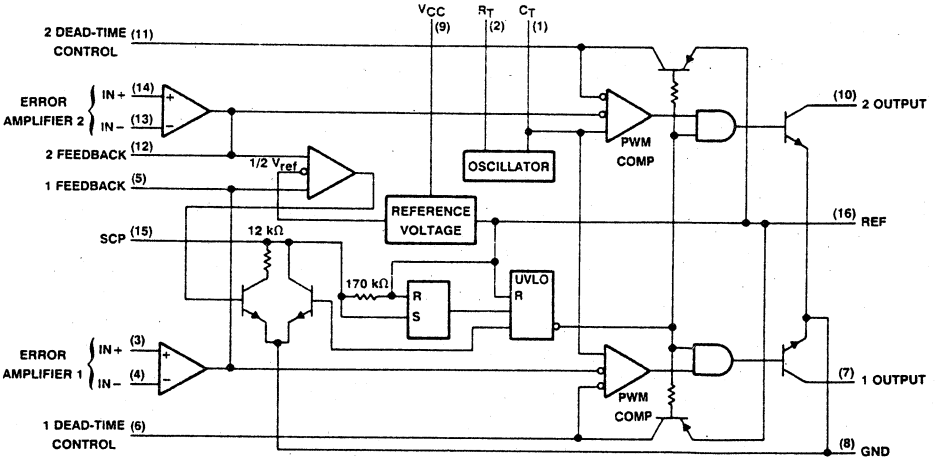
description

The TL1451AC incorporates on a single monolithic chip all the functions required in the construction of two pulse-width-modulation control circuits. Designed primarily for power supply control, the TL1451AC contains an on-chip 2.5-V regulator, two error amplifiers, an adjustable oscillator, two dead-time comparators, undervoltage lockout circuitry, and dual common-emitter output transistor circuits.

The uncommitted output transistors provide common-emitter output capability for each controller. The internal amplifiers exhibit a common-mode voltage range from 1.04 V to 1.45 V. The dead-time control comparator has no offset unless externally altered and may be used to provide 0% to 100% dead time. The on-chip oscillator may be operated by terminating R_T (pin 2) and C_T (pin 1). During low V_{CC} conditions, the undervoltage lockout control circuit feature locks the outputs off until the internal circuitry is operational.

The TL1451AC is characterized for operation from −20°C to 85°C.

functional block diagram



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 41 V
Amplifier input voltage . . . . . 20 V
Collector output voltage . . . . . 51 V
Collector output current . . . . . 21 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . −20°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	500 mW	4.0 mW/°C	320 mW	260 mW
N	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	3.6	40	V
Amplifier input voltage, V_I	1.05	1.45	V
Collector output voltage, V_O		50	V
Collector output current		20	mA
Current into feedback terminal		45	μA
Feedback resistor, R_F	100		kΩ
Timing capacitor, C_T	150	15000	pF
Timing resistor, R_T	5.1	100	kΩ
Oscillator frequency	1	500	kHz
Operating free-air temperature, T_A	−20	85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage (pin 16)	I_O = 1 mA	2.4	2.5	2.6	V
Output voltage change with temperature	T_A = −20°C to 25°C		−0.1%	±1%	
	T_A = 25°C to 85°C		−0.2%	±1%	
Input regulation	V_{CC} = 3.6 V to 40 V		2	12.5	mV
Output regulation	I_O = 0.1 mA to 1 mA		1	7.5	mV
Short-circuit output current	V_O = 0	3	10	30	mV

undervoltage lockout section

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Upper threshold voltage (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C		2.72		V
Lower threshold voltage (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C		2.6		V
Hysteresis (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C	80	120		mV
Reset threshold voltage (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C	1.5	1.8		V

† All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted) (continued)

protection control section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (pin 15)	T_A = 25°C	0.65	0.7	0.75	V
Standby voltage (pin 15)	No pullup	140	185	230	mV
Latched input voltage (pin 15)	No pullup		60	120	mV
Input (source) current	V_I = 0.7 V, T_A = 25°C	−10	−15	−20	µA
Comparator threshold voltage (pins 5 and 12)			1.18		V

oscillator section

PARAMETER	TEST CONDITIONS‡	MIN	TYP†	MAX	UNIT
Frequency	C_T = 330 pF, R_T = 10 kΩ		200		kHz
Standard deviation of frequency	C_T = 330 pF, R_T = 10 kΩ		10%		
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1%		
Frequency change with temperature	T_A = −20°C to 25°C		−0.4%	±2%	
	T_A = 25°C to 85°C		−0.2%	±2%	

dead-time control section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input bias current (pins 6 and 11)				1	µA
Latch mode (source) current (pins 6 and 11)	T_A = 25°C	−80	−145		µA
Latched input voltage (pins 6 and 11)	I_O = 40 µA	2.3			V
Input threshold voltage at f = 10 kHz (pins 6 and 11)	Zero duty cycle		2.05	2.25	V
	Maximum duty cycle	1.2	1.45		

error-amplifier section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input offset voltage	V_O (pins 5 and 12) = 1.25 V			±6	mV
Input offset current	V_O (pins 5 and 12) = 1.25 V			±100	nA
Input bias current	V_O (pins 5 and 12) = 1.25 V		160	500	nA
Common-mode input voltage range	V_{CC} = 3.6 V to 40 V	1.05 to 1.45			V
Open-loop voltage amplification	R_F = 200 kΩ	70	80		dB
Unity-gain bandwidth			1.5		MHz
Common-mode rejection ratio		60	80		dB
Positive output voltage swing		V_{ref}−0.1			V
Negative output voltage swing				1	V
Output (sink) current (pins 5 and 12)	V_{ID} = −0.1 V, V_O = 1.25 V	0.5	1.6		mA
Output (source) current (pins 5 and 12)	V_{ID} = 0.1 V, V_O = 1.25 V	−45	−70		µA

† All typical values are at T_A = 25°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted) (continued)

output section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Collector off-state current	V_O = 50 V			10	μA
Output saturation voltage	I_O = 10 mA		1.2	2	V
Short-circuit output current	V_O = 6 V		90		mA

pwm comparator section

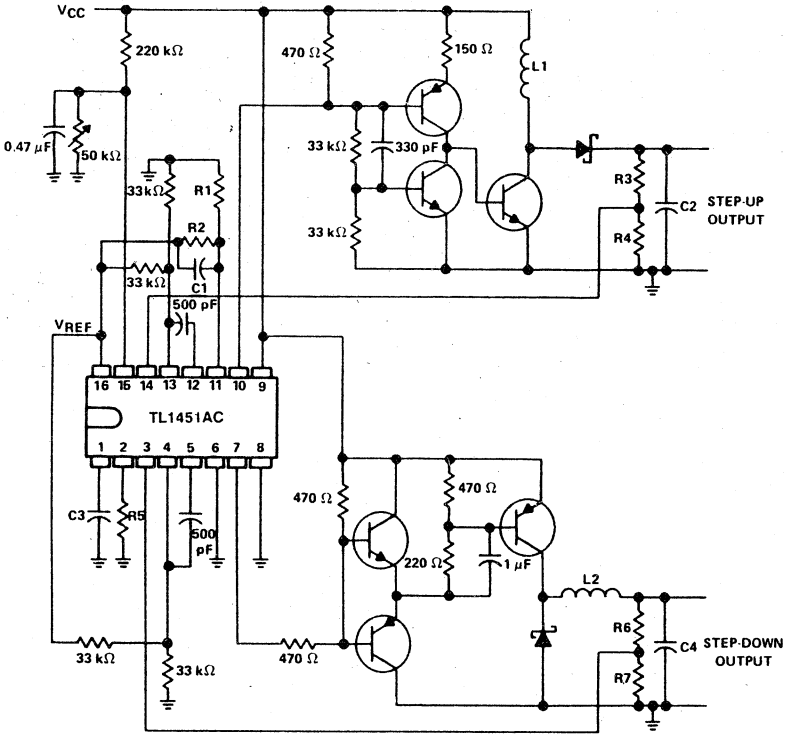
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage	Zero duty cycle		2.05	2.25	V
at f = 10 kHz (pins 5 and 12)	Maximum duty cycle	1.2	1.45		
Input (sink) current (pins 5 and 12)	V_I = 1.25 V	0.5	1.6		mA
Input (source) current (pins 5 and 12)	V_I = 1.25 V	−45	−70		μA

total device

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Standby supply current	Off-state		1.3	1.8	mA
Average supply current	R_T = 10 kΩ		1.7	2.4	mA

† All typical values are at T_A = 25°C.

TYPICAL APPLICATION DATA

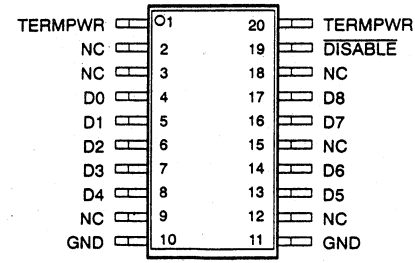


Values for R1 through R7, C1 through C4, and L1 and L2 depend upon inidividual application.

available features

- Fully Integrated 9-Channel SCSI Termination
- No External Components Required
- Maximum Allowed Current Applied at First High-Level Step
- 6-pF Typical Power-Down Output Capacitance
- Wide V_{term}† (Termination Voltage) Operating Range, 3.5 V to 5.5 V
- TTL-Compatible Disable Feature
- Compatible With Active Negation
- Thermal Regulation

PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL2218-285 is a current-mode 9-channel monolithic terminator specially designed for single-ended small-computer-systems-interface (SCSI) bus termination. A user-controlled disable function is provided to reduce standby power. No impedance-matching resistors or other external components are required for its operation as a complete terminator.

The device operates over a wide termination-voltage (V_{term}†) range of 3.5 V to 5.5 V, offering an extra 0.5 V of operating range when compared to the minimum termination voltage of 4 V required by other integrated active terminators. The TL2218-285 functions as a current-sourcing terminator and supplies a constant output current of 23 mA into each asserted line. When a line is deasserted, the device senses the rising voltage level and begins to function as a voltage source, supplying a fixed output voltage of 2.85 V. The TL2218-285 features compatibility with active negation drivers and has a typical sink current capability of 20 mA.

The TL2218-285 is able to ensure that maximum current is applied at the first high-level step. This performance means that the device should provide a first high-level step exceeding 2 V even at a 10-MHz rate. Therefore, noise margins are improved considerably above those provided by resistive terminators.

A key difference between the TL2218-285 current-mode terminator and a Boulay terminator is that this device does not incorporate a low dropout regulator to set the output voltage to 2.85 V. In contrast with the Boulay termination concept, the accuracy of the 2.85 V is not critical with the current-mode method used by the TL2218-285 because this voltage does not determine the driver current. Therefore, the primary device specifications are not the same as with a voltage regulator but are more concerned with output current.

The $\overline{\text{DISABLE}}$ terminal is TTL compatible and must be taken low to shut down the outputs. The device is normally active, even if $\overline{\text{DISABLE}}$ is left floating. In the disable mode, only the device startup circuits remain active, thereby reducing the supply current to just 500 μA. Output capacitance in the shutdown mode is typically 6 pF.

The TL2218-285 has on-board thermal regulation and current limiting, eliminating the need for external protection circuitry. A thermal regulation circuit that is designed to provide limiting, rather than an actual thermal shutdown, is included in the individual channels of the TL2218-285. If a system fault occurs that leads to excessive power dissipation by the terminator, the thermal regulation circuit causes a reduction in the asserted-line output current sufficient to maintain operation. This feature allows the bus to remain active during a fault condition, which permits data transfer immediately upon removal of the fault. A terminator with thermal shutdown does not allow for data transfer until sufficient cooling has occurred. Another advantage offered by the TL2218-285 is a design that does not require costly laser trimming in the manufacturing process.

The TL2218-285 is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

† This symbol is not presently listed within EIA/JEDEC standards for letter symbols.

AVAILABLE OPTIONS

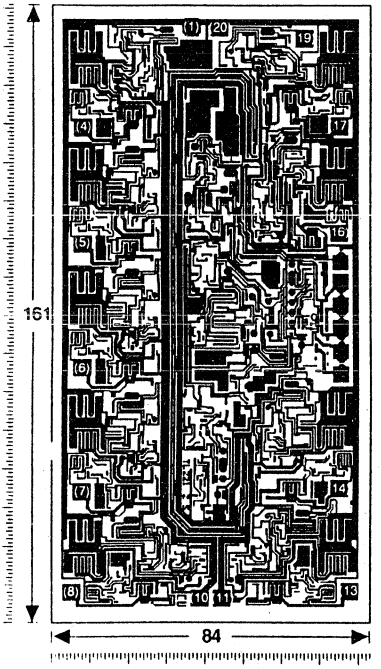
T_J	SURFACE MOUNT (PW)†	CHIP FORM (Y)
0°C to 125°C	TL2218-285PWLE	TL2218-285Y

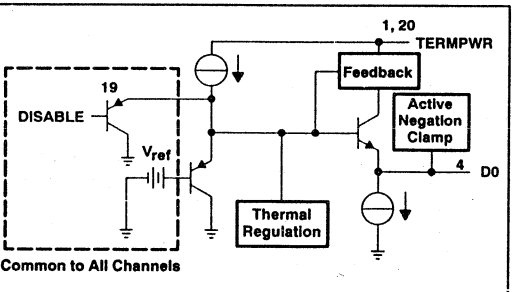
† The PW package is only available left-end taped and reeled.

TL2218-285Y chip information

This chip, when properly assembled, displays characteristics similar to the TL2218-285. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 TYPICAL

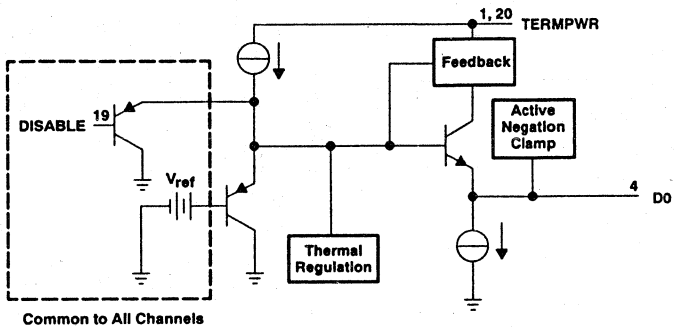
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

functional block diagram (each channel)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Figures 1, 2, and 3)†

Continuous termination voltage	10 V
Continuous output voltage range	0 V to 5.5 V
Continuous disable voltage range	0 V to 5.5 V
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range	−55°C to 150°C
Storage temperature range	−60°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
PW	T_A	828 mW	6.62 mW/°C	530 mW	430 mW	165 mW
	T_C	4032 mW	32.2 mW/°C	2580 mW	2086 mW	806 mW
	T_L‡	2475 mW	19.8 mW/°C	1584 mW	1287 mW	495 mW

‡ $R_{\theta JL}$ is the thermal resistance between the junction and device lead. To determine the virtual junction temperature (T_J) relative to the device lead temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JL} + T_L$, where P_D is the internal power dissipation of the device and T_L is the device lead temperature at the point of contact to the printed wiring board. $R_{\theta JL}$ is 50.5°C/W.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

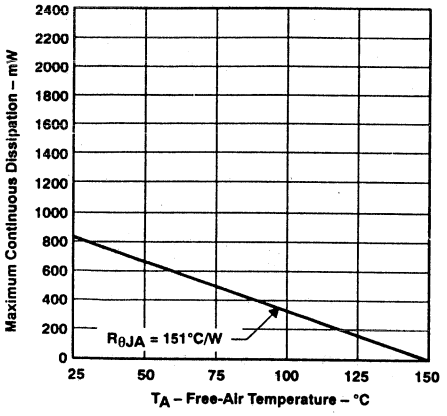


Figure 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

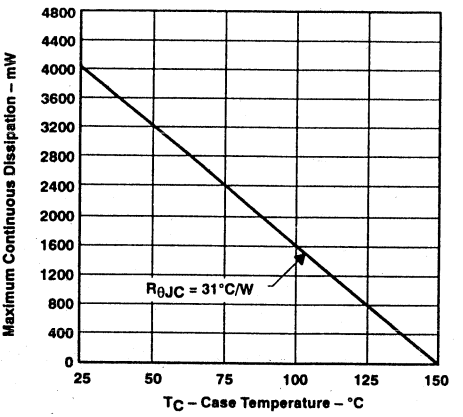


Figure 2

LEAD TEMPERATURE
DISSIPATION DERATING CURVE

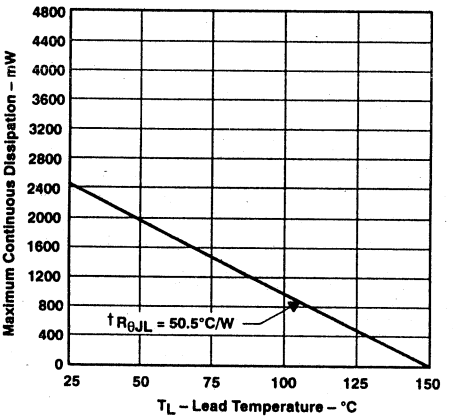


Figure 3

† $R_{\theta JL}$ is the thermal resistance between the junction and device lead. To determine the virtual junction temperature (T_J) relative to the device lead temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JL} + T_L$, where P_D is the internal power dissipation of the device, and T_L is the device lead temperature at the point of contact to the printed wiring board. $R_{\theta JL}$ is 50.5°C/W.

recommended operating conditions

	MIN	MAX	UNIT
Termination voltage	3.5	5.5	V
High-level disable input voltage, V_{IH}	2	V_{term}	V
Low-level disable input voltage, V_{IL}	0	0.8	V
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics, V_{term} = 4.75 V, V_O = 0.5 V, T_J = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output high voltage		2.5	2.85		V
TERMPWR supply current	All data lines open		9		mA
	All data lines = 0.5 V		228		
	$\overline{\text{DISABLE}}$ = 0 V		500		µA
Output current		−20.5	−23	−24	mA
Disable input current (see Note 1)	$\overline{\text{DISABLE}}$ = 4.75 V			1	µA
	$\overline{\text{DISABLE}}$ = 0 V			600	
Output leakage current	$\overline{\text{DISABLE}}$ = 0 V		100		nA
Output capacitance, device disabled	V_O = 0 V, 1 MHz		6		pF
Termination sink current, total	V_O = 4 V		20		mA

NOTE 1: If DISABLE is open or high, the terminator is active.

THERMAL INFORMATION

The need for smaller surface-mount packages for use on compact printed-wiring boards (PWB) causes an increasingly difficult problem in the area of thermal dissipation. In order to provide the systems designer with a better approximation of the junction temperature rise in the thin-shrink small-outline package (TSSOP), the junction-to-lead thermal resistance ($R_{\theta JL}$) is provided along with the more typical values of junction-to-ambient and junction-to-case thermal resistances, $R_{\theta JA}$ and $R_{\theta JC}$.

$R_{\theta JL}$ is used to calculate the device junction temperature rise measured from the leads of the unit. Consequently, the junction temperature is dependent upon the board temperature at the leads, $R_{\theta JL}$, and the internal power dissipation of the device. The board temperature is contingent upon several variables, including device packing density, thickness, material, area, and number of interconnects. The $R_{\theta JL}$ value depends on the number of leads connecting to the die-mount pad, the lead-frame alloy, area of the die, mount material, and mold compound. Since the power level at which the TSSOP can be used is highly dependent upon both the temperature rise of the PWB and the device itself, the systems designer can maximize this level by optimizing the circuit board. The junction temperature of the device can be calculated using the equation $T_J = (P_D \times R_{\theta JL}) + T_L$ where T_J = junction temperature, P_D = power dissipation, $R_{\theta JL}$ = junction-to-lead thermal resistance, and T_L = board temperature at the leads of the unit.

The values of thermal resistance for the TL2218-285 PW are as follows:

Thermal Resistance	Typical Junction Rise
$R_{\theta JA}$	151°C/W
$R_{\theta JC}$	31 °C/W
$R_{\theta JL}$	50.5°C/W

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_O	Output current	vs Input voltage	4
V_O	Output voltage	vs Input voltage	5
I_O	Output current	vs Junction temperature	6
V_O	Output voltage	vs Junction temperature	7

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
INPUT VOLTAGE

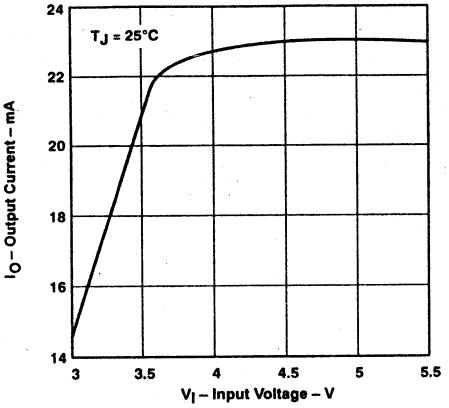


Figure 4

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

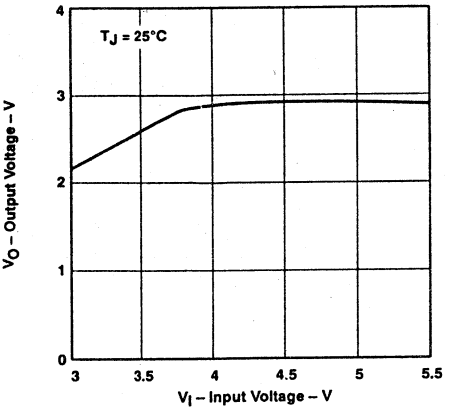


Figure 5

OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

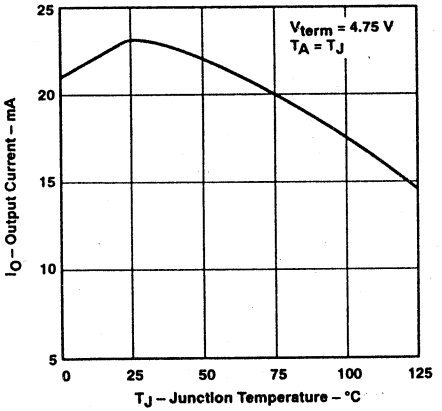


Figure 6

OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

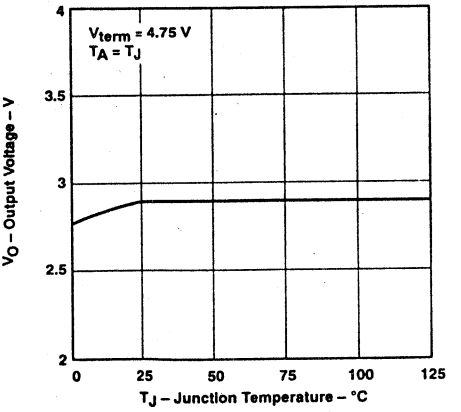


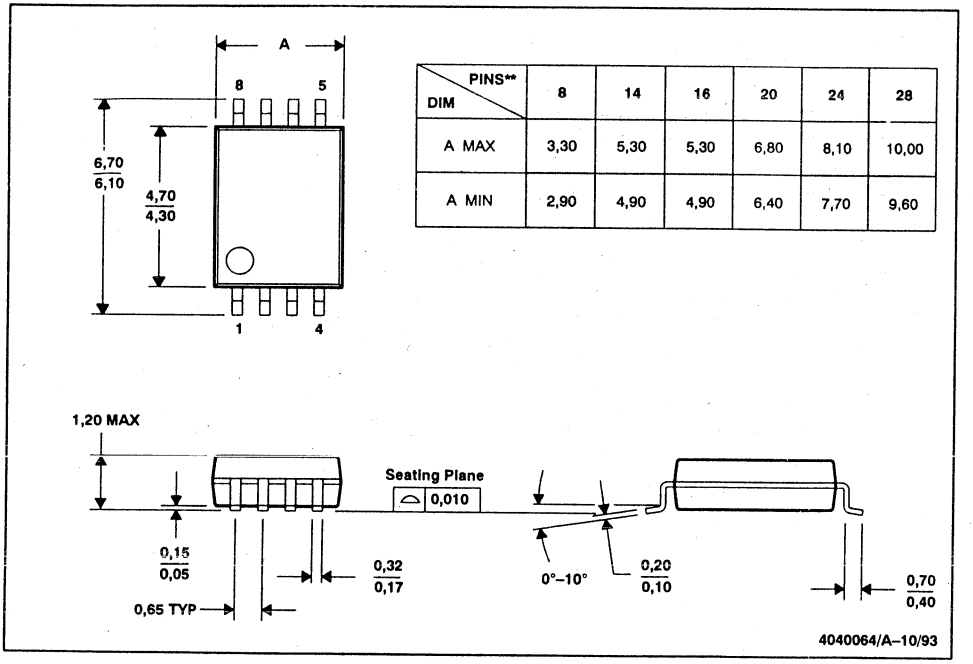
Figure 7

MECHANICAL DATA

PW/R-PDSO-G**

PLASTIC SMALL-OUTLINE PACKAGE

8-PIN SHOWN



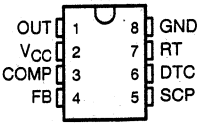
DIM \ PINS**	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Leads are within 0,127 radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

SLVS084A – APRIL 1994 – REVISED JULY 1994

- **Complete PWM Power Control**
- **3.6-V to 40-V Operation**
- **Internal Undervoltage-Lockout Circuit**
- **Internal Short-Circuit Protection**
- **Oscillator Frequency . . . 40 kHz to 400 kHz**
- **Variable Dead Time Provides Control Over Total Range**

D OR P PACKAGE
(TOP VIEW)



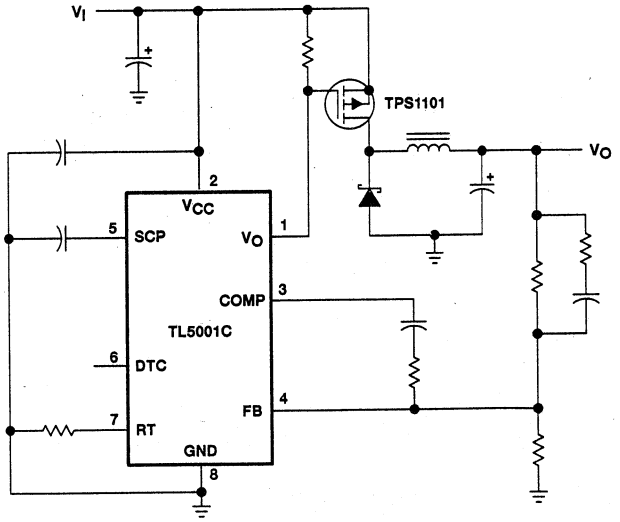
description

The TL5001C incorporates on a single monolithic chip all the functions required for a pulse-width-modulation (PWM) control circuit. Designed primarily for power-supply control, the TL5001C contains an error amplifier, a regulator, an oscillator, a PWM comparator with a dead-time-control input, undervoltage lockout (UVLO), short-circuit protection (SCP), and an open-collector output transistor.

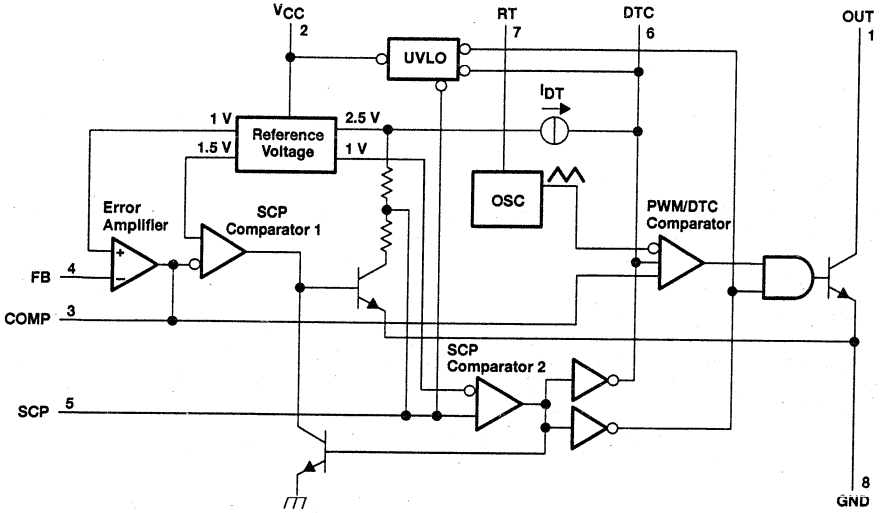
The error-amplifier common-mode voltage ranges from 0 V to 1.5 V. The noninverting input of the error amplifier is connected to a 1-V reference. Dead-time control (DTC) can be set to provide 0% to 100% dead time by connecting an external resistor between DTC and GND. The oscillator frequency is set by terminating RT with an external resistor to GND. During low V_{CC} conditions, the UVLO circuit turns the output off until V_{CC} recovers to its normal operating range.

The TL5001C is characterized for operation from –20°C to 85°C.

schematic for typical application



functional block diagram



detailed description

voltage reference

A 2.5-V regulator operating from V_{CC} is used to power the internal circuitry of the TL5001C and as a reference for the error amplifier and SCP circuits. A resistive divider provides a 1-V reference for the error amplifier noninverting input. The 1-V reference remains within 2% of nominal over the operating temperature range.

error amplifier

The error amplifier compares a sample of the dc-to-dc converter output voltage to the 1-V reference and generates an error signal for the PWM comparator. The dc-to-dc converter output voltage is set by selecting the error-amplifier gain (see Figure 1), using the following expression:

$$V_O = (1 + R1/R2)\ (1\ V)$$

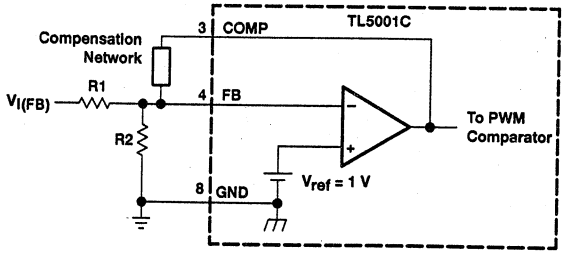


Figure 1. Error-Amplifier Gain Setting

error amplifier (continued)

The error-amplifier output is brought out as COMP for use in compensating the dc-to-dc converter control loop for stability. Because the amplifier can only source 45-μA, the total dc load resistance should be 100 kΩ or more.

oscillator/PWM

The oscillator frequency can be set between 40 kHz and 400 kHz by connecting a resistor between the timing resistor (RT) and GND. Acceptable resistor values range from 15 kΩ to 250 kΩ. The oscillator frequency can be determined by using the graph shown as Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error-amplifier output voltage and the DTC input voltage to the triangular wave and turns the output transistor off whenever the triangular wave is greater than the lesser of the two inputs.

dead-time control (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100 percent, which is critical for boost and flyback converters. A current source generates a reference current (I_{DT}) at DTC that is nominally equal to the current at the oscillator timing terminal, RT. Connecting a resistor between DTC and GND generates a dead-time reference voltage (V_{DT}), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0 percent when V_{DT} is 0.7 V or less and 100 percent when V_{DT} is 1.3 V or greater. Because the triangle wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250 Ω), choosing R_{DT} for a specific maximum duty cycle, D, is accomplished using the following equation and the voltage limits for the frequency in question as found in Figure 11 (V_{max} and V_{min} are the maximum and minimum oscillator levels):

$$R_{DT} = \left(R_t + 1250\right)\left[D\left(V_{max} - V_{min}\right) + V_{min}\right]$$

where

R_{DT} and R_t are in ohms, D in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor (C_{DT}) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT}R_{DT}\left(1 - e^{\left(-t/R_{DT}C_{DT}\right)}\right)$$

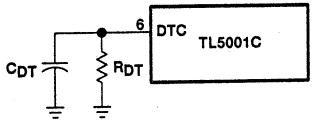


Figure 2. Soft-Start Circuit

If the dc-to-dc converter must be in regulation within a specified period of time, the time constant, $R_{DT}C_{DT}$, should be $t_0/3$ to $t_0/5$. The TL5001C remains off until $V_{DT} \approx 0.7$ V, the minimum ramp value. C_{DT} is discharged every time UVLO or SCP becomes active.

undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output transistor off and resets the SCP latch whenever the supply voltage drops too low (approximately 3 V) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

short-circuit protection (SCP)

The TL5001C includes short-circuit protection (see Figure 3), which turns the power switch off to prevent damage when the converter output is shorted. When activated, the SCP prevents the switch from being turned on until the internal latching circuit is reset. The circuit is reset by reducing the input voltage until UVLO becomes active or until the SCP terminal is pulled to ground externally.

When a short circuit occurs, the error-amplifier output at COMP rises to increase the power-switch duty cycle in an attempt to maintain the output voltage. SCP comparator 1 starts an RC timing circuit when COMP exceeds 1.5 V. If the short is removed and the error-amplifier output drops below 1.5 V before time out, normal converter operation continues. If the fault is still present at the end of the time-out period, the timer sets the latching circuit and turns the TL5001C output transistor off.

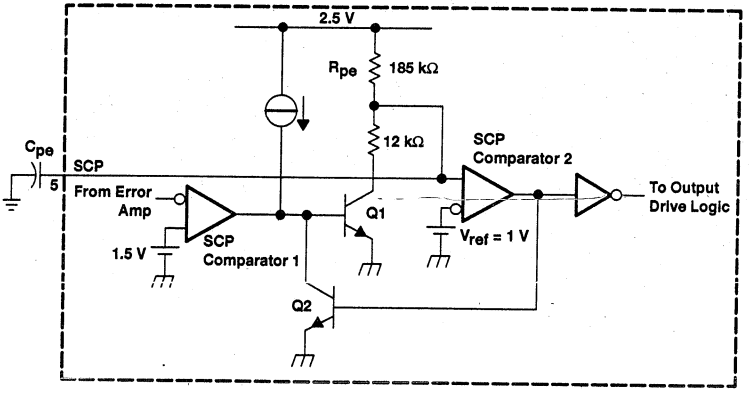


Figure 3. SCP Circuit

The timer operates by charging an external protection-enable capacitor (C_{pe}), connected between the SCP terminal and ground, towards 2.5 V through a 185-kΩ protection-enable resistor (R_{pe}). The circuit begins charging from an initial voltage of about 185 mV and times out when the capacitor voltage reaches 1 V and the output of SCP comparator 2 goes high, turns Q2 on, and latches the timer circuit. The expression for setting the SCP time period is derived from the following:

$$V_{SCP} - 0.185 = (2.5 - 0.185)\left(1 - e^{-t/\tau}\right)$$

where

$$\tau = R_{pe}C_{pe}$$

The end of the time-out period, t_{pe}, occurs when V_{SCP} = 1 V. Therefore, the capacitor for any given time is:

$$C_{pe} = 12.46 \times t_{pe}$$

where

t is in seconds, C in μF.

t_{pe} must be longer than the converter start-up period or the converter will not start.

output transistor

The output of the TL5001C is an open-collector transistor with a maximum collector current rating of 21 mA and a voltage rating of 51 V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, the UVLO circuit is inactive, and the short-circuit protection circuit is inactive.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 41 V
Amplifier input voltage, $V_{I(FB)}$ ..... 20 V
Collector output voltage, V_O ..... 51 V
Collector output current, I_O ..... 21 mA
Collector output peak current ..... 100 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating ambient temperature range, T_A ..... −20°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	975 mW	8.0 mW/°C	615 mW	495 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	3.6	40	V
Amplifier input voltage, $V_{I(FB)}$	0	1.5	V
Collector output voltage, V_O		50	V
Collector output current, I_O		20	mA
COMP source current		45	μA
COMP dc load resistance	100		kΩ
Oscillator timing resistor, R_t	15	250	kΩ
Oscillator frequency, f_{osc}	40	400	kHz
Operating ambient temperature, T_A	−20	85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted)

reference

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Output voltage	COMP connected to FB	0.95	1	1.05	V
Input regulation	V_{CC} = 3.6 V to 40 V		2	12.5	mV
Output voltage change with temperature	T_A = −20°C to 25°C	−10	−1	10	mV/V
	T_A = 25°C to 85°C	−10	−2	10	

‡ All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

undervoltage lockout

PARAMETER	MIN	TYP†	MAX	UNIT
Upper threshold voltage		3		V
Lower threshold voltage		2.8		V
Hysteresis	100	200		mV

short-circuit protection

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
SCP threshold voltage	T_A = 25°C	0.95	1	1.05	V
SCP voltage, latched	No pullup	140	185	230	mV
SCP voltage, UVLO standby	No pullup		60	120	mV
Timing resistance			185		kΩ
SCP comparator 1 threshold voltage			1.5		V

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Frequency	R_t = 100 kΩ		97		kHz
Standard deviation of frequency			15		kHz
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1		kHz
Frequency change with temperature	T_A = −20°C to 25°C	−4	−0.4	4	kHz
	T_A = 25°C to 85°C	−4	−0.2	4	
Voltage at RT			1		V

dead-time control

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output (source) current		0.9 × I_{RT}‡		1.1 × I_{RT}	μA
Input threshold voltage	Duty cycle = 0%	0.5	0.7		V
	Duty cycle = 100%		1.3	1.5	

error amplifier

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input voltage range		V_{CC} = 3.6 V to 40 V	0		1.5	V
Input bias current				−160	−500	nA
Output voltage swing	Positive		1.5	2.3		V
	Negative			0.3	0.4	V
Open-loop voltage amplification				80		dB
Unity-gain bandwidth				1.5		MHz
Output (sink) current		$V_{I(FB)}$ = 1.2 V, COMP = 1 V	100	600		μA
Output (source) current		$V_{I(FB)}$ = 0.8 V, COMP = 1 V	−45	−90		μA

† All typical values are at T_A = 25°C.
‡ Output source current at RT

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

output

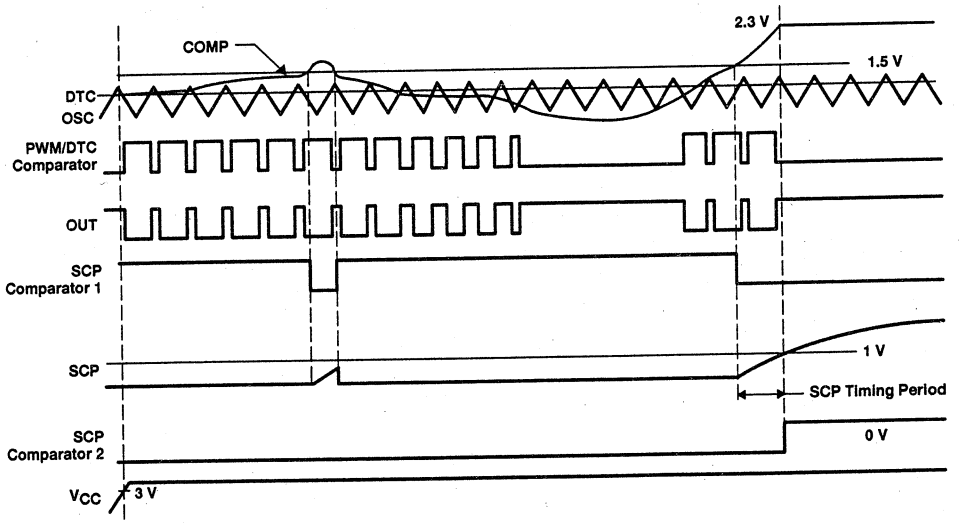
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output saturation voltage	I_O = 10 mA		1.5	2	V
Collector off-state current	V_O = 50 V, V_{CC} = 0			10	µA
	V_O = 50 V			10	
Short-circuit output current	V_O = 6 V		40		mA

total device

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Standby supply current	Off state			1	1.5	mA
Average supply current		R_t = 100 kΩ		1.1	2.1	mA

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTE A: The waveforms show timing characteristics for an intermittent short circuit and a longer short circuit that is sufficient to activate SCP.

Figure 4. PWM Timing Diagram

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY
vs
TIMING RESISTANCE

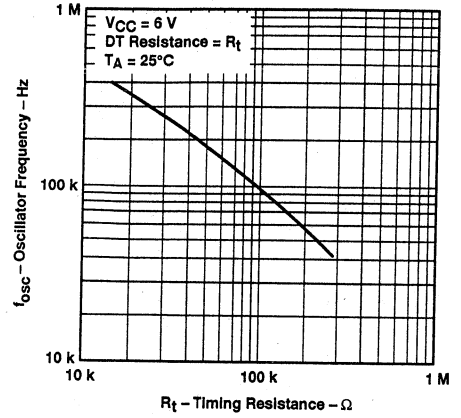


Figure 5

OSCILLATION FREQUENCY
vs
AMBIENT TEMPERATURE

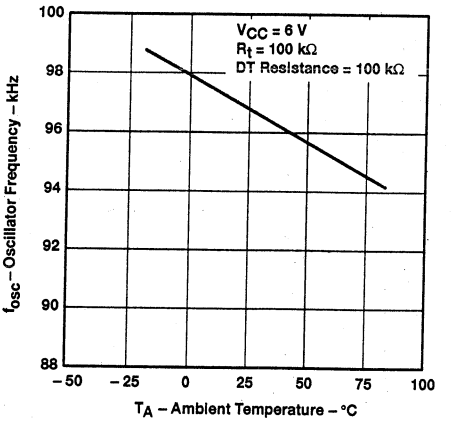


Figure 6

REFERENCE OUTPUT VOLTAGE
vs
POWER SUPPLY VOLTAGE

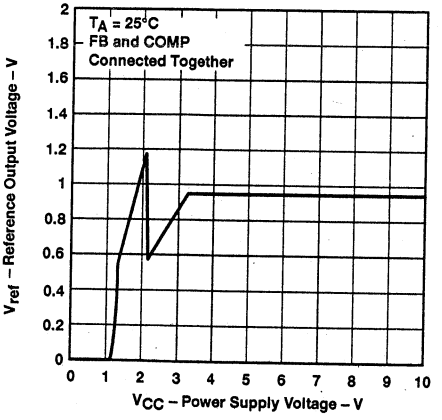


Figure 7

REFERENCE OUTPUT VOLTAGE FLUCTUATION
vs
AMBIENT TEMPERATURE

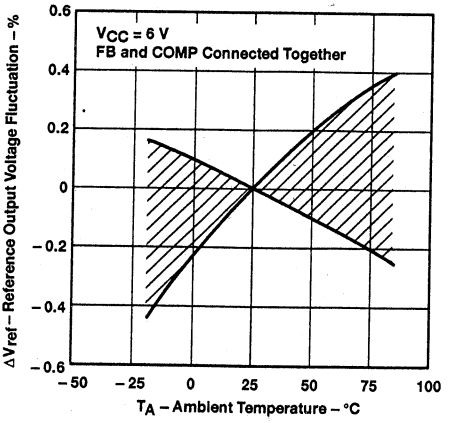


Figure 8

TYPICAL CHARACTERISTICS

AVERAGE STANDBY CURRENT
vs
POWER SUPPLY VOLTAGE

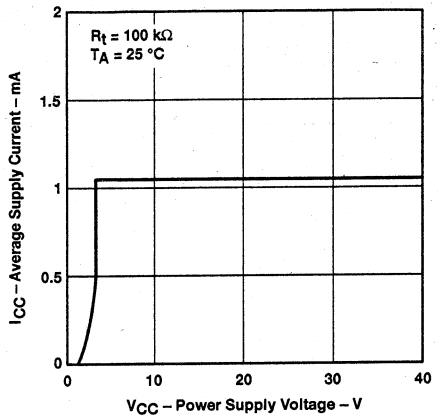


Figure 9

AVERAGE SUPPLY CURRENT
vs
AMBIENT TEMPERATURE

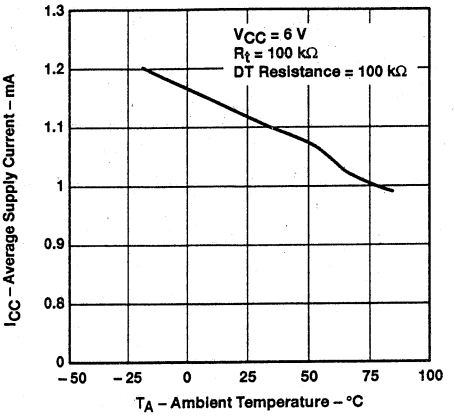


Figure 10

PWM TRIANGLE WAVE AMPLITUDE VOLTAGE
vs
OSCILLATOR FREQUENCY

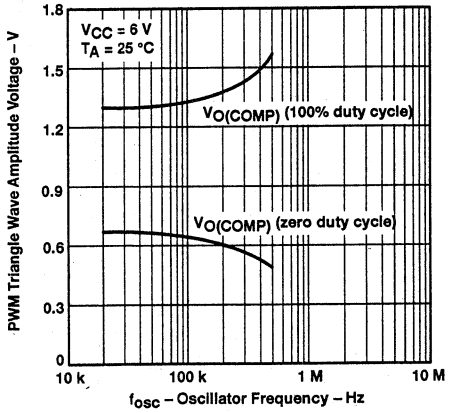


Figure 11

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
OUTPUT SINK CURRENT

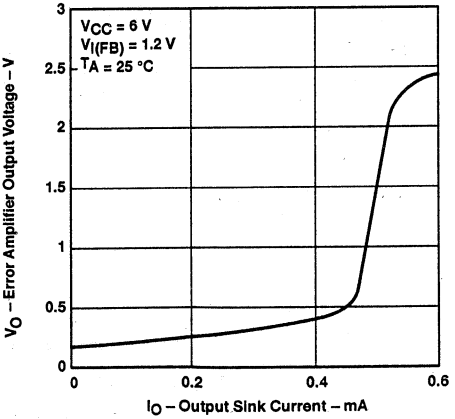


Figure 12

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
OUTPUT SOURCE CURRENT

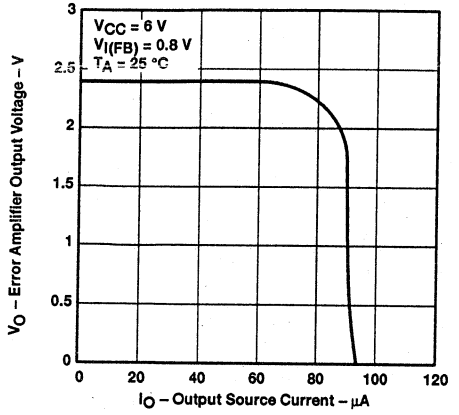


Figure 13

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
AMBIENT TEMPERATURE

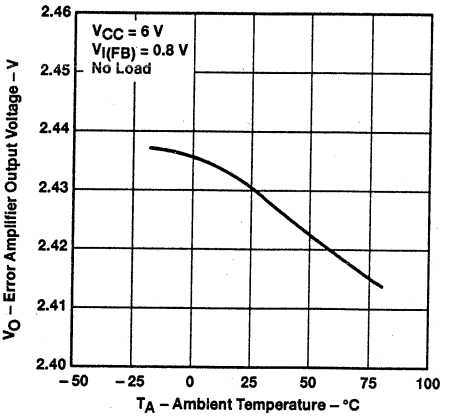


Figure 14

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
AMBIENT TEMPERATURE

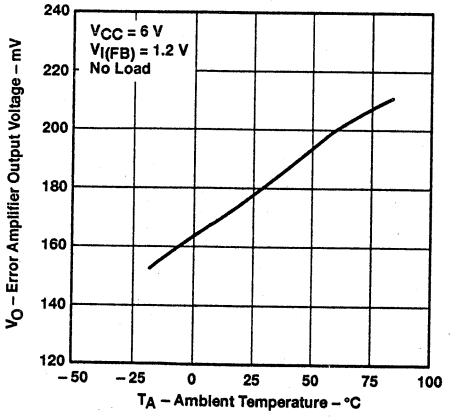


Figure 15

ERROR AMPLIFIER CLOSED-LOOP GAIN AND
PHASE SHIFT
vs
OSCILLATOR FREQUENCY

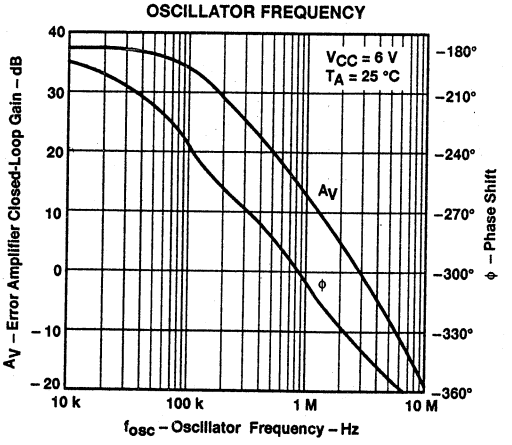


Figure 16

TYPICAL CHARACTERISTICS

OUTPUT DUTY CYCLE
vs
DTC VOLTAGE

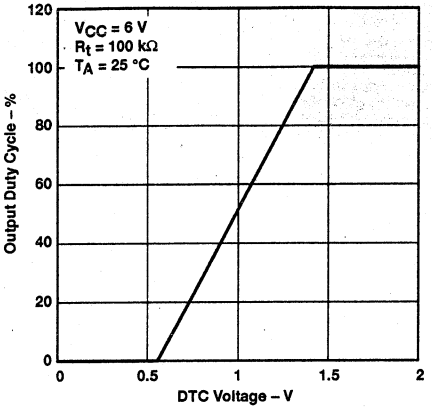


Figure 17

PROTECTION ENABLE TIME
vs
PROTECTION ENABLE CAPACITANCE

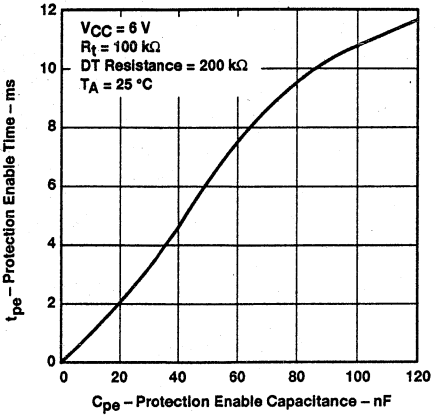


Figure 18

DTC OUTPUT CURRENT
vs
RT OUTPUT CURRENT

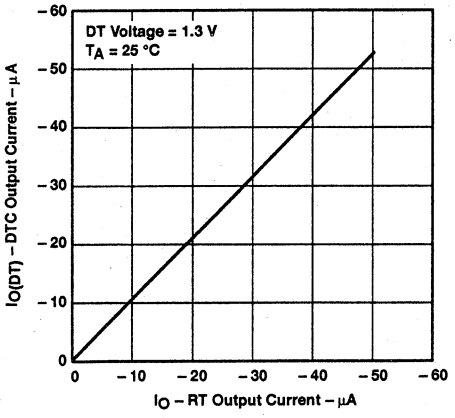


Figure 19

COLLECTOR SATURATION VOLTAGE
vs
OUTPUT SINK CURRENT

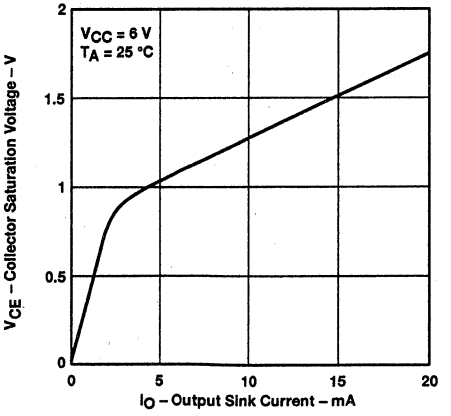
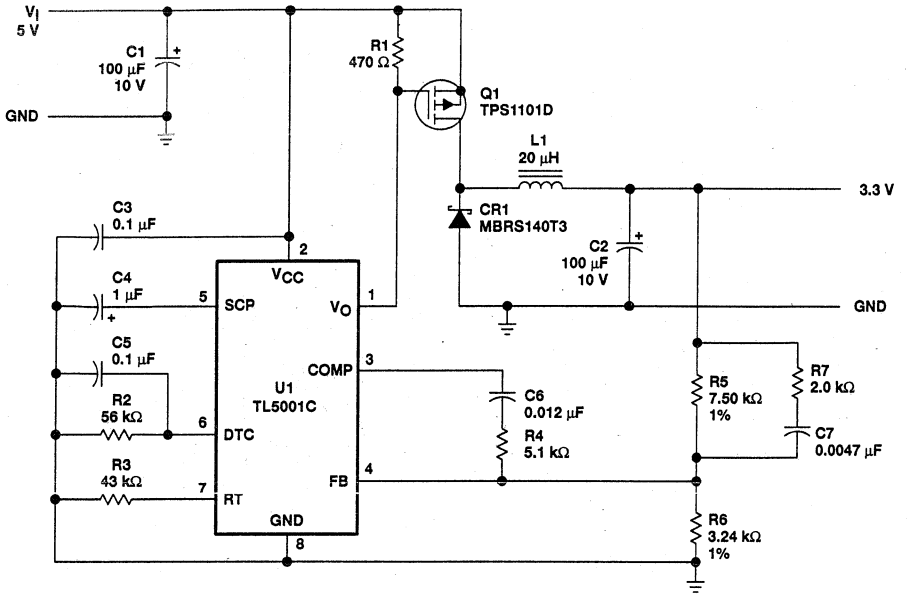


Figure 20

APPLICATION INFORMATION



NOTES: A. Frequency = 200 kHz
B. Duty cycle = 90% max
C. Soft-start time constant (TC) = 5.6 ms
D. SCP TC = 70 ms

Partial Bill of Materials:

U1	TL5001CD	Texas Instruments
Q1	TPS1101	Texas Instruments
LI	CTX20-1 or 23 turns of #28 wire on Micrometals No. T5O-26B core	Coiltronics
C1	TPSD107M010R0100	AVX
C2	TPSD107M010R0100	AVX
CR1	MBRS140T3	Motorola

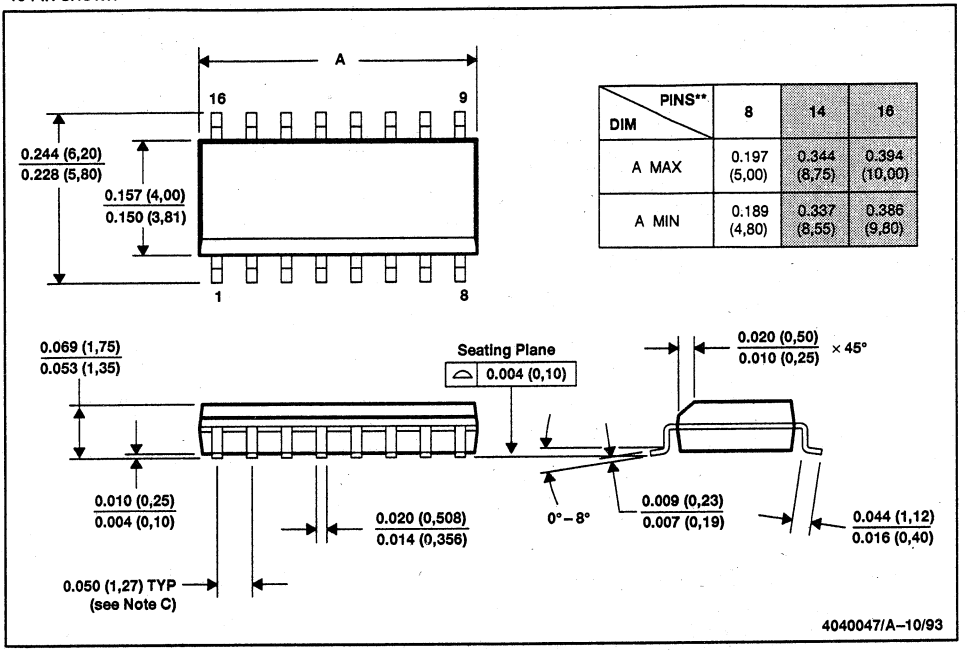
Figure 21. Step-Down Converter

MECHANICAL DATA

D/R-PDSO-G**

PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE

16-PIN SHOWN

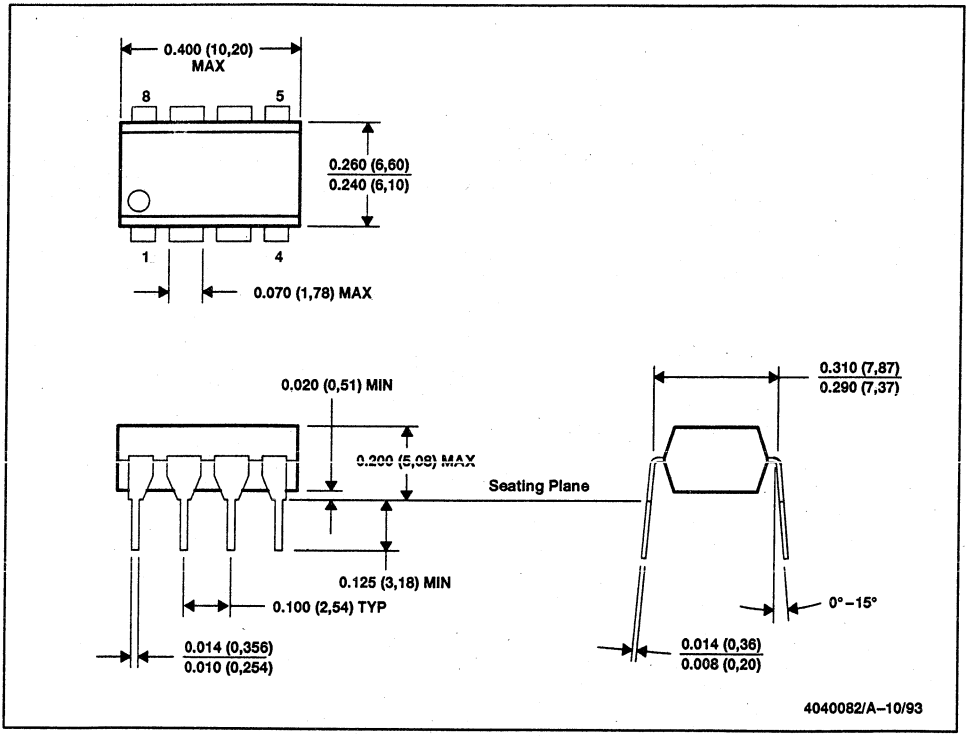


DIM \ PINS**	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.

MECHANICAL DATA

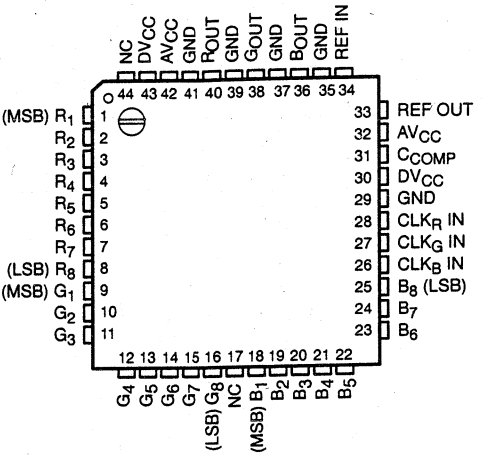
P/R-PDIP-T8 **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

- **8-Bit Resolution**
- **Linearity . . . ±1/2 LSB Maximum**
- **Differential Nonlinearity . . . ±1/2 LSB Maximum**
- **Conversion Rate . . . 60 MHz Min**
- **Nominal Output Signal Operating Range V_{CC} to V_{CC} – 1 V**
- **TTL Digital Input Voltage**
- **5-V Single Power Supply Operation**
- **Low Power Consumption . . . 350 mW Typ**

FR PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL5632C is a low-power ultra-high-speed video digital-to-analog converter that uses the Advanced Low-Power Schottky (ALS) process. The device has a three channel I/O; the red, the blue, and the green channel. The red, blue, and green signals are referred to collectively as the RGB signal. An internally generated reference is also provided for the standard video output voltage range. Conversion of digital signals to analog signals can be at a sampling rate of dc to 60 MHz. The high conversion rate makes the TL5632C suitable for digital television, computer digital video processing, and high-speed data conversion.

The TL5632C is characterized for operation from 0°C to 70°C.

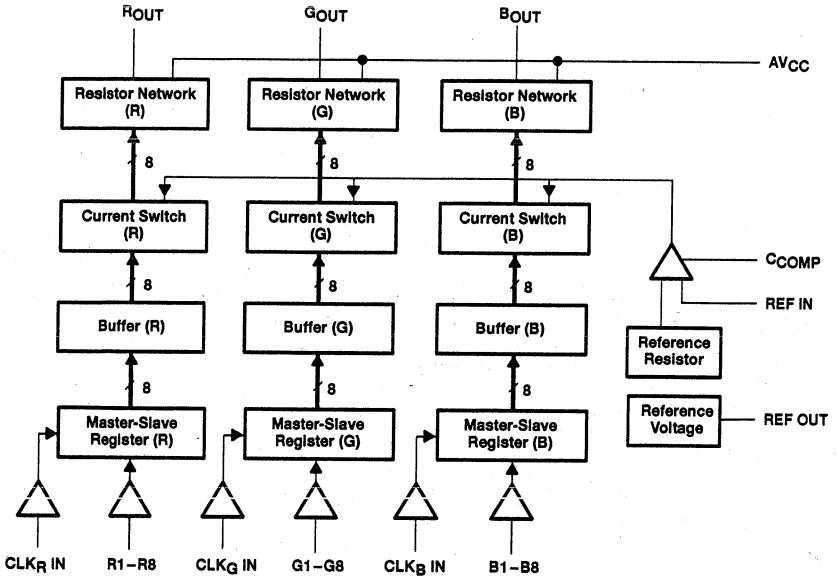
FUNCTION TABLE

STEP	DIGITAL INPUT	OUTPUT VOLTAGE
0	LLLLLLLL	3.980 V
1	LLLLLLLH	3.984 V
•	•	•
•	•	•
•	•	•
127	LHHHHHHH	4.488 V
128	HLLLLLLL	4.492 V
129	HLLLLLLH	4.996 V
•	•	•
•	•	•
•	•	•
254	HHHHHHHL	4.996 V
255	HHHHHHHH	5.000 V

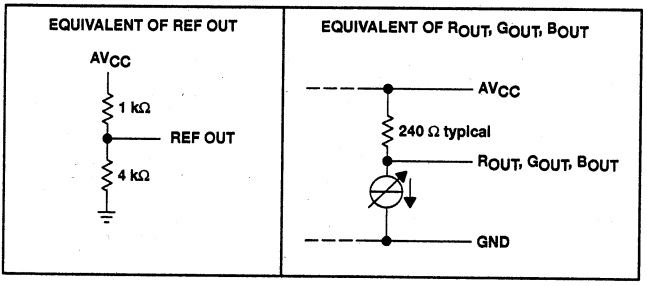
AVAILABLE OPTIONS

T_A	PACKAGE
0°C to 70°C	TL5632CFR

functional block diagram



schematics of outputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$B_1 - B_8$	18 – 25	I	B-channel digital input (B_1 = MSB)
B_{OUT}	36	O	B-channel analog output
C_{COMP}	31		Phase compensation capacitance. A 1 μF capacitor is connected from C_{COMP} to GND.
CLK_B IN	26	I	B-channel clock input
CLK_G IN	27	I	G-channel clock input
CLK_R IN	28	I	R-channel clock input
$G_1 - G_8$	9 – 16	I	G-Channel digital input (G_1 = MSB)
GND	29, 35, 37, 39, 41		Ground. All GND terminals are connected internally; however, all GND terminals should be connected externally to a ground plane or equivalent low impedance ground return.
G_{OUT}	38	O	G-channel analog output
NC	17, 44		No connection internally
$R_1 - R_8$	1 – 8	I	R-channel digital input (R_1 = MSB)
R_{OUT}	40	O	R-channel analog output
AV_{CC}	32, 42		Analog power supply voltage
DV_{CC}	30, 43		Digital power supply voltage
REF IN	34	I	Reference voltage input. REF IN accepts the reference voltage on REF OUT. An external reference can also be applied consistent with Note 1.
REF OUT	33	O	Reference voltage output. An internal voltage divider generates the voltage level (see schematics of outputs, page 2).

NOTE 1: $V_{CC} - V_{ref} \leq 1.2$ V

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Power supply voltage range, AV_{CC}, DV_{CC} (see Note 2) ..... −0.3 V to 7 V
Digital input voltage range, V_I ..... −0.3 V to DV_{CC}
Analog output voltage range, R_{OUT}, G_{OUT}, B_{OUT}, C_{COMP} (externally applied) .... −0.3 V to AV_{CC} + 0.3 V
Reference input range, REF IN ..... −0.3 V to AV_{CC} + 0.3 V
Reference output range, REF OUT ..... −0.3 V to AV_{CC} + 0.3 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, AV_{CC}, DV_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref} (see Note 1)	3.8	4	4.2	V
Setup time, data before CLK↑, t_{su1}	10			ns
Hold time, data after CLK↑, t_{h1}	3			ns
Pulse duration at high level, t_{w1}	8.3			ns
Pulse duration at low level, t_{w2}	8.3			ns
External phase compensation capacitance, C_{COMP}	1			µF
Operating free-air temperature, T_A	0		70	°C

NOTE 1: $V_{CC} - V_{ref} \leq 1.2$ V

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

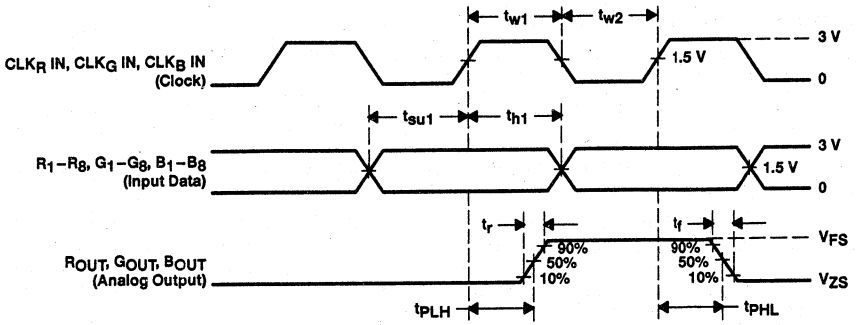
	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Resolution					8	Bit
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_{IH} = 2.7 V			20	µA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_{IH} = 2.7 V	−400			µA
I_{ref}	Reference input current	REF IN = 4 V				10	µA
V_{ref}	Reference output voltage	V_{CC} = 5 V,	With internal reference	3.8	4	4.2	V
V_{FS}	Full-scale analog output voltage	V_{IH} = 2 V,	REF IN = 4 V	AV_{CC}−15	AV_{CC}	AV_{CC}+15	mV
V_{ZS}	Zero-scale analog output voltage	V_{IL} = 0.8 V,	REF IN = 4 V	3.9	3.98	4.05	V
	RGB full-scale ratio			0%	4%	8%	
z_o	Output impedance			200	240	280	Ω
I_{CC}	Supply current				70	90	mA

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
E_L	Linearity error	End point,	REF IN = 4 V			±0.5	LSB
E_D	Differential linearity error	REF IN = 4 V				±0.5	LSB
f_c	Maximum conversion rate			60			MHz
t_{PLH}	Propagation delay time, low-to-high level	T_A = 25°C,	$C_L \leq 5$ pF‡		10		ns
t_{PHL}	Propagation delay time, high-to-low level				10		
t_r	Rise time				5		ns
t_f	Fall time				5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ C_L includes probe and jig capacitances.

PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

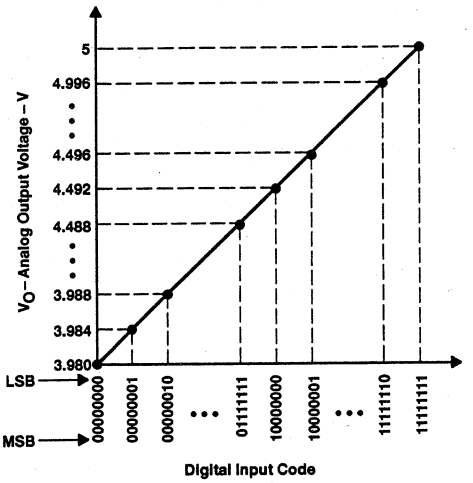


Figure 1. Ideal Conversion Characteristics

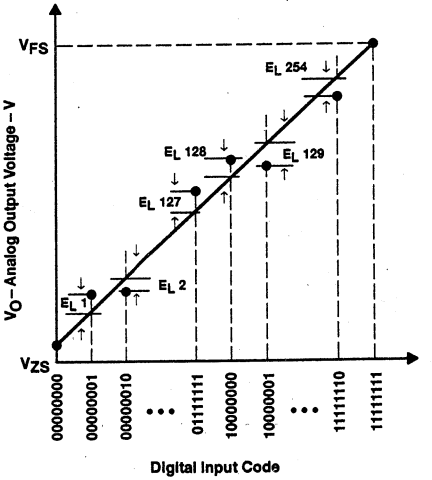


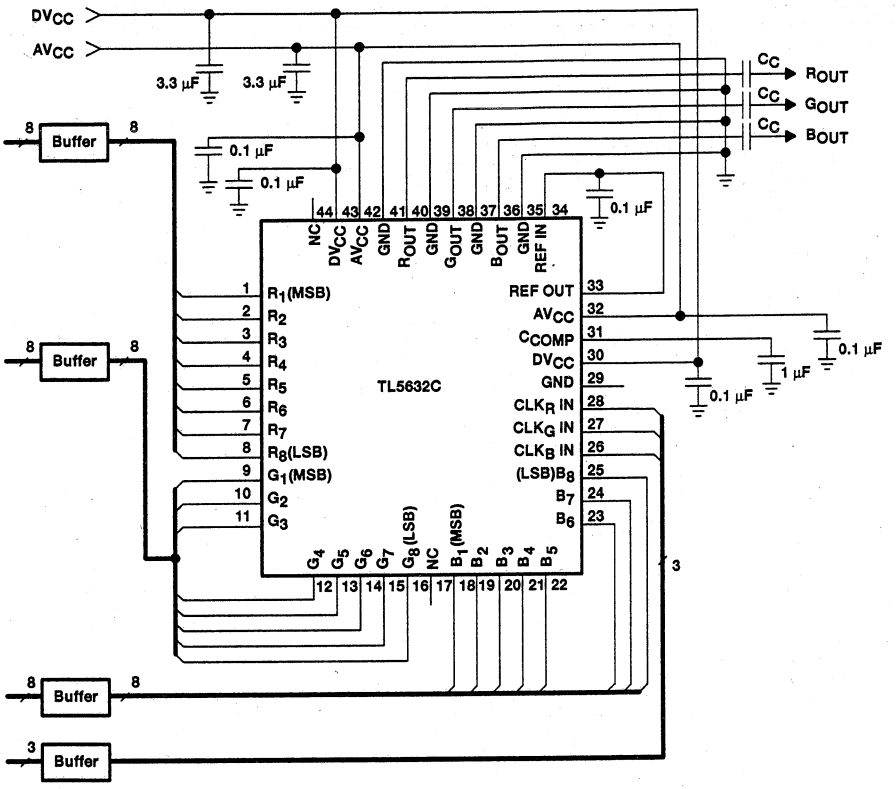
Figure 2. End-Point Linearity Error

APPLICATION INFORMATION

The following design procedures should be used for optimum operation.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. A ground plane is the better choice for noise reduction.
- AV_{CC} and DV_{CC} are also separate internally, so they must be connected externally. These external PCB leads should also be made as wide as possible. A ferrite bead or equivalent inductance should be placed in series with AV_{CC} and the decoupling capacitor before the AV_{CC} and DV_{CC} leads are connected together on the board. It is critical that the supply voltage applied to AV_{CC} be as noise free and ripple free as possible. Ripple and noise rejection should be a minimum of 60 dB below the full-scale output range of 1 V peak-to-peak.
- AV_{CC} to GND and DV_{CC} to GND should be decoupled with 3.3-µF and 0.1-µF capacitors, respectively, as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.1-µF capacitor.
- The phase compensation capacitor should be connected between C_{COMP} and GND with as short a lead-in as possible.
- The no-connection (NC) terminals on the small-outline package should be connected to GND.
- AV_{CC}, DV_{CC}, and R_{OUT}, G_{OUT}, and B_{OUT} should be shielded from the high-frequency terminals CLK_R IN, CLK_G IN, and CLK_B IN and the input data terminals. GND traces should be placed on both sides of the R_{OUT}, G_{OUT}, and B_{OUT} traces on the PCB to the following signal processing stage. These output traces should be as short as possible.

APPLICATION INFORMATION

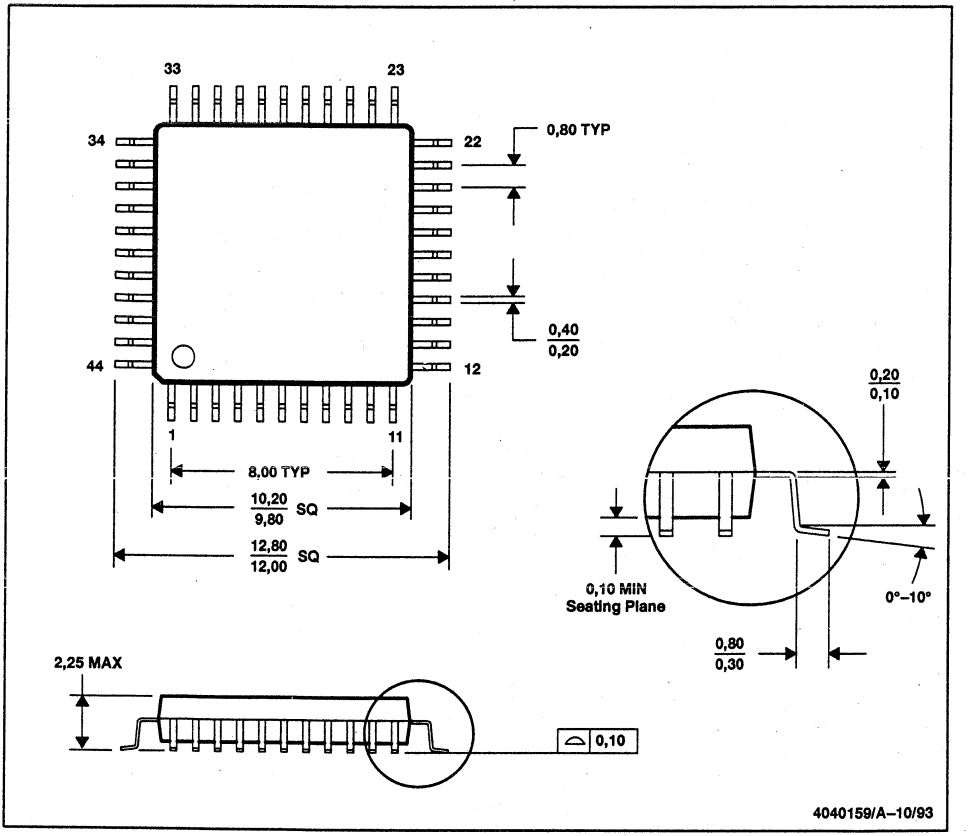


NOTES: A. Buffers are SN74AS244 or equivalent.
B. 0.1 µF capacitors should be placed as close to the device terminals as possible.
C. The coupling capacitor (C_C) value is application specific and selectable by the user.

Figure 3. Typical Bypass, Buffer, and Output Configuration

MECHANICAL DATA

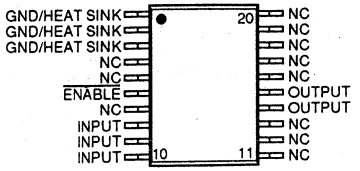
FR/S-PQFP-G44 PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

- **Very Low-Dropout Voltage . . . Less Than 400 mV at 300 mA**
- **Standby Mode Reduces Current to a Maximum of 150 µA**
- **Output Regulated to Within ±2% Over Full Temperature Range**
- **Packaged in Thin Shrink Small-Outline Package**
- **Only 10-µF Load Capacitor Required to Maintain Regulation at I_O = 300 mA**

PW PACKAGE†
(TOP VIEW)



GND/HEAT SINK – These pins have an internal connection to ground and must be grounded.
NC – No internal connection
†The PW package is only available in left-end taped and reeled (order device TL75LPXXQPWLE).

description

The TL75LPXXQ devices are low-dropout voltage regulators specifically targeted for use in portable applications. These devices generate fixed output voltages at loads of up to 300 mA with only 400-mV dropout over the full temperature range.

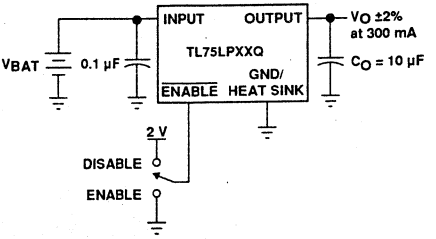
Low-dropout voltage regulators are commonly used in battery-powered systems such as analog and digital cellular phones. The TL75LPXX family of regulators feature a TTL/CMOS-compatible enable pin which can be used to switch the device into standby mode. This feature reduces power consumption when the instrument is not active. Less than 150 µA is required when the unit is disabled.

A concern in many new designs is conservation of board space and overall reduction in equipment size. The TI thin shrink small-outline package (TSSOP) minimizes board area and reduces component height (headroom). This package has a maximum height of less than 1.1 mm (less than a standard 8-pin SO package) and dimensions of only 6.5 mm by 4.4 mm.

All low-dropout regulators require an external capacitor at the output to maintain regulation and stability. To further reduce board area and cost, the TL75LPXX devices are designed to require a minimum capacitor of only 10 µF. This is 1/10 the typical value used by many other low-dropout regulators. To simplify the task of choosing a suitable capacitor, TI has included in this datasheet a list of recommended capacitors for use with these devices.

The TL75LPXXQ devices are characterized for operation over a virtual junction temperature range of –40°C to 125°C.

typical application schematic

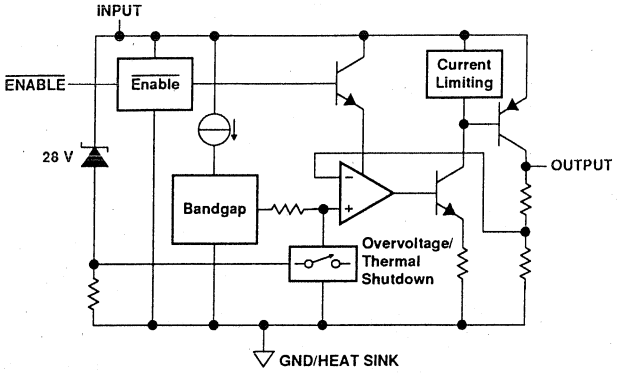


available options

PART NUMBER	OUTPUT VOLTAGE			UNIT
	MIN	TYP	MAX	
TL75LP48QPWLE	4.75	4.85	4.95	V
TL75LP48Y				
TL75LP05QPWLE	4.9	5	5.1	
TL75LP05Y				
TL75LP08QPWLE	7.84	8	8.16	
TL75LP08Y				
TL75LP10QPWLE	9.8	10	10.2	
TL75LP10Y				
TL75LP12QPWLE	11.76	12	12.24	
TL75LP12Y				

TEXAS INSTRUMENTS

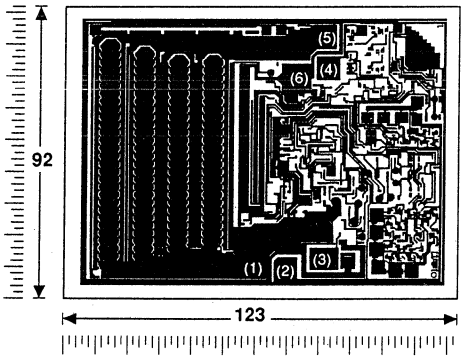
functional block diagram

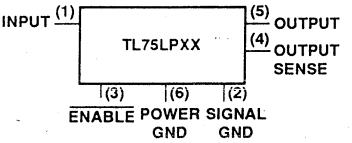


TL75LPXXY chip information

Thermal compresson or ultrasonic bonding may be used on the doped aluminum bonding pad. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 TYPICAL

BONDING PADS: 7 X 7 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

NOTE: SIGNAL GND and POWER GND must be tied together as close to device as possible. OUTPUT and OUTPUT SENSE should be tied together.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}† . . . . . 25 V
Output current . . . . . 400 mA
Operating virtual junction temperature range, T_J . . . . . – 55°C to 150°C
Continuous total power dissipation (see Note 1) . . . . . See Dissipation Rating Table
Storage temperature range . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† All voltage values are with respect to network terminal ground.

NOTE 1: Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
PW	T_A	828 mW	6.62 mW/°C	530 mW	430 mW	165 mW
	T_C	4032 mW	32.2 mW/°C	2580 mW	2086 mW	806 mW
	T_P‡	2475 mW	19.8 mW/°C	1584 mW	1287 mW	495 mW

‡ $R_{\theta JP}$ is the thermal resistance between the junction and the device pin. To determine the virtual junction temperature (T_J) relative to the device pin temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JP} + T_P$, where P_D is the internal power dissipation of the device and T_P is the device pin temperature at the point of contact to the printed wiring board. The $R_{\theta JP}$ for the TL75LPXX series is 50.5°C/W.

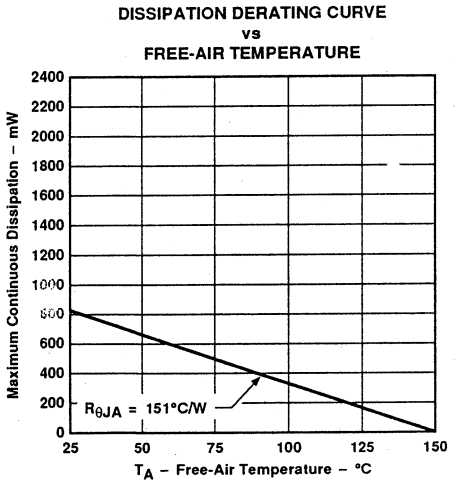


Figure 1

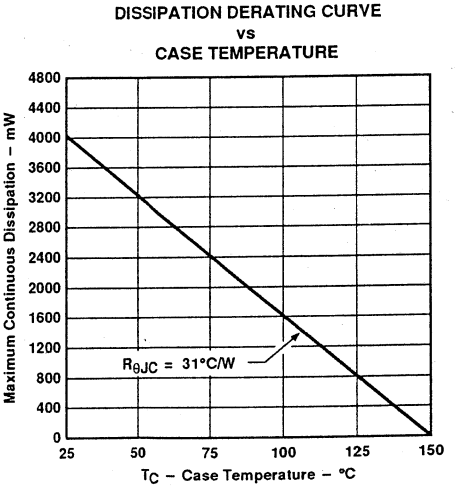


Figure 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	TL75LP48	5.15	23.0	V
	TL75LP05	5.3	23.0	
	TL75LP08	8.4	23.0	
	TL75LP10	10.4	23.0	
	TL75LP12	12.5	23.0	
High-level input voltage, $\overline{ENABLE}$, V_{IH}		2.0	15.0	V
Low-level input voltage, $\overline{ENABLE}$, V_{IL}		0	0.8	V
Output current range, I_O		5	300	mA
Operating virtual junction temperature range, T_J		–40	125	°C

TL75LP48Q electrical characteristics over operating virtual junction temperature range, V_I = 10 V, I_O = 300 mA, $\overline{ENABLE}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 5.35 V to 10 V	4.75	4.85	4.95	V
Input regulation	V_I = 5.35 V to 10 V, T_J = 25°C		10	25	mV
Ripple rejection	V_I = 5.6 V to 15.6 V, f = 120 Hz, T_J = 25°C	50	55		dB
Output regulation	I_O = 5 mA to 300 mA, T_J = 25°C		12	30	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, T_J = 25°C		500		μV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{ENABLE}$	$\overline{ENABLE}$ = 0.8 V		7	25	μA
Low-level input current, $\overline{ENABLE}$	$\overline{ENABLE}$ = 2 V		0.05	6	μA
Standby current	$\overline{ENABLE}$ = 2 V		100	150	μA

†Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum capacitor. Although not normally recommended, an electrolitic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

TL75LP05Q electrical characteristics over operating virtual junction temperature range, V_I = 10 V, I_O = 300 mA, $\overline{ENABLE}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 5.5 V to 10 V	4.9	5	5.1	V
Input regulation	V_I = 5.5 V to 10 V, T_J = 25°C		10	25	mV
Ripple rejection	V_I = 6 V to 16 V, f = 120 Hz, T_J = 25°C	50	55		dB
Output regulation	I_O = 5 mA to 300 mA, T_J = 25°C		12	30	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, T_J = 25°C		500		μV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{ENABLE}$	$\overline{ENABLE}$ = 0.8 V		7	25	μA
Low-level input current, $\overline{ENABLE}$	$\overline{ENABLE}$ = 2 V		0.05	6	μA
Standby current	$\overline{ENABLE}$ = 2 V		100	150	μA

TL75LP08Q electrical characteristics over operating virtual junction temperature range, V_I = 10 V, I_O = 300 mA, $\overline{ENABLE}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 8.6 V to 15 V	7.84	8	8.16	V
Input regulation	V_I = 8.6 V to 15 V, T_J = 25°C		12	40	mV
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz, T_J = 25°C	50	55		dB
Output regulation	I_O = 5 mA to 300 mA, T_J = 25°C		12	40	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, T_J = 25°C		500		μV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{ENABLE}$	$\overline{ENABLE}$ = 0.8 V		7	25	μA
Low-level input current, $\overline{ENABLE}$	$\overline{ENABLE}$ = 2 V		0.05	6	μA
Standby current	$\overline{ENABLE}$ = 2 V		100	150	μA

†Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum capacitor. Although not normally recommended, an electrolitic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

TL75LP10Q electrical characteristics over operating virtual junction temperature range, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 10.6 V to 17 V	9.8	10	10.2	V
Input regulation	V_I = 10.6 V to 17 V, T_J = 25°C		15	43	mV
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz, T_J = 25°C	50	55		dB
Output regulation	I_O = 5 mA to 300 mA, T_J = 25°C		15	50	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, T_J = 25°C		1000		μV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7	25	μA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05	6	μA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100	150	μA

TL75LP12Q electrical characteristics over operating virtual junction temperature range, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 12.7 V to 18 V	11.76	12	12.24	V
Input regulation	V_I = 12.7 V to 18 V, T_J = 25°C		15	43	mV
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz, T_J = 25°C	50	55		dB
Output regulation	I_O = 5 mA to 300 mA, T_J = 25°C		15	60	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, T_J = 25°C		1000		μV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7	25	μA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05	6	μA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100	150	μA

†Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum capacitor. Although not normally recommended, an electrolitic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

TL75LP48Y electrical characteristics at V_I = 10 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ = 0 V, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 5.35 V to 10 V	4.75	4.85	4.95	V
Input regulation	V_I = 5.35 V to 10 V		10	25	mV
Ripple rejection	V_I = 5.6 V to 15.6 V, f = 120 Hz		55		dB
Output regulation	I_O = 5 mA to 300 mA		12	30	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7	25	μA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05	6	μA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100	150	μA

TL75LP05Y electrical characteristics at V_I = 10 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ = 0 V, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 5.5 V to 10 V	4.75	5	5.1	V
Input regulation	V_I = 5.5 V to 10 V		10	25	mV
Ripple rejection	V_I = 6 V to 16 V, f = 120 Hz		55		dB
Output regulation	I_O = 5 mA to 300 mA		12	30	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7	25	μA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05	6	μA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100	150	μA

†Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum capacitor. Although not normally recommended, an electrolitic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

TL75LP08Y electrical characteristics at V_I = 10 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ = 0 V, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 8.6 V to 15 V	7.84	8	8.16	V
Input regulation	V_I = 8.6 V to 15 V		12	40	mV
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz		55		dB
Output regulation	I_O = 5 mA to 300 mA		12	40	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7	25	μA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05	6	μA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100	150	μA

TL75LP10Y electrical characteristics at V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ = 0 V, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 10.6 V to 17 V	9.8	10	10.2	V
Input regulation	V_I = 10.6 V to 17 V		15	43	mV
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz		55		dB
Output regulation	I_O = 5 mA to 300 mA		15	50	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz		1000		μV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7	25	μA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05	6	μA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100	150	μA

†Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum capacitor. Although not normally recommended, an electrolitic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

TL75LP12Y electrical characteristics at V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ = 0 V, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 12.7 V to 18 V	11.76	12	12.24	V
Input regulation	V_I = 12.7 V to 18 V		15	43	mV
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		55		dB
Output regulation	I_O = 5 mA to 300 mA		12	60	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7	25	μA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05	6	μA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100	150	μA

†Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum capacitor. Although not normally recommended, an electrolitic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

PARAMETER MEASUREMENT INFORMATION

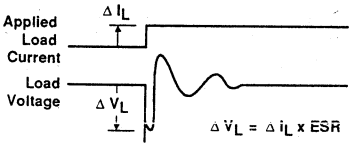
The TL75LPXX series are low-dropout voltage regulators. This means that the capacitance is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can be used to establish the capacitance value and ESR range for optimum regulator performance.

Figure 3 shows the recommended range of ESR, measured at 120 Hz, for a given load with a 10-µF capacitor on the output. In addition, it shows a maximum ESR limit of 2 Ω and a load dependent minimum ESR limit.

For applications with varying loads, the lightest load condition should be chosen since it is the worst case. Figure 4 shows the relationship of the reciprocal of ESR to the square root of the capacitance with a minimum capacitance limit of 10 µF and a maximum ESR limit of 2 Ω. Figure 4 is used to establish the amount that the minimum ESR limit of Figure 3 can be adjusted for different capacitor values. For example, if the minimum load needed is 200 mA, Figure 3 suggests an ESR range of 0.8 Ω to 2 Ω for 10 µF. Figure 4 shows that changing the capacitor from 10 µF to 400 µF can change the ESR minimum by greater than 3/0.5 (or 6). Therefore, the new minimum ESR value is 0.8/6 (or 0.13 Ω). This now allows an ESR range of 0.13 Ω to 2 Ω. This expanded ESR range is achieved by using a larger capacitor at the output. For better stability in low-current applications, it is recommended that a small resistance be placed in series with the capacitor (see Table 1) so that the ESR better approximates those in Figures 3 and 4.

Table 1. Compensations for Increased Stability at Low Currents

MANUFACTURE	CAPACITANCE	ESR TYP	PART NUMBER	ADDITIONAL RESISTANCE
AVX	15 µF	0.9 Ω	TAJB156M010S	1 Ω
KEMET	33 µF	0.6 Ω	T491D336M010AS	0.5 Ω



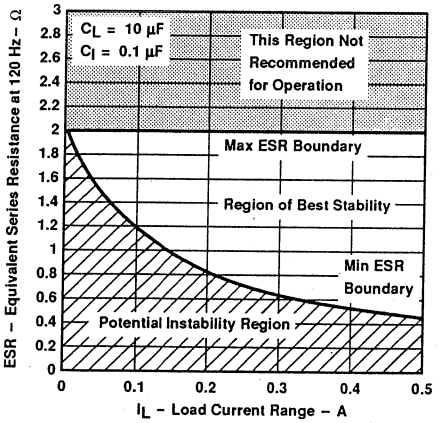


Figure 3

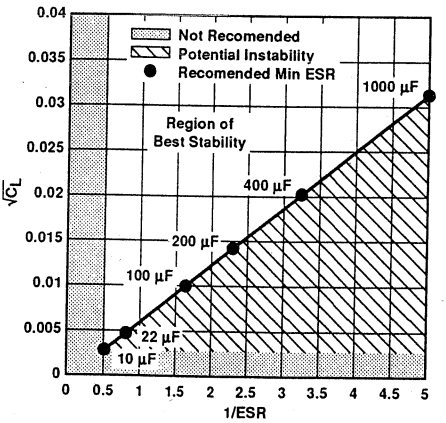


Figure 4

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
Output voltage		vs Input voltage	5
Input current	10 mA	vs Input voltage	6
	100 mA	vs Input voltage	7
Dropout voltage		vs Output current	8
Quiescent current		vs Output current	9
Short-circuit protection conditions Output voltage		vs Output current	10
Load transient response		vs Time	11
Line transient response		vs Time	12

TYPICAL CHARACTERISTICS

TL75LP05
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

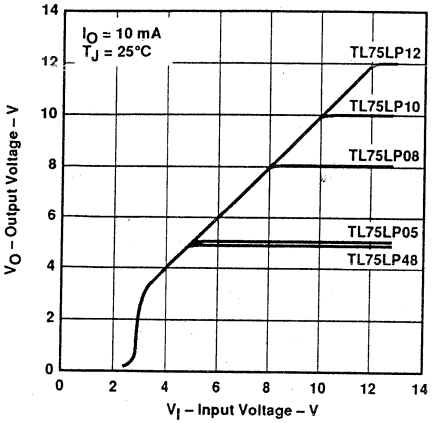


Figure 5

INPUT CURRENT
vs
INPUT VOLTAGE

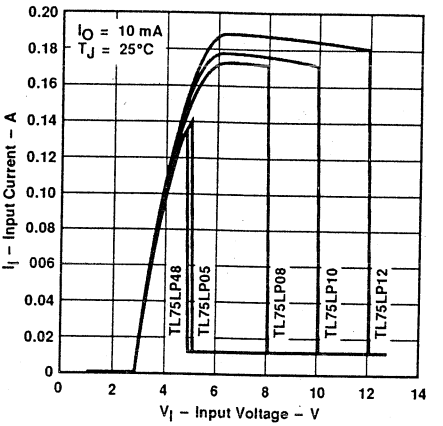


Figure 6

INPUT CURRENT
vs
INPUT VOLTAGE

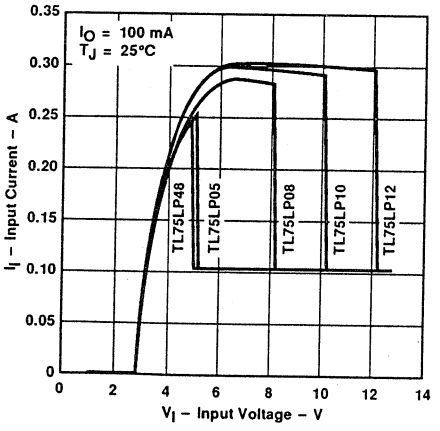


Figure 7

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

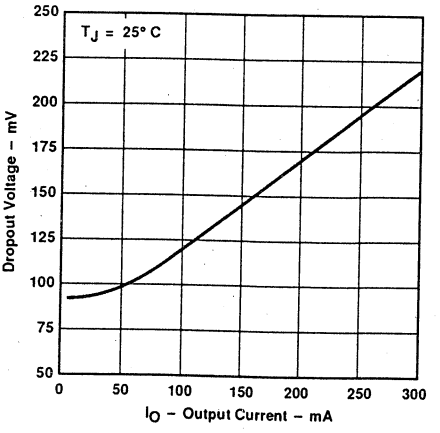


Figure 8

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT
vs
OUTPUT CURRENT

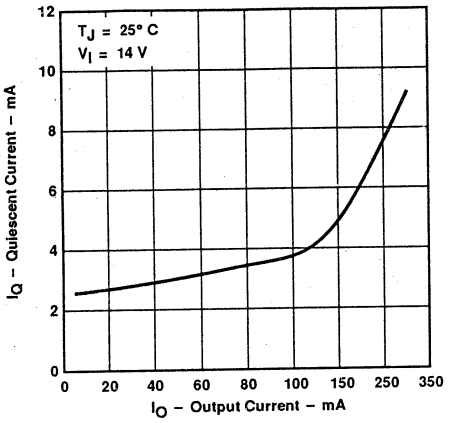


Figure 9

SHORT-CIRCUIT PROTECTION CONDITIONS
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

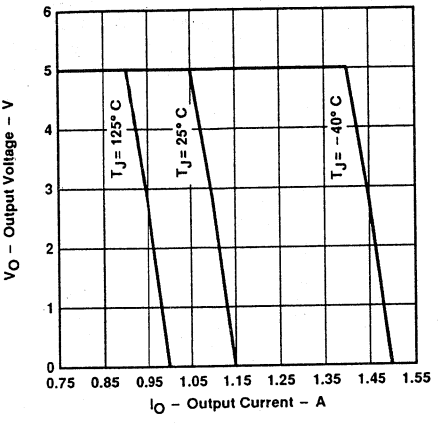


Figure 10

LOAD TRANSIENT RESPONSE

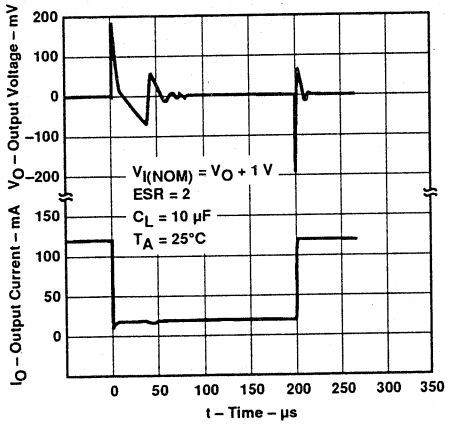


Figure 11

LINE TRANSIENT RESPONSE

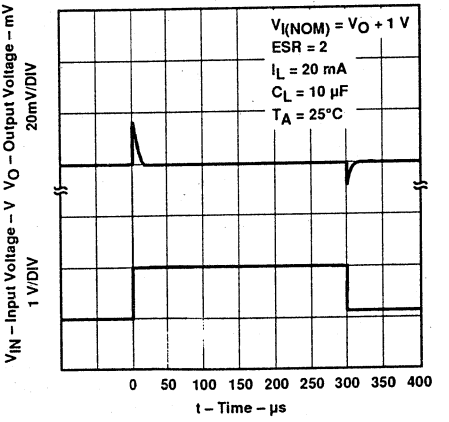
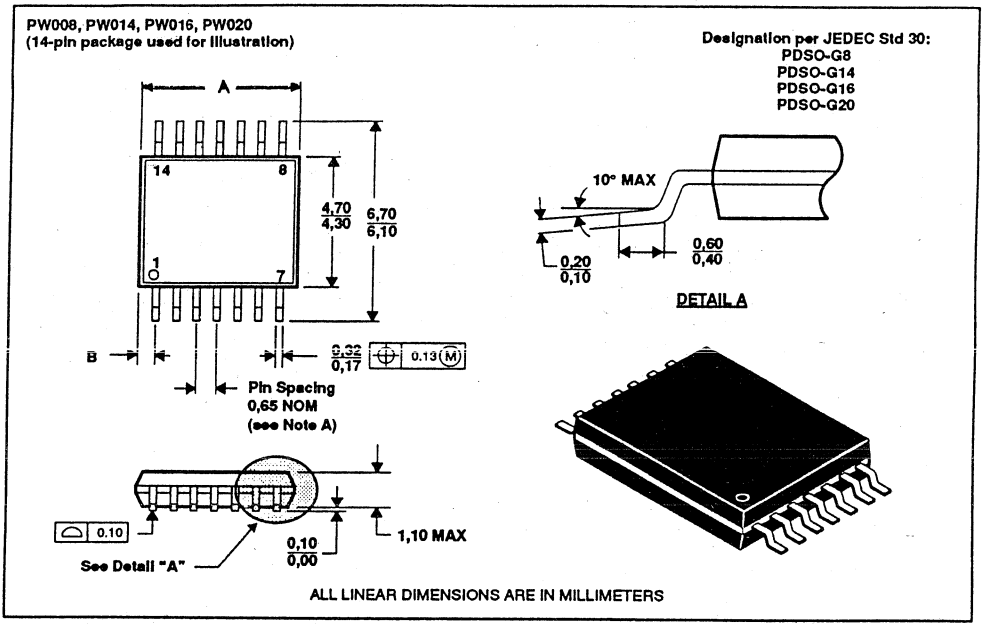


Figure 12

MECHANICAL DATA

PW008, PW014, PW016, PW020
shrink small-outline packages

These shrunk small-outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



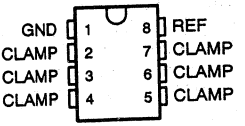
NOTES: A. Leads are within 0,25-mm radius of true position at maximum material condition.
B. Body dimensions include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 mm.
D. Lead tips to be planar within ±0,051 mm exclusive of solder.

DIM \ PINS	8	14	16	20
A MIN	2,99	4,99	4,99	6,40
A MAX	3,03	5,30	5,30	6,80
B MAX	0,65	0,70	0,38	0,48

SLAS078 – D4102, SEPTEMBER 1993

- **Protects Against Latch-Up**
- **25-mA Current Sink In Active State**
- **Less Than 1-mW Dissipation In Standby Condition**
- **Ideal for Applications In Environments Where Large Transient Spikes Occur**
- **Stable Operation for All Values of Capacitive Load**
- **No Output Overshoot**

D OR P PACKAGE
(TOP VIEW)



description

The TL7726C, TL7726I, and TL7726Q each consist of six identical clamping circuits that monitor an input voltage with respect to a reference value, REF. For an input voltage (V_I) in the range of GND to < REF, the clamping circuits present a very high impedance to ground, drawing current of less than 10 μA. The clamping circuits are active for V_I < GND or V_I > REF when they have a very low impedance and can sink up to 25 mA.

These characteristics make the TL7726C, TL7726I, and TL7726Q ideal as protection devices for CMOS semiconductor devices in environments where there are large positive or negative transients to protect analog-to-digital converters in automotive or industrial systems. The use of clamping circuits provides a safeguard against potential latch-up.

The TL7726C is characterized for operation over the temperature range of 0°C to 70°C. The TL7726I is characterized for operation over the temperature range of –25°C to 85°C. The TL7726Q is characterized for operation over the temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

OPERATING TEMPERATURE RANGE	DEVICE	PACKAGE
0°C – 70°C	TL7726CD	8-pin SO
0°C – 70°C	TL7726CP	8-pin DIP
–25°C – 85°C	TL7726ID	8-pin SO
–25°C – 85°C	TL7726IP	8-pin DIP
–40°C – 125°C	TL7726QD	8-pin SO
–40°C – 125°C	TL7726QP	8-pin DIP

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Reference voltage, V_{ref} ..... 6 V
Clamping current, I_{IK} ..... ±50 mA
Junction temperature, T_J ..... 150°C
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: TL7726C ..... 0°C to 70°C
TL7726I ..... −40°C to 85°C
TL7726Q ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A \le 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	728 mW	5.8 mW/°C	460 mW	374 mW	144 mW
P	924 mW	9.5 mW/°C	757 mW	615 mW	237 mW

recommended operating conditions

		MIN	MAX	UNIT
Reference voltage, V_{ref}		4.5	5.5	V
Input clamping current, I_{IK}	$V_I \ge V_{ref}$		25	mA
	$V_I \le GND$	−25		

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK+}	Positive clamp voltage	I_I = 20 mA	V_{ref}		V_{ref} + 200	mV
V_{IK-}	Negative clamp voltage	I_I = 20 mA	−200		0	mV
I_Z	Reference current	V_{ref} = 5 V		25	60	µA
I_I	Input current	V_{ref} − 50 mV ≤ $V_I \le V_{ref}$			10	µA
		GND ≤ V_I ≤ 50 mV	−10			µA
		50 mV ≤ $V_I \le V_{ref}$ − 50 mV	−1		1	µA

† All typical values are at T_A = 25°C.

switching characteristics specified at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_s	Settling time	V_I(system) = ±13 V, R_l = 600 Ω, t_t < 1 µs, Measured at 10% to 90%, See Figure 1		30	µs

PARAMETER MEASUREMENT INFORMATION

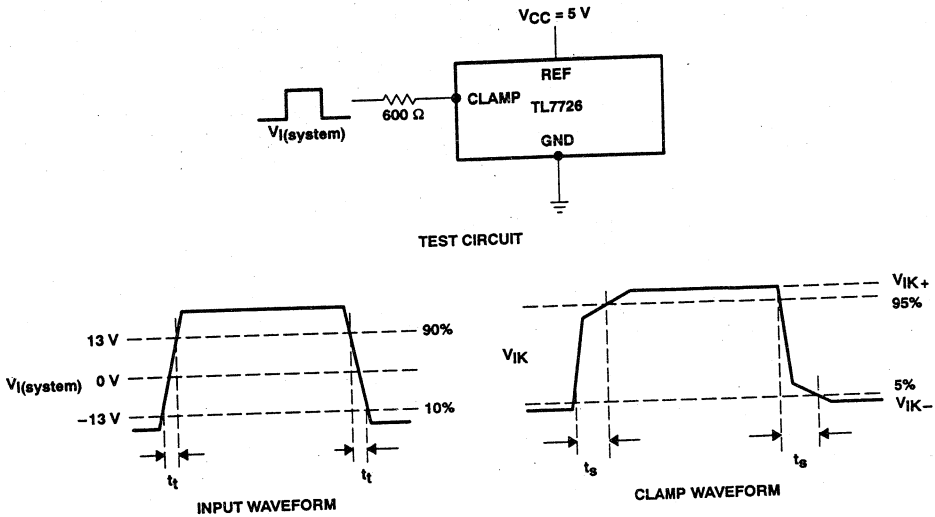


Figure 1. Switching Characteristics

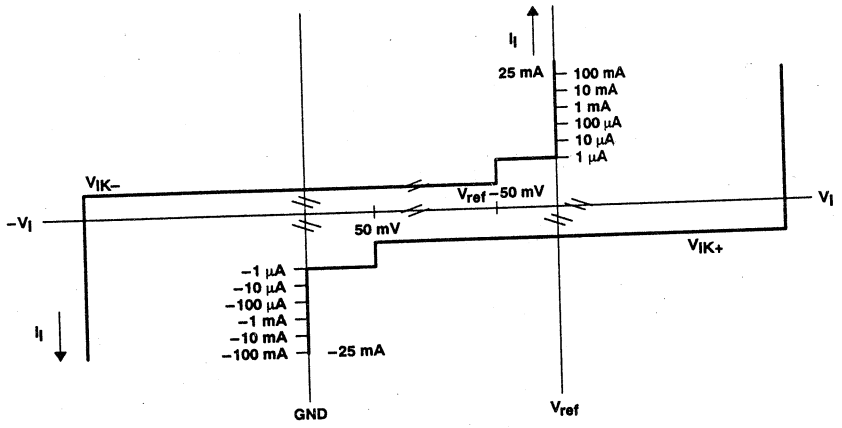
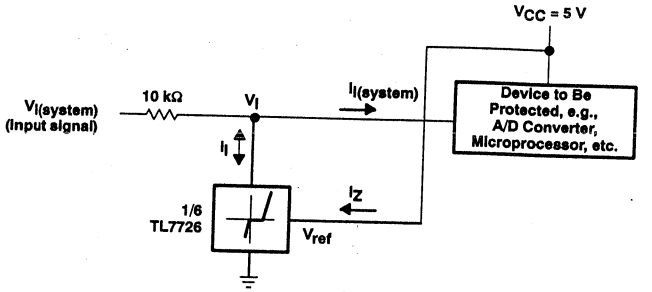


Figure 2. Tolerance Band for Clamping Circuit

APPLICATION INFORMATION



Example: If $I_I >> I_{I(system)}$, i.e., $V_{I(system)} > V_{ref}$ + 200 mV
where:

$I_{I(system)}$ = Input current to the device being protected
$V_{I(system)}$ = Input voltage to the device being protected
then the maximum input voltage

$$V_{I(system)max} = V_{ref} + I_I max(10k\Omega)$$
$$= 5\ V + 25\ mA(10k\Omega)$$
$$= 5\ V + 250\ V$$
$$= 255\ V$$

Figure 3. Typical Application

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Very Low Power . . . 35 μA Per Channel Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 850 μV Max at T_A = 25°C (TLC2252A)**
- **Macromodel Included**

description

The TLC2252 and TLC2252A are dual operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices exhibit rail-to-rail output performance while having better input offset voltage and lower power dissipation levels than existing CMOS operational amplifiers. In addition, the noise performance has been dramatically improved for this class of low-power CMOS amplifier. Figure 1 depicts the low level of voltage noise for this CMOS amplifier, which has only 35 μA (typical) of supply current per amplifier. Also, the common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ±5 mV. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

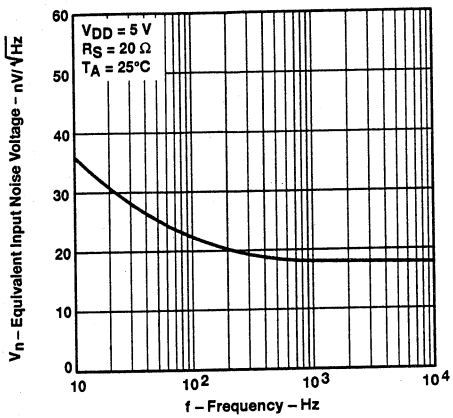


Figure 1

The TLC2252 and TLC2252A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the low-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to ADCs. All of these features, combined with its temperature performance, make the TLC2252 family ideal for sonobuoys, remote pressure sensors, temperature control, active VR sensors, accelerometers, portable medical applications, hand-held metering, and many other applications.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	1500 μV	TLC2252CD	TLC2252CP	TLC2252CPWLE	TLC2252Y
−40°C to 125°C	850 μV	TLC2252AID	TLC2252AIP	TLC2252AIPWLE	
	1500 μV	TLC2252ID	TLC2252IP	—	

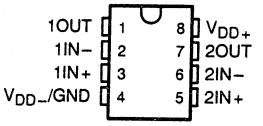
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2252CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

TEXAS INSTRUMENTS

description (continued)

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

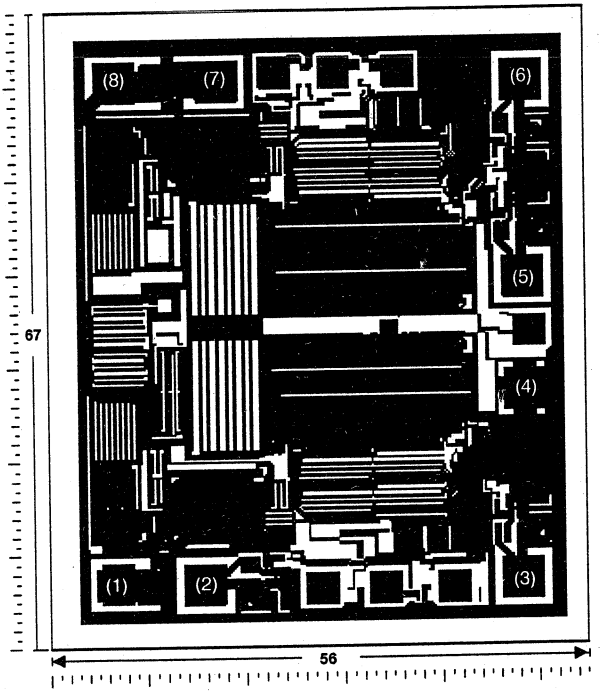
D, P, OR PW PACKAGE
(TOP VIEW)

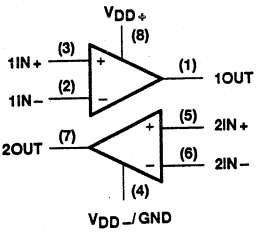


TLC2252Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2252C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

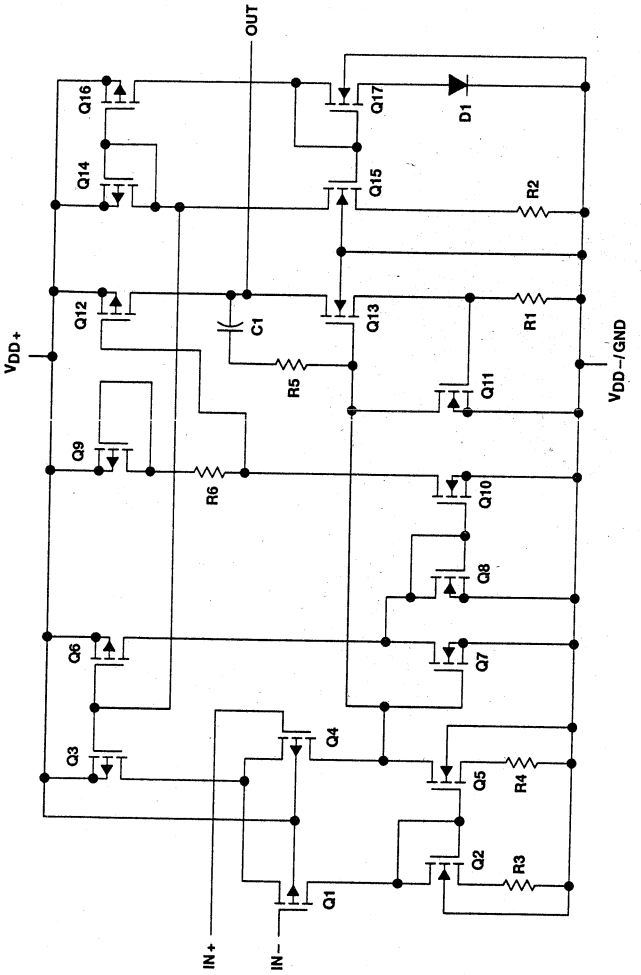
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	38
Diodes	9
Resistors	30
Capacitors	3

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1) ..... 8 V
Supply voltage, V_{DD-} (see Note 1) ..... −8 V
Differential input voltage, V_{ID} (see Note 2) ..... ±16 V
Input voltage, V_I (any input, see Note 1) ..... ±8 V
Input current, I_I (each input) ..... ±5 mA
Output current, I_O ..... ±50 mA
Total current into V_{DD+} ..... ±50 mA
Total current out of V_{DD-} ..... ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current flows if input is brought below V_{DD-} − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+}-1.5$	V_{DD-}	$V_{DD+}-1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-1.5$	V_{DD-}	$V_{DD+}-1.5$	V
Operating free-air temperature, T_A	0	70	−40	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2252C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±2.5 V, R_S = 50 Ω	25°C		200	1500	µV
				Full range			1750	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.98		V
		I_{OH} = −75 µA		25°C	4.9	4.94		
				Full range	4.8			
		I_{OH} = −150 µA		25°C	4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15	
				Full range			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3	
				Full range			0.3	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.7	1	
				Full range			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ‡	25°C	100	350		V/mV
				Full range	10			
			R_L = 1 MΩ‡	25°C		1700		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		70	125	µA
				Full range			125	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 100 kΩ‡,	25°C	0.07	0.12		V/μs
				Full range	0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36		nV/√Hz
		f = 1 kHz		25°C		19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%		
			A_V = 10			1%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°		
	Gain margin			25°C		15		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		T_A†	TLC2252C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		200	1500	µV
				Full range			1750	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω	25°C	−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.98		V
		I_O = −100 µA		25°C	4.9	4.93		
				Full range	4.7			
		I_O = −200 µA		25°C	4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0,	I_O = 50 µA	25°C		−4.99		V
		V_{IC} = 0,	I_O = 500 µA	25°C	−4.85	−4.91		
				Full range	−4.85			
		V_{IC} = 0,	I_O = 1 mA	25°C	−4.7	−4.8		
				Full range	−4.7			
		V_{IC} = 0,	I_O = 4 mA	25°C	−4	−4.3		
				Full range	−3.8			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 100 kΩ	25°C	45	650		V/mV
				Full range	10			
			R_L = 1 MΩ	25°C		3000		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		190		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0,	R_S = 50 Ω	25°C	75	88		dB
				Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = 2.2 V to ±8 V, V_{IC} = 0,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 0,	No load	25°C		80	125	µA
				Full range			125	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±1.9 V, C_L = 100 pF	R_L = 100 kΩ,	25°C	0.07	0.12		V/μs
				Full range	0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		38		nV/√Hz
		f = 1 kHz		25°C		19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion pulse duration	V_O = ±2.3 V, f = 10 kHz, R_L = 50 kΩ	A_V = 1	25°C		0.2%		
			A_V = 10			1%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.21		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		14		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		63°		
	Gain margin			25°C		15		dB

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		200	1500		200	850	µV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO}\rvert \le$ 5 mV		25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.98			4.98		V
		I_{OH} = −75 µA		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		I_{OH} = −150 µA		25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 µA		25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 µA		25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 4 mA		25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ‡	25°C	100	350		100	350		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		1700			1700		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		70	125		70	125	µA
				Full range			125			125	

† Full range is − 40°C to 125°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		200	1500		200	850	μV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$5 mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA		25°C		4.98			4.98		V
		I_O = −100 μA		25°C	4.9	4.93		4.9	4.93		
				Full range	4.7			4.7			
		I_O = −200 μA		25°C	4.8	4.86		4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0,	I_O = 50 μA	25°C		−4.99			−4.99		V
		V_{IC} = 0,	I_O = 500 μA	25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0,	I_O = 4 mA	25°C	−4	−4.3		−4	−4.3		
				Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 50 kΩ	25°C	40	150		40	150		V/mV
				Full range	10			10			
			R_L = 1 MΩ	25°C		3000			3000		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		190			190		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0,	R_S = 50 Ω	25°C	75	88		75	88		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load		25°C		80	125		80	125	μA
				Full range			125			125	

† Full range is − 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±1.9 V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		38			38		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 50 kΩ, f = 10 kHz	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.21			0.21		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		14			14		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is −40°C to 125°C.

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2252Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω		200	1500	μV
I_{IO}	Input offset current				0.5	100	pA
I_{IB}	Input bias current				1	100	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω	0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA			4.98		V
		I_{OH} = −75 μA		4.9	4.94		
		I_{OH} = −150 μA		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA		0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA		0.8	1	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ†	100	350		V/mV
			R_L = 1 MΩ†		1700		
r_{id}	Differential input resistance				10^{12}		Ω
r_{ic}	Common-mode input resistance				10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10		200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V,	V_O = 2.5 V, R_S = 50 Ω	70	83		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V,	V_{IC} = V_{DD}/2, No load	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		70	125	μA

† Referenced to 2.5 V

TEXAS INSTRUMENTS

electrical characteristics at $V_{DD\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLC2252Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	V_O = 0,	R_S = 50 Ω		200	1500	μV
I_{IO}	Input offset current					0.5	100	pA
I_{IB}	Input bias current					1	100	pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert \le$ 5 mV,	R_S = 50 Ω		−5 to 4	−5.3 to 4.2		V
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA				4.99		V
		I_O = −100 μA			4.9	4.93		
		I_O = −200 μA			4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0,	I_{OL} = 50 μA			−4.99		V
		V_{IC} = 0,	I_{OL} = 500 μA		−4.85	−4.91		
		V_{IC} = 0,	I_{OL} = 4 mA		−3.8	−4.1		
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 100 kΩ		40	150		V/mV
			R_L = 1 MΩ			3000		
r_{id}	Differential input resistance					10^{12}		Ω
r_{ic}	Common-mode input resistance					10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10			190		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V,	V_O = 0,	R_S = 50 Ω	75	88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V,	V_{IC} = 0,	No load	80	95		dB
I_{DD}	Supply current	V_O = 0,	No load			80	125	μA

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

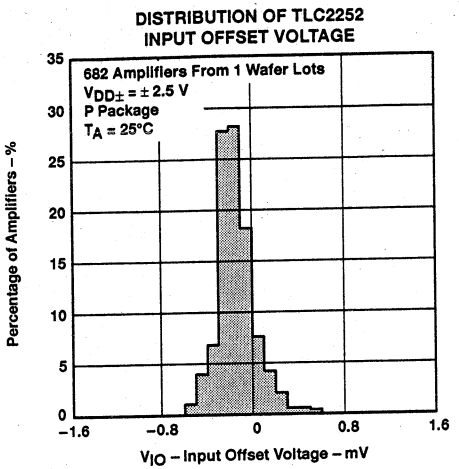


Figure 2

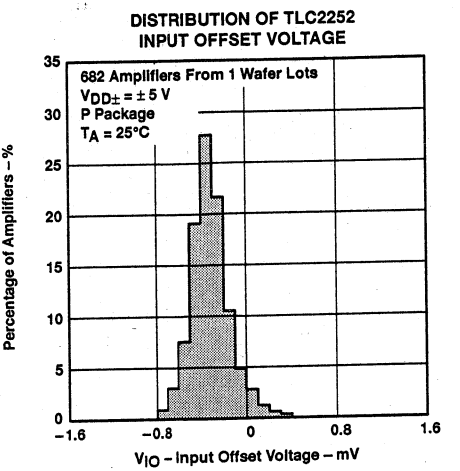
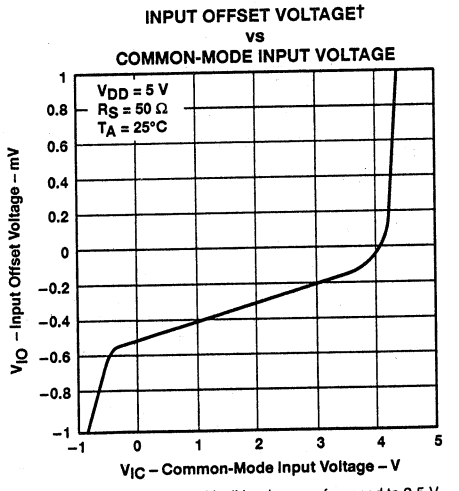


Figure 3



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 4

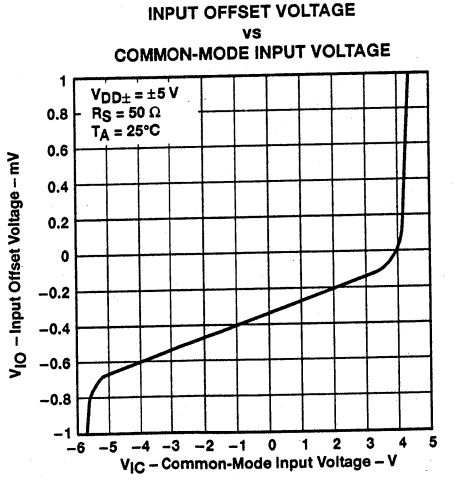


Figure 5

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC2252 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

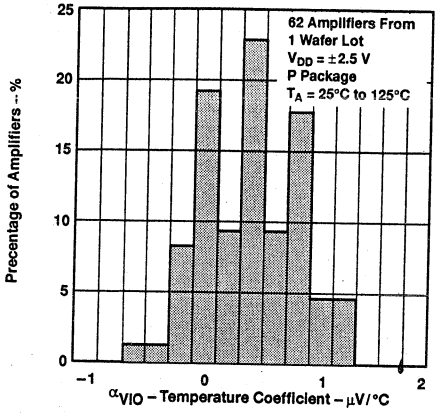


Figure 6

DISTRIBUTION OF TLC2252 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

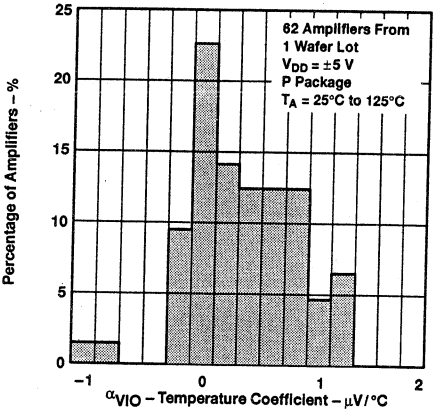


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

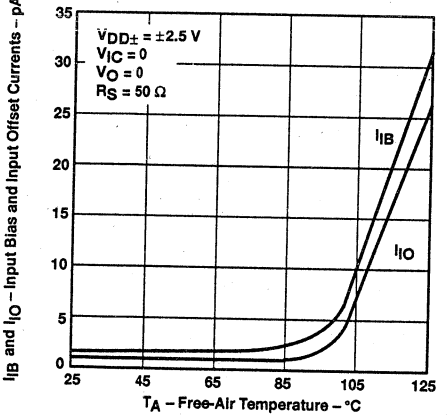


Figure 8

INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

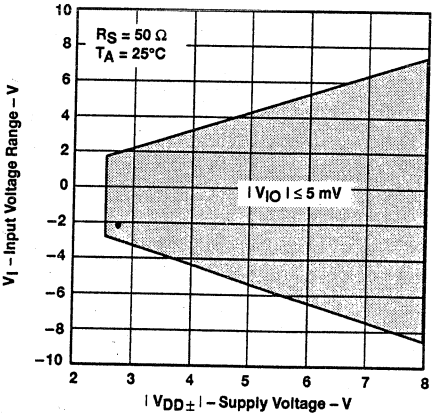


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS†‡

INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

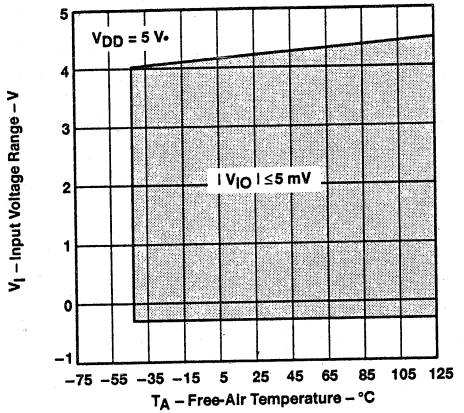


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

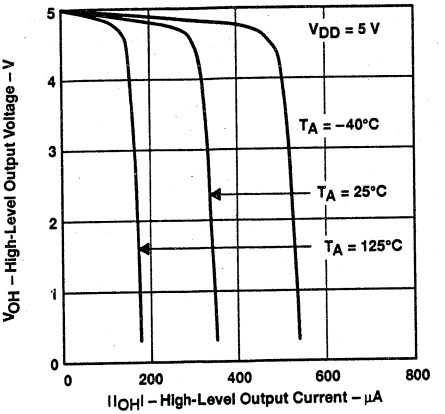


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

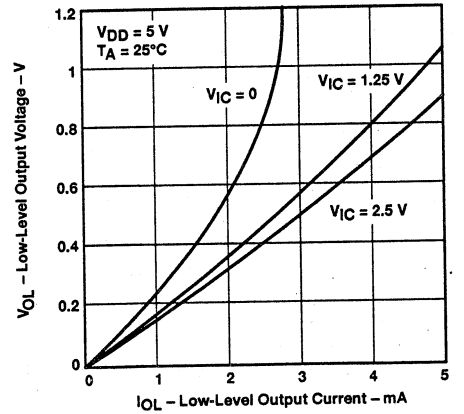


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

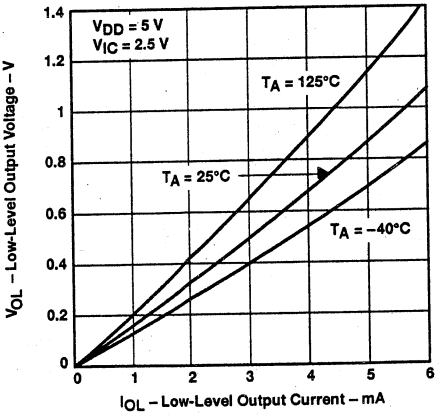


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

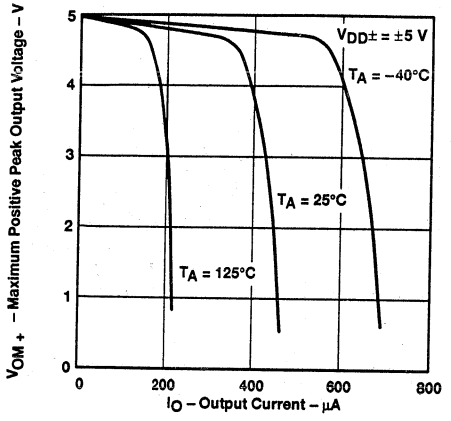


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

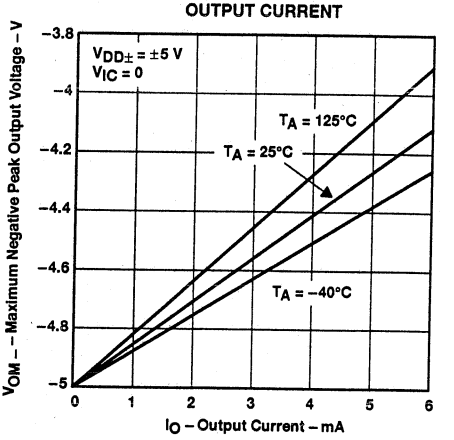
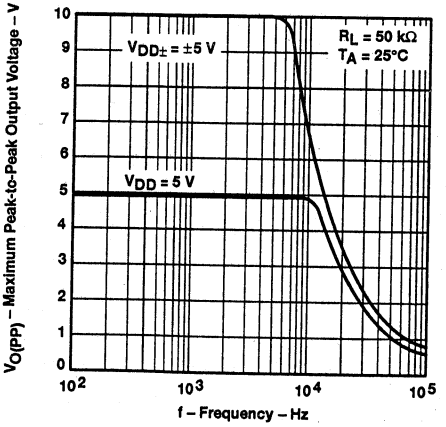


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE†
vs
FREQUENCY



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 16

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

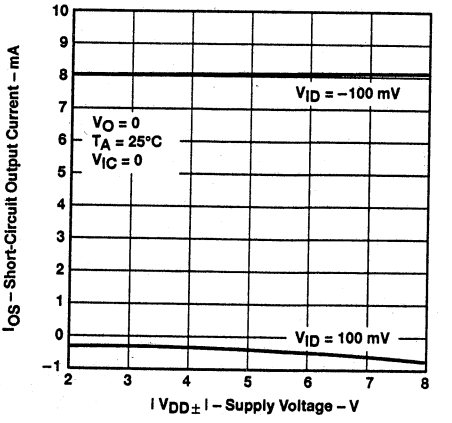


Figure 17

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

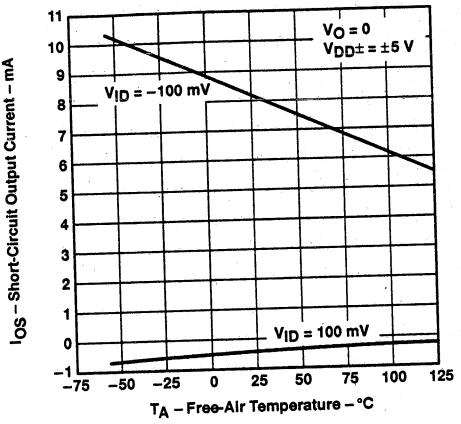


Figure 18

OUTPUT VOLTAGE‡
vs
DIFFERENTIAL INPUT VOLTAGE

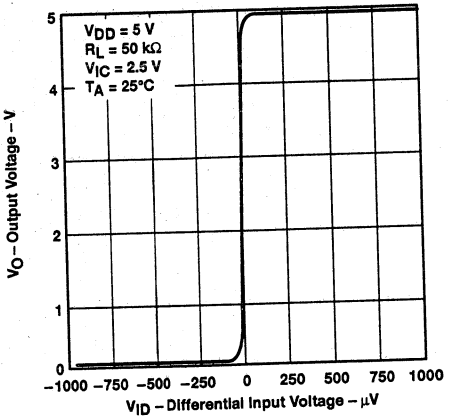


Figure 19

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

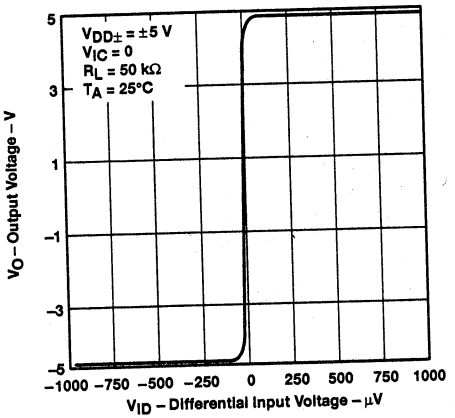


Figure 20

DIFFERENTIAL GAIN‡
vs
LOAD RESISTANCE

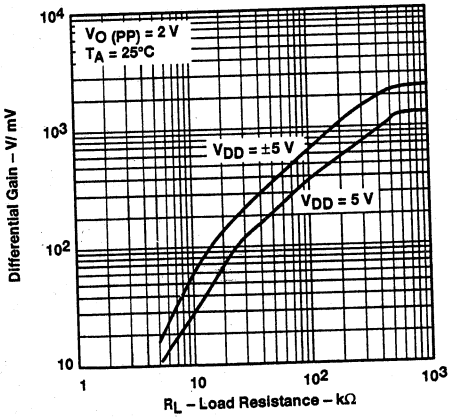
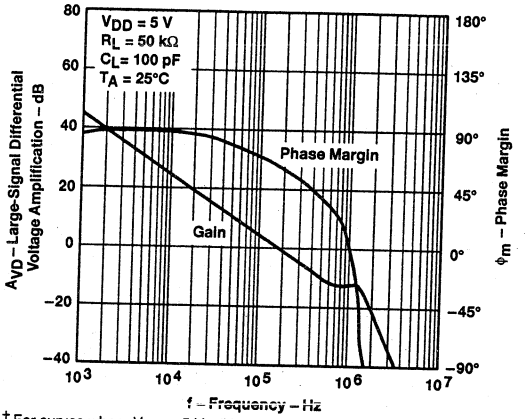


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN vs FREQUENCY



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

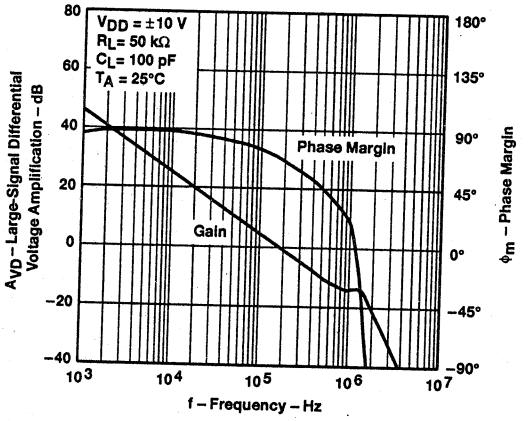


Figure 23

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL‡
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

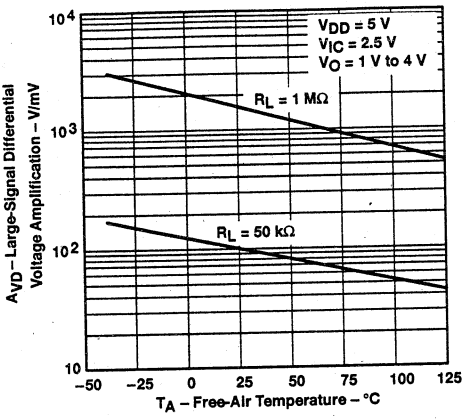


Figure 24

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

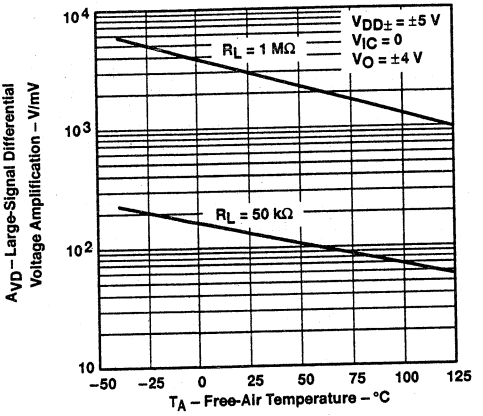


Figure 25

OUTPUT IMPEDANCE‡
vs
FREQUENCY

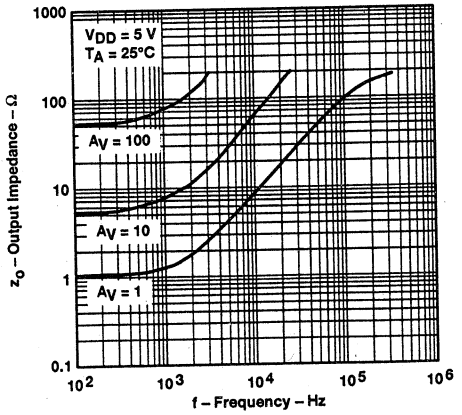


Figure 26

OUTPUT IMPEDANCE
vs
FREQUENCY

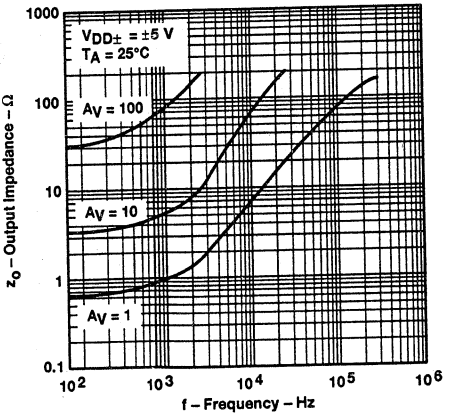


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO‡ vs FREQUENCY

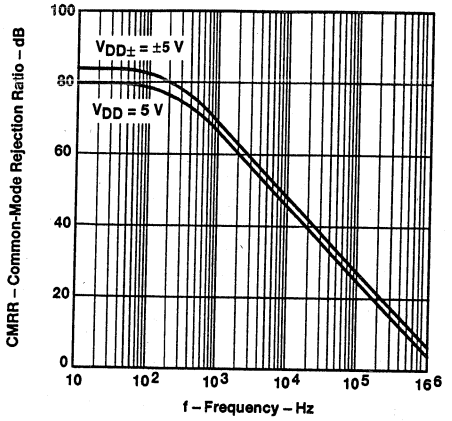


Figure 28

COMMON-MODE REJECTION RATIO‡ vs FREE-AIR TEMPERATURE

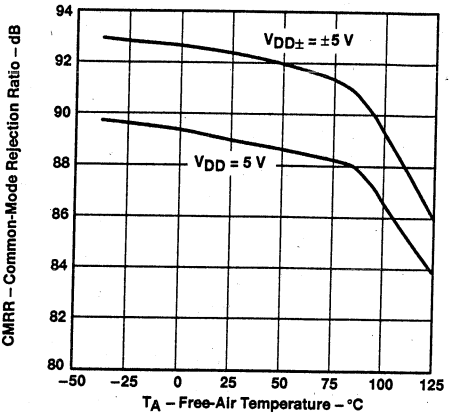


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO‡ vs FREQUENCY

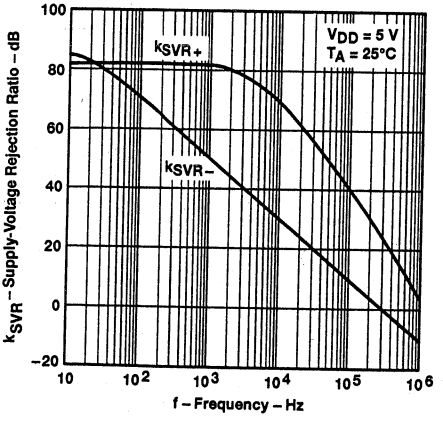


Figure 30

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

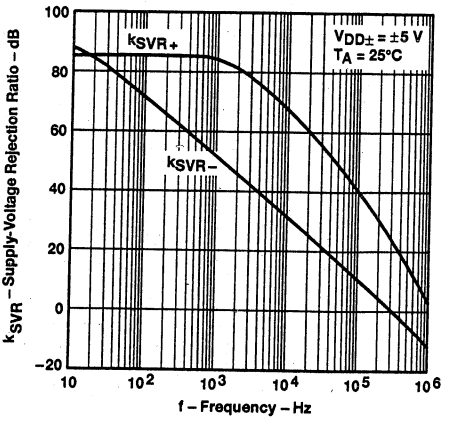


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

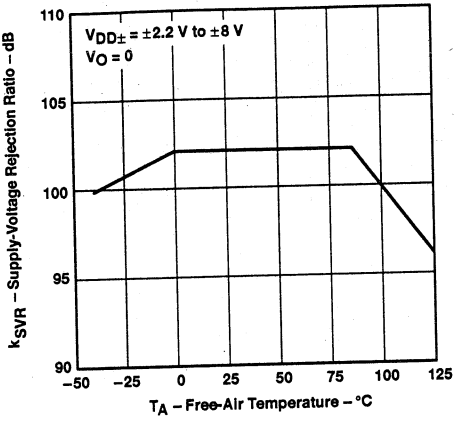


Figure 32

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

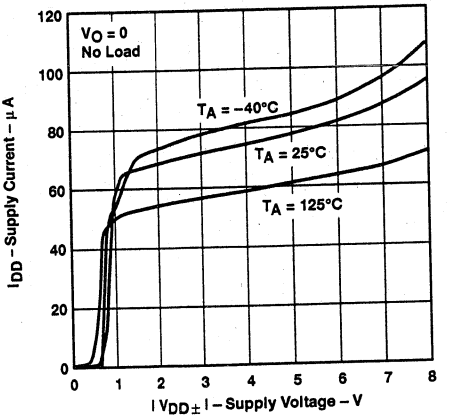


Figure 33

SUPPLY CURRENT‡
vs
FREE-AIR TEMPERATURE

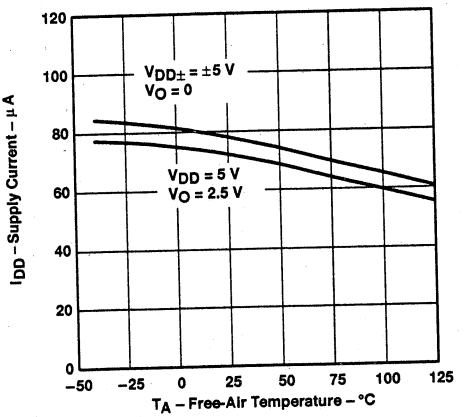


Figure 34

SLEW RATE‡
vs
LOAD CAPACITANCE

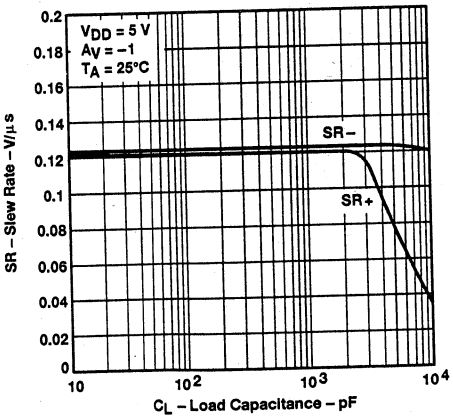


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS†

SLEW RATE‡
vs
FREE-AIR TEMPERATURE

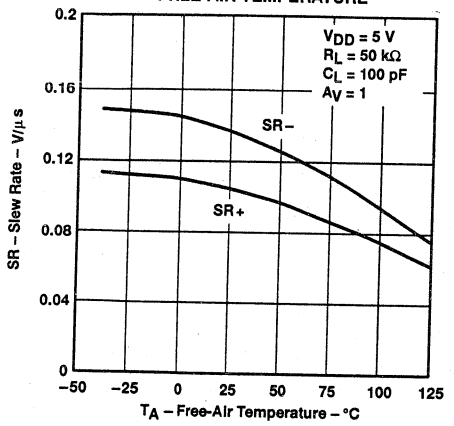


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE‡

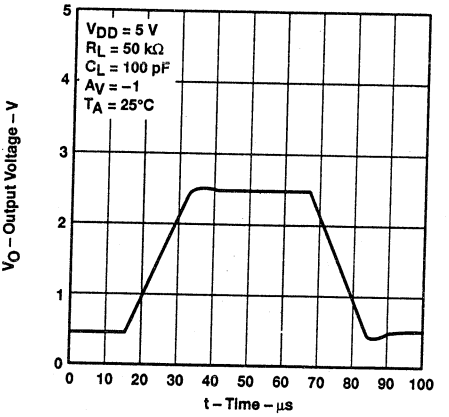


Figure 37

INVERTING LARGE-SIGNAL PULSE RESPONSE

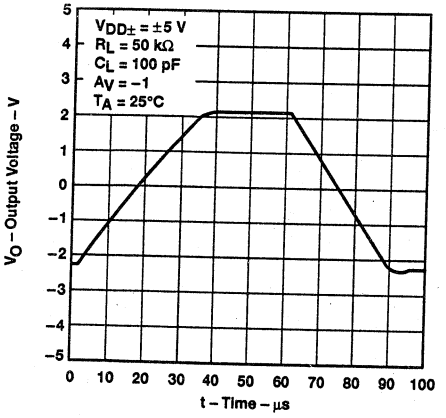


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE‡

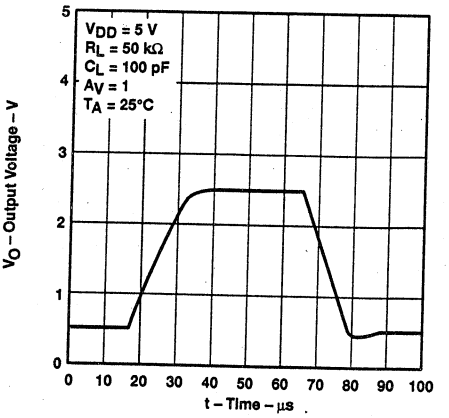


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

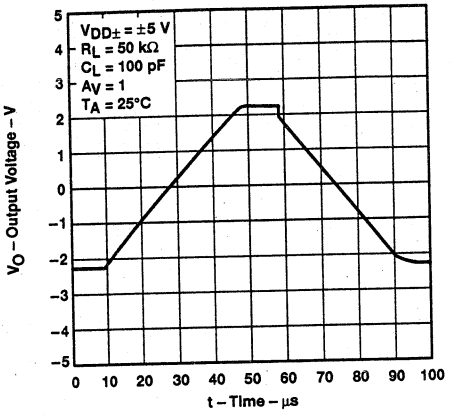


Figure 40

INVERTING SMALL-SIGNAL PULSE RESPONSE†

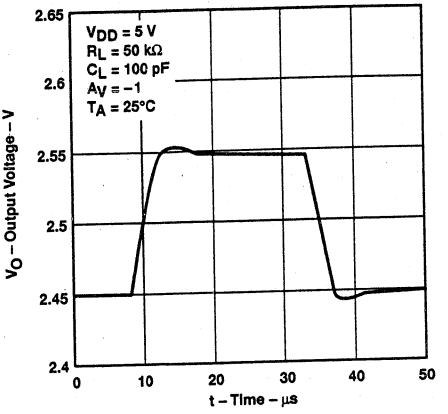


Figure 41

INVERTING SMALL-SIGNAL PULSE RESPONSE

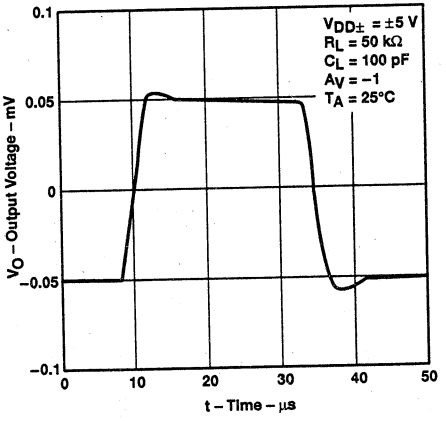


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

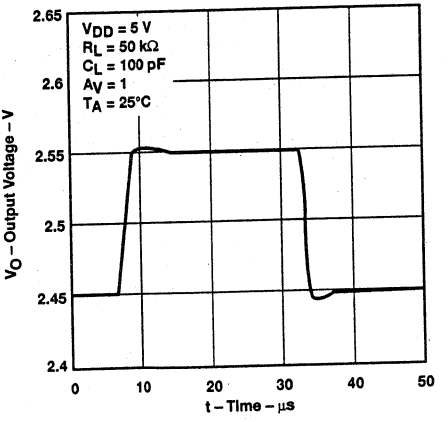


Figure 43

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

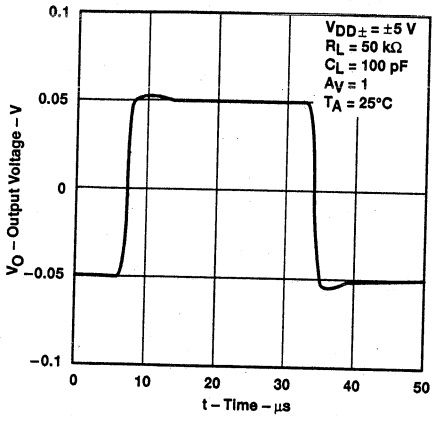


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE† vs FREQUENCY

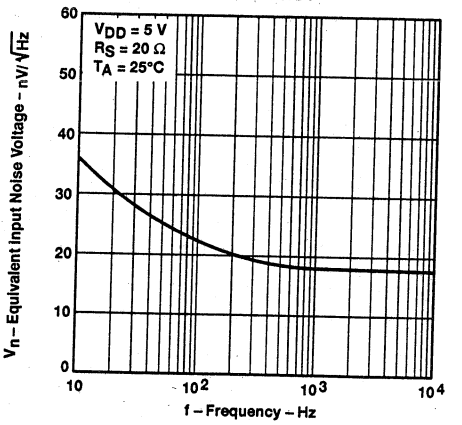


Figure 45

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

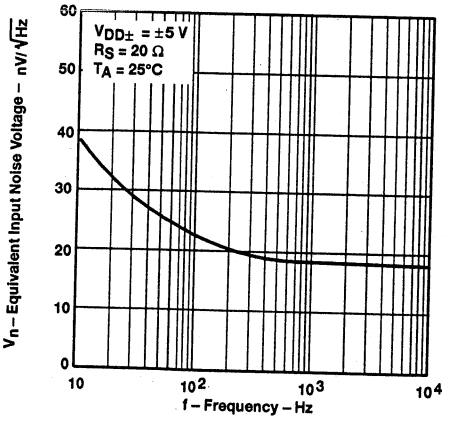


Figure 46

EQUIVALENT INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD†

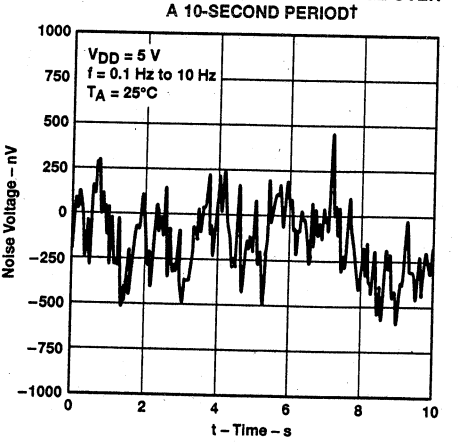


Figure 47

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS†

INTEGRATED NOISE VOLTAGE
vs
FREQUENCY

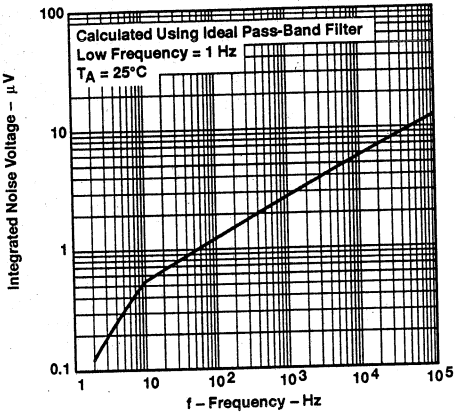


Figure 48

TOTAL HARMONIC DISTORTION PLUS NOISE‡
vs
FREQUENCY

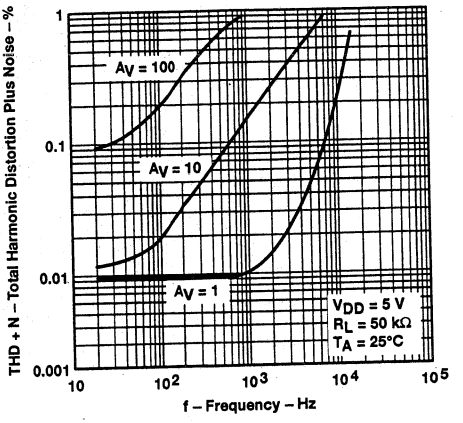


Figure 49

GAIN-BANDWIDTH PRODUCT‡
vs
FREE-AIR TEMPERATURE

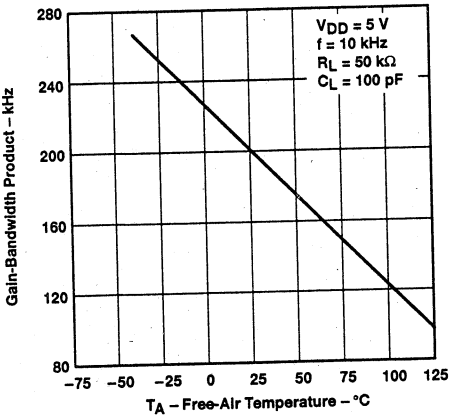


Figure 50

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

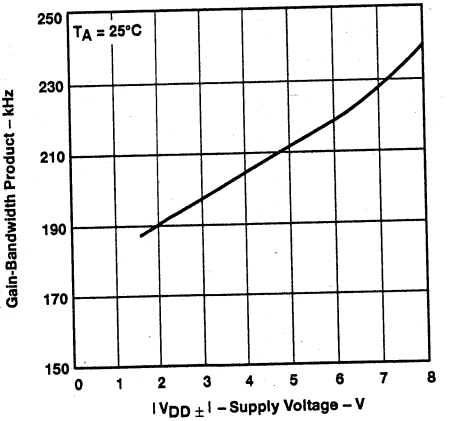


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

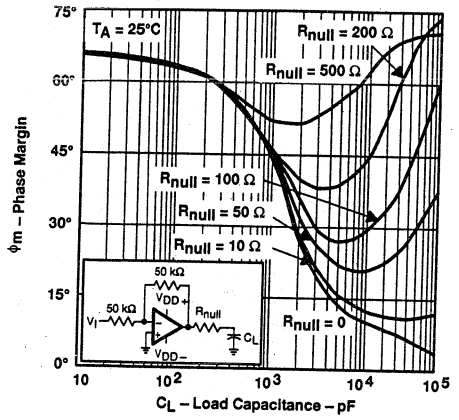


Figure 52

GAIN MARGIN
vs
LOAD CAPACITANCE

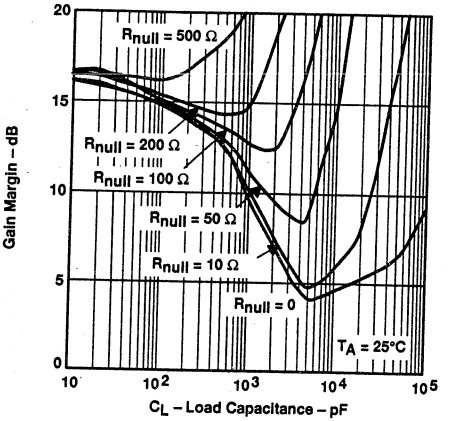


Figure 53

UNITY-GAIN BANDWIDTH†
vs
LOAD CAPACITANCE

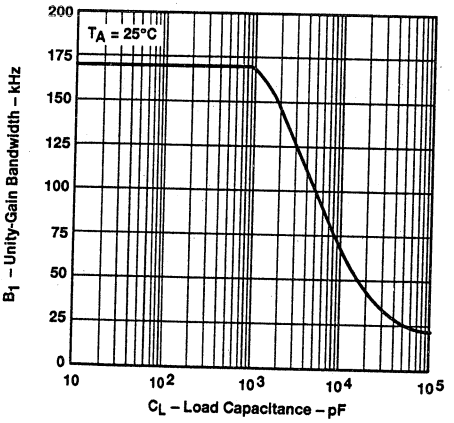


Figure 54

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE

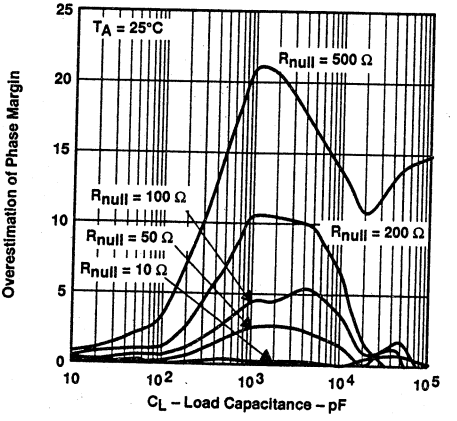


Figure 55

† See application information

TEXAS INSTRUMENTS

APPLICATION INFORMATION

driving large capacitive loads

The TLC2252 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 52 and Figure 53 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 56) improves the gain and phase margins when driving large capacitive loads. Figure 52 and Figure 53 show the effects of adding series resistances of 10 Ω, 50 Ω, 100 Ω, 200 Ω, and 500 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L\right) \quad (1)$$

where :

$\Delta\phi_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 54). To use equation (1), UGBW must be approximated from Figure 54.

Using equation (1) alone overestimates the improvement in phase margin, as illustrated in Figure 55. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 56, with equation (1) enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

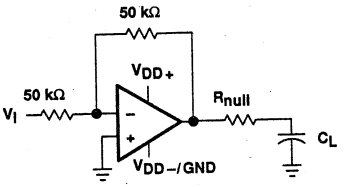


Figure 56. Series-Resistance Circuit

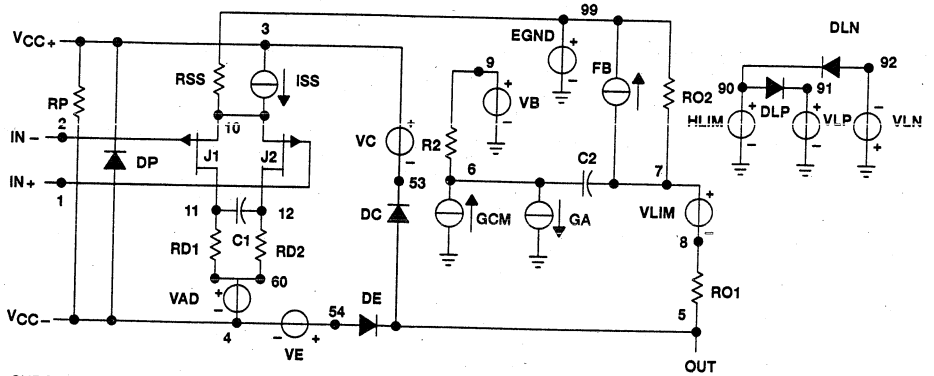
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 57 are generated using the TLC2252 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLC2252 1 2 3 4 5
C1      11    12    6.369E-12
C2      6     7     25.00E-12
DC      5     53    DX
DE      54    5     DX
DLP     90    91    DX
DLN     92    90    DX
DP      4     3     DX
EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
FB      7     99    POLY (5) VB VC VE VLP
+ VLN 0 57.62E6 –60E6 60E6 60E6 –60E6
GA      6     0     11    12 26.86E–6
GCM     0     6     10    99 2.686E–9
ISS     3     10    DC 3.1E–6
HLIM    90    0     VLIM 1K
J1      11    2     10 JX
J2      12    1     10 JX
R2      6     9     100.0E3
RD1     60    11    37.23E3
RD2     60    12    37.23E3
RO1     8     5     84
RO2     7     99    84
RP      3     4     71.43E3
RSS     10    99    64.52E6
VAD     60    4     –.5
VB      9     0     DC 0
VC      3     53    DC .605
VE      54    4     DC .605
VLIM    7     8     DC 0
VLP     91    0     DC –.235
VLN     0     92    DC 7.5
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=139E–6
+ VTO=–.05)
.ENDS
```

Figure 57. Boyle Macromodel and Subcircuit

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TEXAS INSTRUMENTS

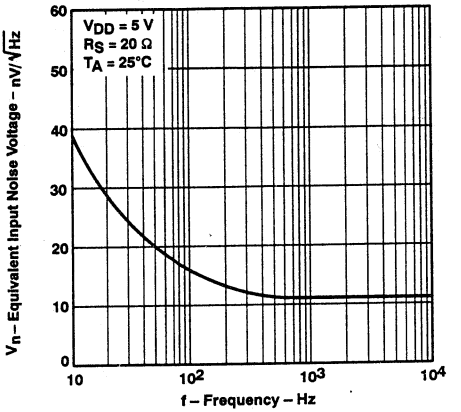
available features

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 500 μA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C (TLC2262A)**
- **Macromodel Included**

description

The TLC2262 and TLC2262A are dual operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices exhibit rail-to-rail output performance while having better input offset voltage and lower power dissipation levels than existing CMOS operational amplifiers. In addition, the noise performance has been dramatically increased for this class of low power CMOS amplifier. The graph at the right depicts the low level of voltage noise for this CMOS amplifier, which has only 200 μA (typical) of supply current per amplifier. Also, the common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ±5 mV. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input impedance levels that meet or exceed levels offered by topgate JFET and expensive dielectric-isolated devices.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



The TLC2262 and TLC2262A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the low power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to ADCs. All of these features, combined with its temperature performance, make the TLC2262 family ideal for sonobuoys, remote pressure sensors, temperature control, active VR sensors, accelerometers, portable medical applications, hand-held metering, and many other applications.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	2.5 mV	TLC2262CD	TLC2262CP	TLC2262CPWLE	TLC2262Y
−40°C to 125°C	950 μV	TLC2262AID	TLC2262AIP	TLC2262AIPWLE	
	2.5 mV	TLC2262ID	TLC2262IP	—	

The D packages are available taped and reeled. Add R suffix to device type, (e.g., TLC2262CDR).
The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

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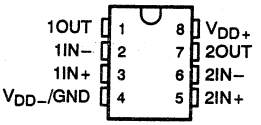
TEXAS INSTRUMENTS

description (continued)

The device inputs and outputs are designed to withstand 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply line transients under powered conditions. Transients of greater than 20 V can trigger the ESD protection structure inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

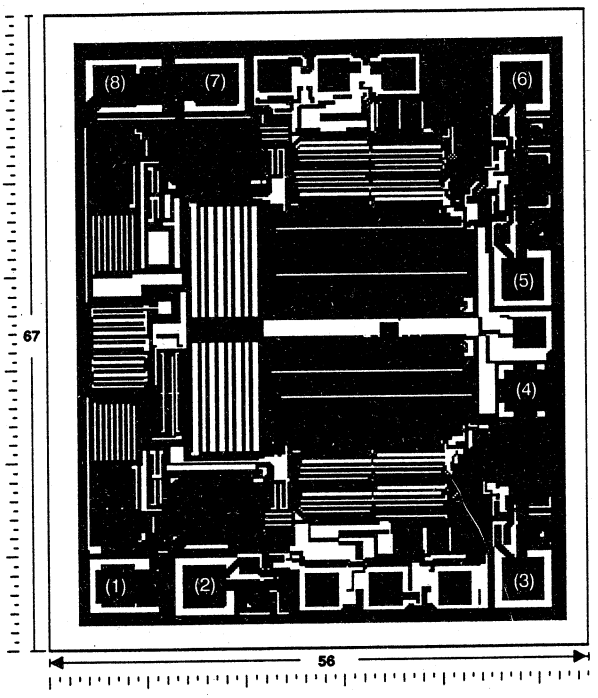
D, P, OR PW PACKAGE
(TOP VIEW)

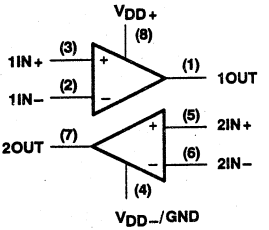


chip information

This chip, when properly assembled, displays characteristics similar to the TLC2262. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

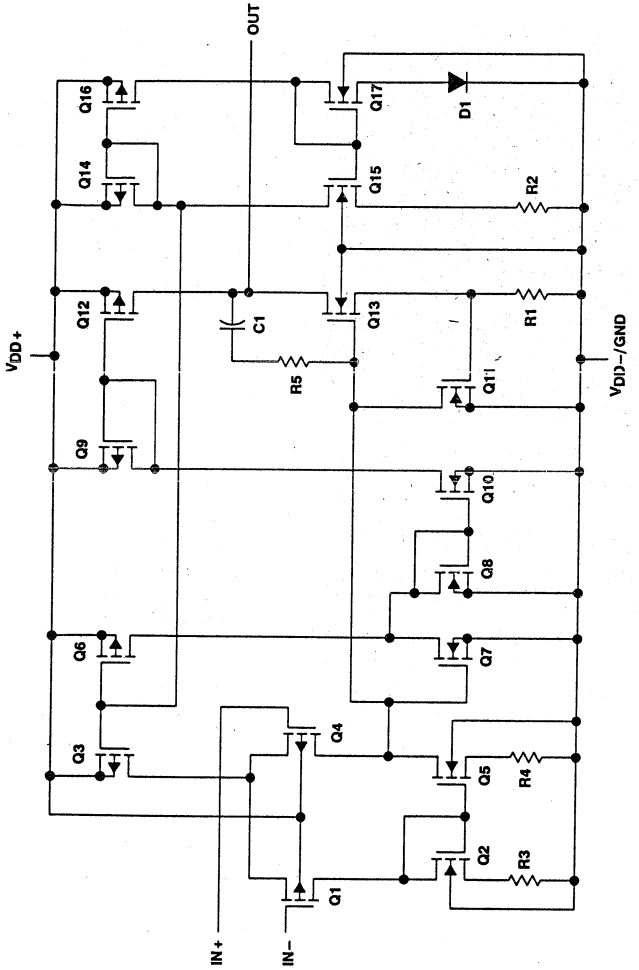
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	38
Diodes	9
Resistors	26
Capacitors	3

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) ..... 8 V
Supply voltage, V_{DD-} (see Note 1) ..... −8 V
Differential input voltage, V_{ID} (see Note 2) ..... ±16 V
Input voltage range, V_I (any input, see Note 1) ..... ±8 V
Input current, I_I (each input) ..... ±5 mA
Output current, I_O ..... ±50 mA
Total current into V_{DD+} ..... ±50 mA
Total current out of V_{DD-} ..... ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix ..... 0°C to 70°C
I-suffix ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+}-1.5$	V_{DD-}	$V_{DD+}-1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-1.5$	V_{DD-}	$V_{DD+}-1.5$	V
Operating free-air temperature, T_A	0	70	−40	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±2.5 V, R_S = 50 Ω	25°C		300	2500	μV
				Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\| \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		
				Full range	4.82			
		I_{OH} = −200 μA		25°C	4.70	4.85		
				Full range	4.60			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15	
				Full range			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3	
				Full range			0.3	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.7	1	
				Full range			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		V/mV
				Full range	55			
			R_L = 1 MΩ‡	25°C		550		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, No load,	V_{IC} = V_{DD}/2	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		400	500	μA
				Full range			500	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 1 V to 3.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C	0.35	0.55		V/μs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%		
			A_V = 10			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.82		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		205		kHz
	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4		μs
			To 0.01%			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		49°		
	Gain margin			25°C		11		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500	µV
				Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\| \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.99		V
		I_O = −100 µA		25°C	4.85	4.94		
				Full range	4.82			
		I_O = −200 µA		25°C	4.7	4.85		
				Full range	4.6			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0,	I_O = 50 µA	25°C		−4.99		V
		V_{IC} = 0,	I_O = 500 µA	25°C	−4.85	−4.91		
				Full range	−4.85			
		V_{IC} = 0,	I_O = 1 mA	25°C	−4.7	−4.8		
				Full range	−4.7			
		V_{IC} = 0,	I_O = 4 mA	25°C	−4	−4.3		
				Full range	−3.8			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 50 kΩ	25°C	80	200		V/mV
				Full range	55			
			R_L = 1 MΩ	25°C		1000		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		25°C	75	88		dB
				Full range	75			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = 2.2 V to ±8 V, No load, V_{IC} = 0		25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 0 V, No load		25°C		425	500	µA
				Full range			500	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±1.9 V, C_L = 100 pF, R_L = 50 kΩ,		25°C	0.35	0.55		V/μs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion pulse duration	V_O = ±2.3 V, f = 20 kHz, R_L = 50 kΩ	A_V = 1	25°C		0.014%		
			A_V = 10			0.024%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF, R_L = 50 kΩ,		25°C		0.86		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		210		kHz
	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1		μs
			To 0.01%			16.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		51°		
	Gain margin			25°C		12		dB

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262I			TLC2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0, V_{IC} = 0, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO}\rvert \le$ 5 mV		25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −200 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	100		80	170		V/mV
				Full range	50			50			
			R_L = 1 MΩ‡	25°C		150			550		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 4.4 V to 16 V, No load,	V_{IC} = V_{DD}/2	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		400	500		400	500	μA
				Full range			500			500	

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262I			TLC2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3.5 V, R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.82			0.82		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		205			205		kHz
	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
¢m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		49°			49°		
	Gain margin			25°C		11			11		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262I			TLC2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\|$ ≤5 mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA		25°C		4.99			4.99		V
		I_O = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_O = −200 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 μA		25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 μA		25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0, I_O = 4 mA		25°C	−4	−4.3		−4	−4.3		
				Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 50 kΩ	25°C	80	200		80	200		V/mV
				Full range	50			50			
			R_L = 1 MΩ	25°C		1000			1000		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	75	88		75	88		dB
				Full range	75			75			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, No load, V_{IC} = V_{DD}/2		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load		25°C		425	500		425	500	μA
				Full range			500			500	

† Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262I			TLC2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±1.9 V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 50 kΩ, f = 20 kHz	A_V = 1	25°C		0.014%			0.014%		
			A_V = 10			0.024%			0.024%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.86			0.86		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		210			210		kHz
	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1			7.1		μs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		51°			51°		
	Gain margin			25°C		12			12		dB

† Full range is −40°C to 125°C.

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω		300	2500	μV
I_{IO}	Input offset current				0.5	100	pA
I_{IB}	Input bias current				1	100	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω	0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA			4.99		V
		I_{OH} = −100 μA		4.85	4.94		
		I_{OH} = −200 μA		4.7	4.85		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA		0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA		0.8	1	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ†	80	170		V/mV
			R_L = 1 MΩ†		550		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V,	V_O = 2.5 V, R_S = 50 Ω	70	83		dB
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V,	No load, V_{IC} = V_{DD}/2	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		400	500	μA

† Referenced to 2.5 V

electrical characteristics at $V_{DD\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,			300	2500	μV
I_{IO}	Input offset current					0.5	100	pA
I_{IB}	Input bias current					1	100	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω		−5 to 4	−5.3 to 4.2		V
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA				4.99		V
		I_O = −100 μA			4.85	4.94		
		I_O = −200 μA			4.7	4.85		
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0,	I_{OL} = 50 μA			−4.99		V
		V_{IC} = 0,	I_{OL} = 500 μA		−4.85	−4.91		
		V_{IC} = 0,	I_{OL} = 4 mA		−3.8	−4.1		
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 50 kΩ		80	200		V/mV
			R_L = 1 MΩ			1000		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V,	V_O = 0,	R_S = 50 Ω	75	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±2.2 V to ±8 V,	No load,	V_{IC} = 0	80	95		dB
I_{DD}	Supply current	V_O = 0,	No load			425	500	μA

TYPICAL CHARACTERISTICS

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NOTE For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2262
INPUT OFFSET VOLTAGE

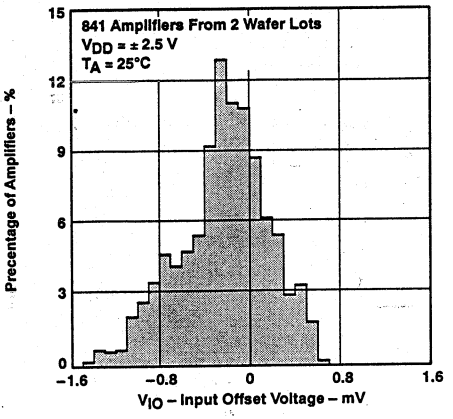


Figure 1

DISTRIBUTION OF TLC2262
INPUT OFFSET VOLTAGE

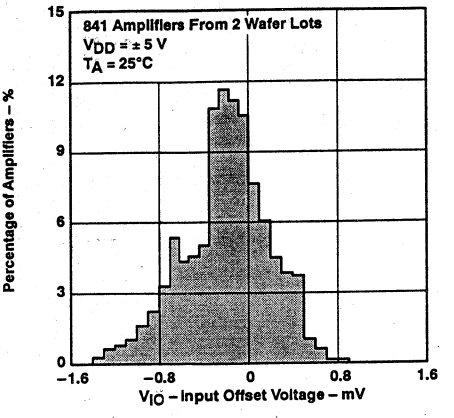


Figure 2

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

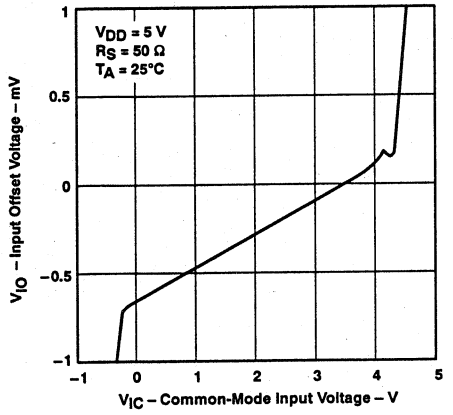


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

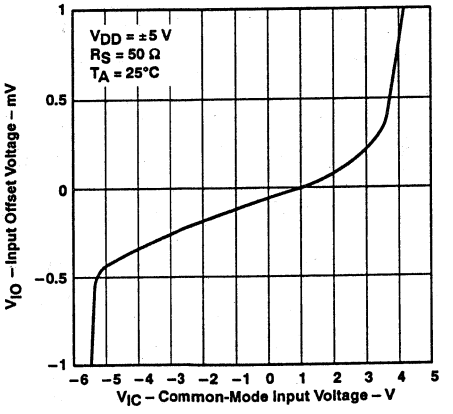


Figure 4

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

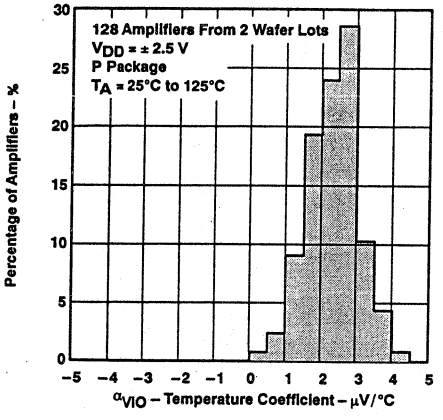


Figure 5

DISTRIBUTION OF TLC2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

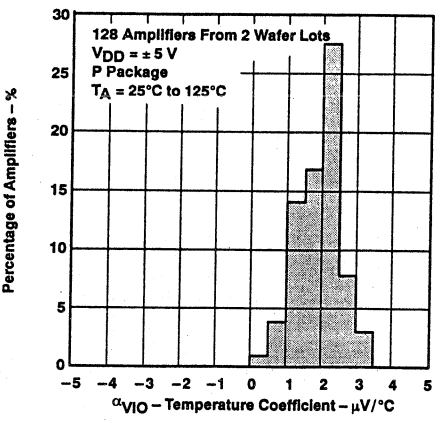


Figure 6

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

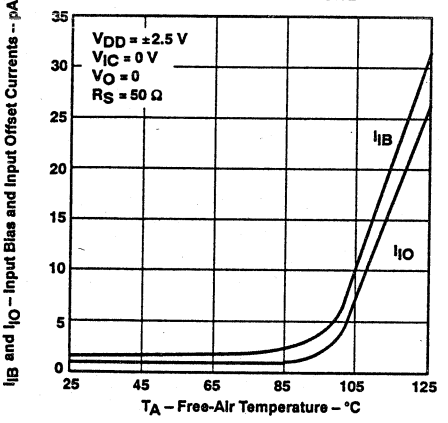


Figure 7

INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

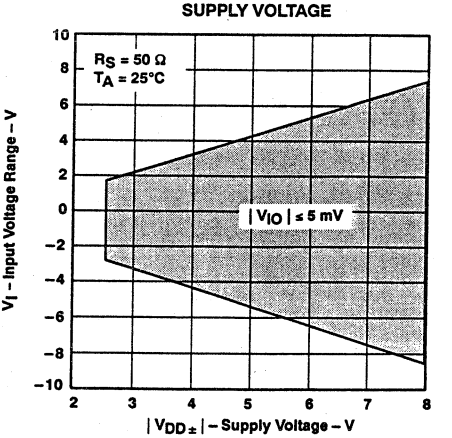


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

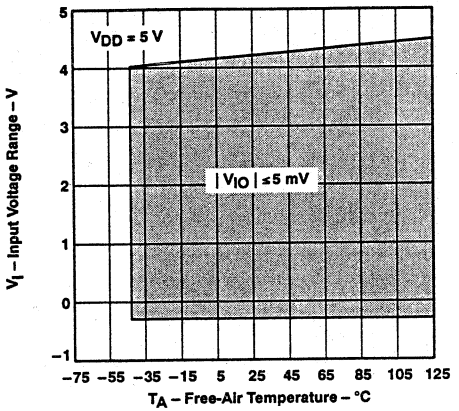


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

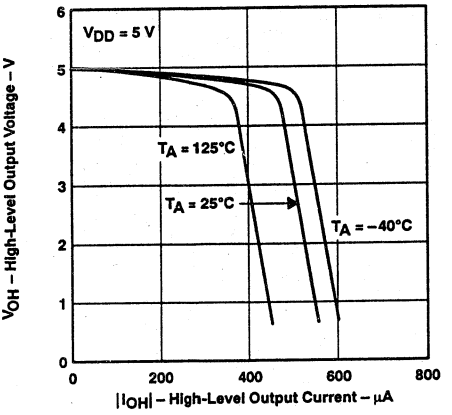


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

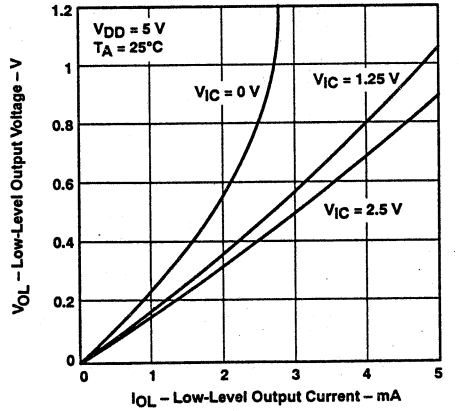


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

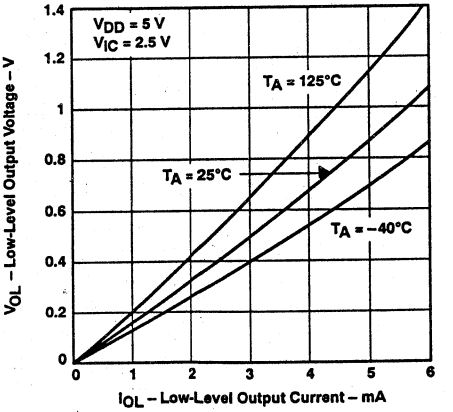


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE OUTPUT VOLTAGE
vs
OUTPUT CURRENT

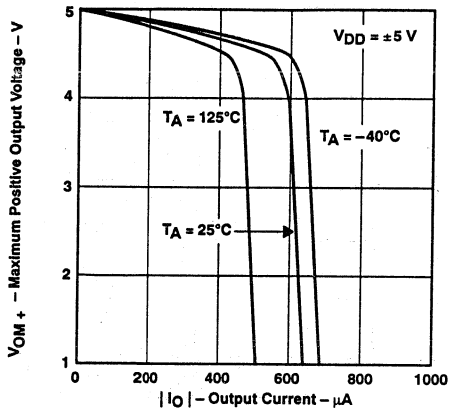


Figure 13

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

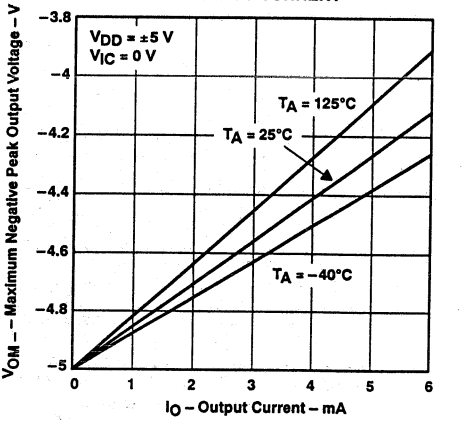


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

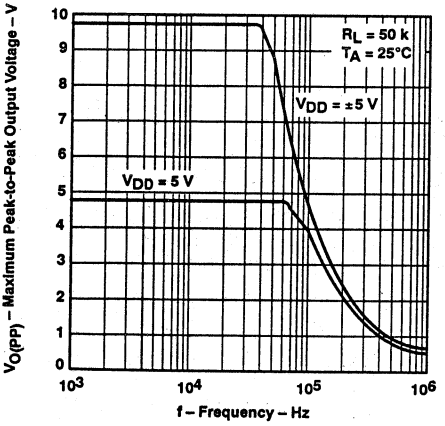


Figure 15

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

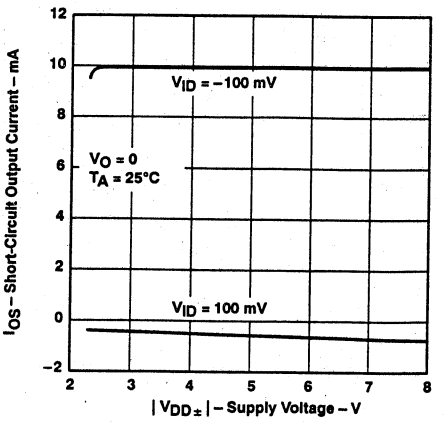


Figure 16

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

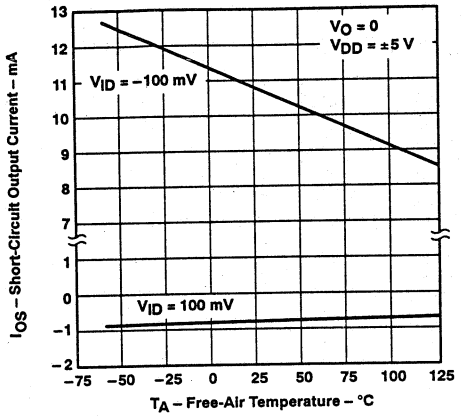


Figure 17

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

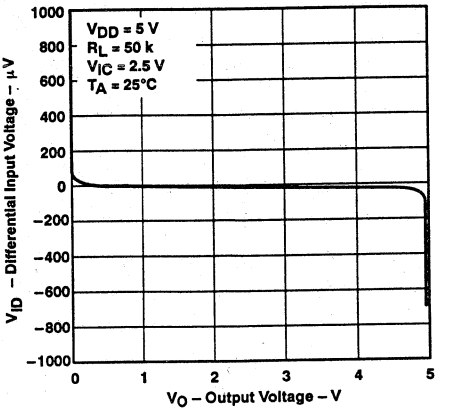


Figure 18

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

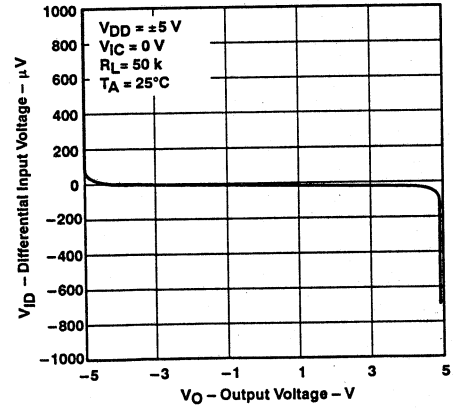


Figure 19

DIFFERENTIAL GAIN
vs
LOAD RESISTANCE

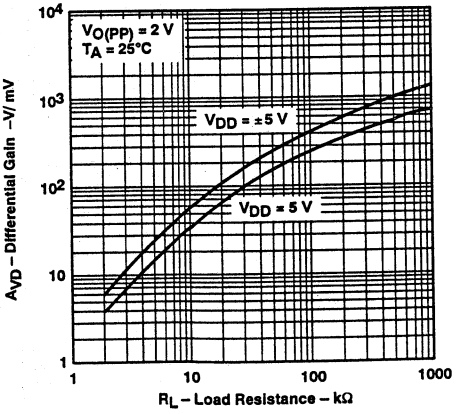


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

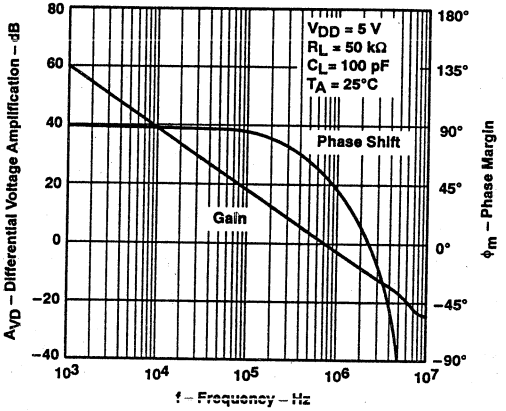


Figure 21

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

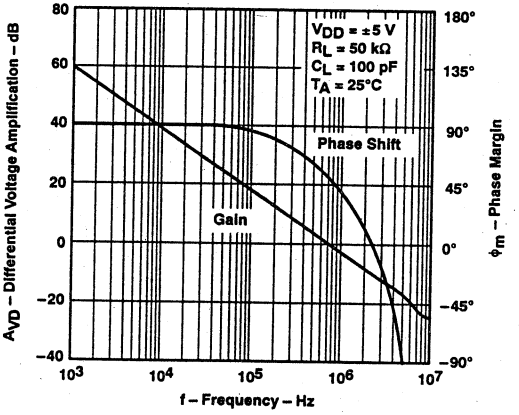


Figure 22

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

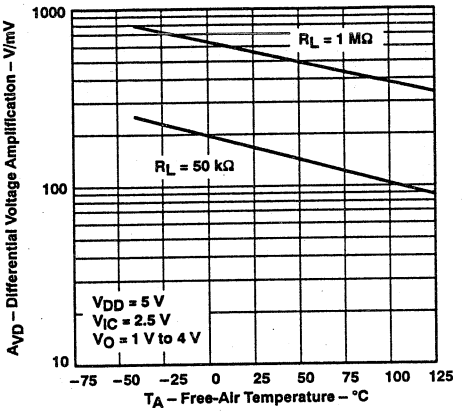


Figure 23

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

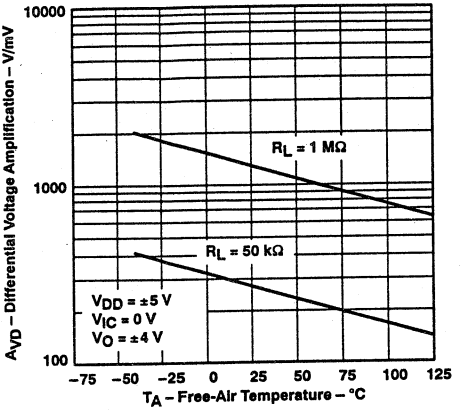


Figure 24

OUTPUT IMPEDANCE vs FREQUENCY

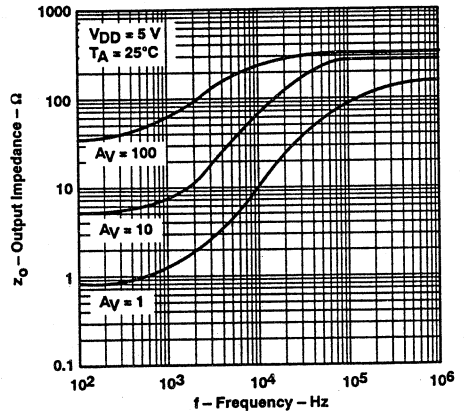


Figure 25

OUTPUT IMPEDANCE vs FREQUENCY

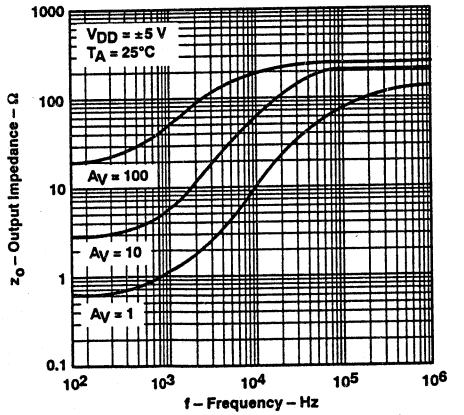


Figure 26

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

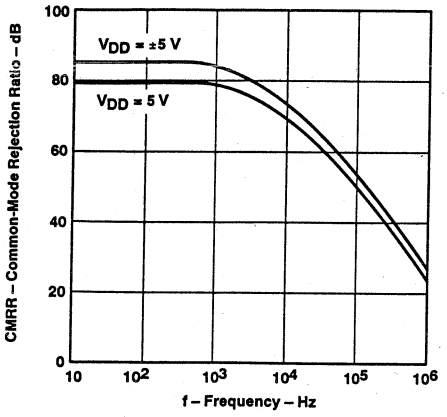


Figure 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

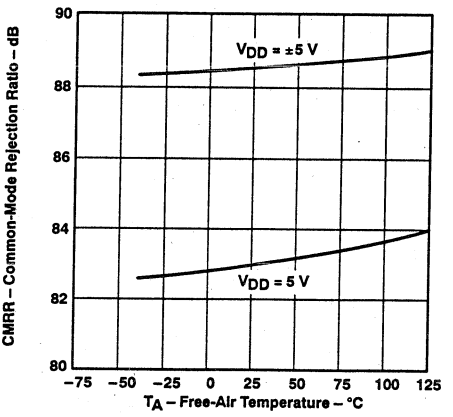


Figure 28

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

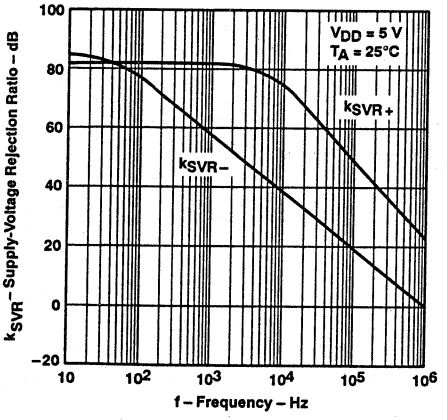


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

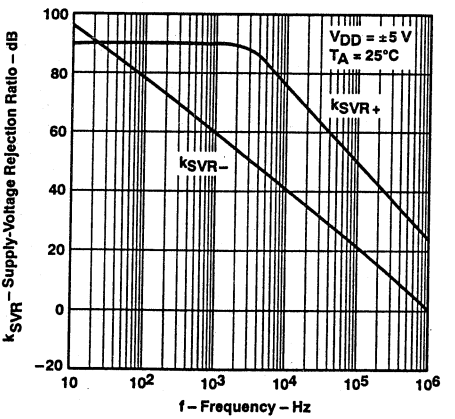


Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

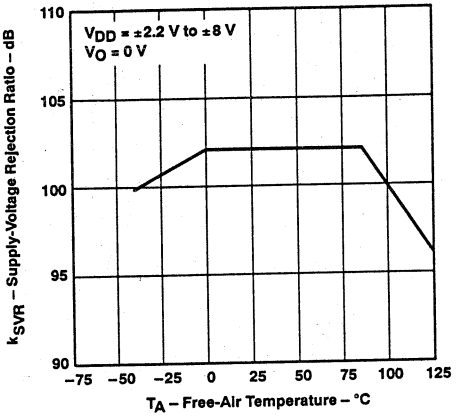


Figure 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

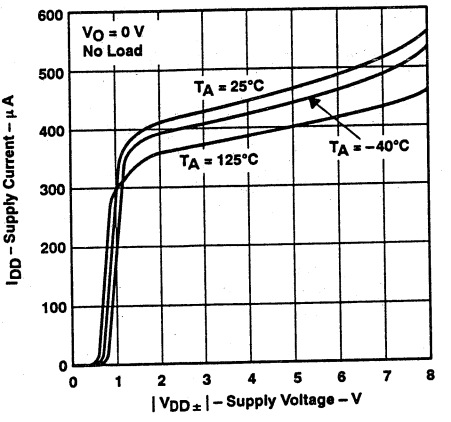


Figure 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

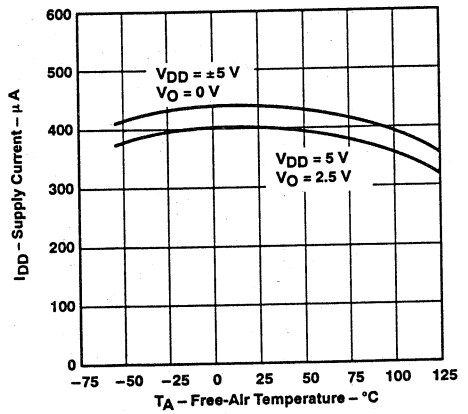


Figure 33

SLEW RATE
vs
LOAD CAPACITANCE

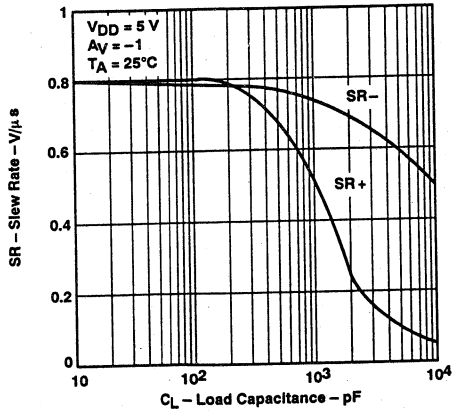


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
FREE-AIR TEMPERATURE

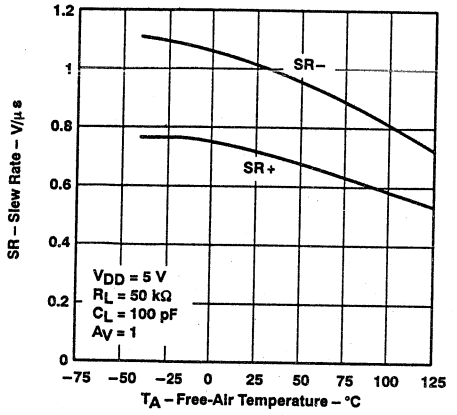


Figure 35

INVERTING LARGE-SIGNAL PULSE
RESPONSE

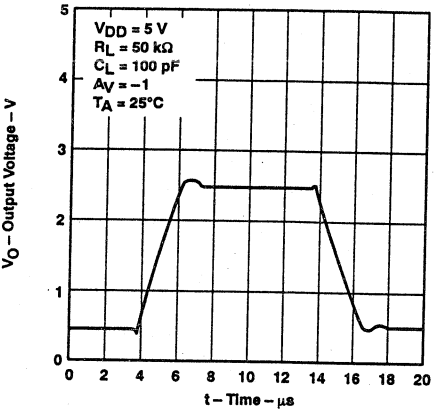


Figure 36

INVERTING LARGE-SIGNAL PULSE
RESPONSE

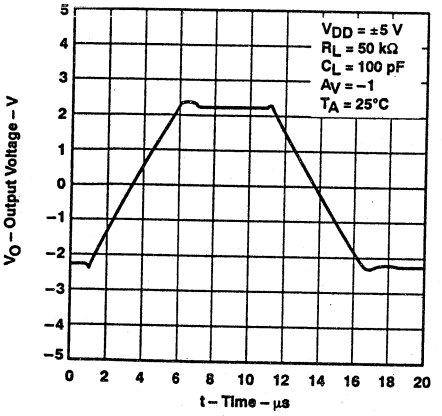


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE

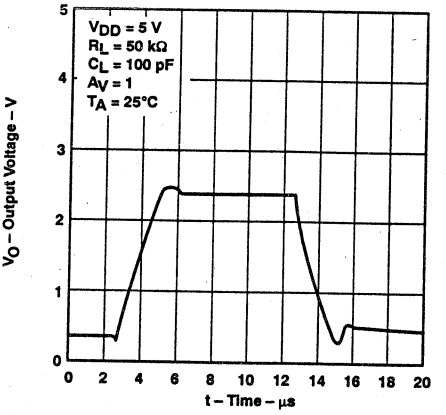


Figure 38

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

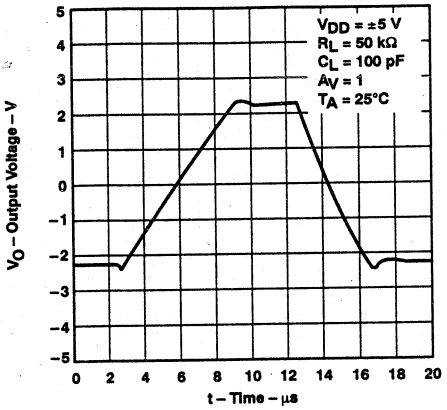


Figure 39

INVERTING SMALL-SIGNAL PULSE RESPONSE

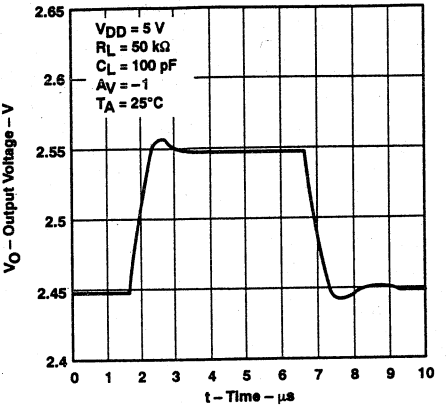


Figure 40

INVERTING SMALL-SIGNAL PULSE RESPONSE

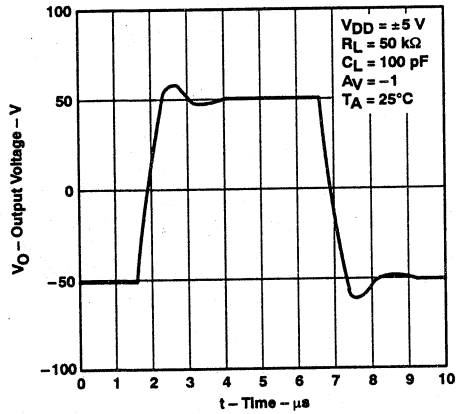


Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

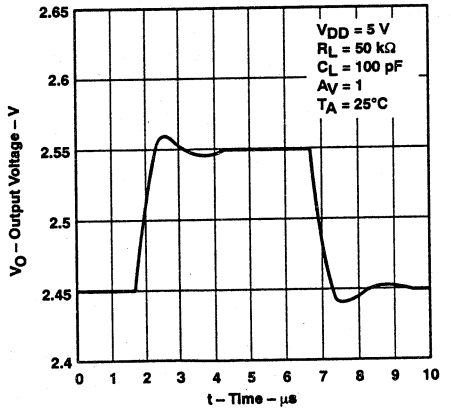


Figure 42

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

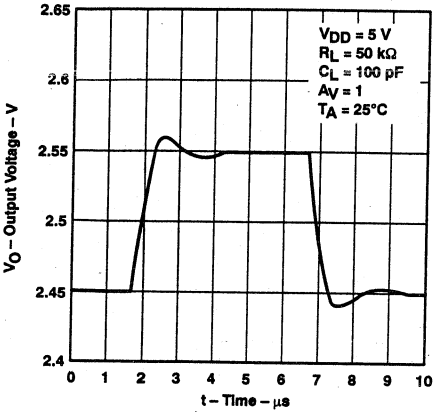


Figure 43

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

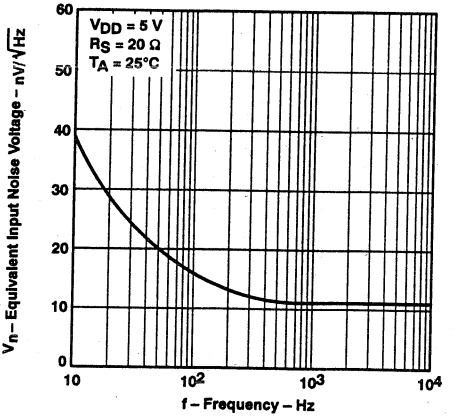


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

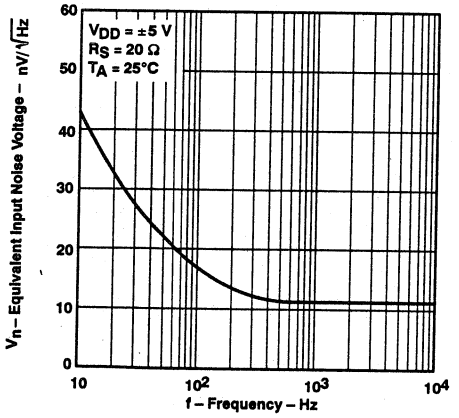


Figure 45

EQUIVALENT INPUT NOISE VOLTAGE OVER
A 10 SECOND PERIOD

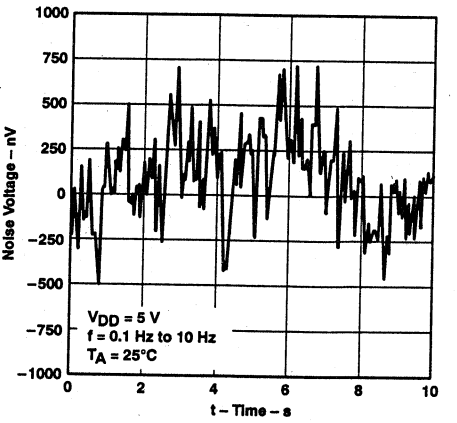


Figure 46

TYPICAL CHARACTERISTICS†

INTEGRATED NOISE VOLTAGE
vs
FREQUENCY

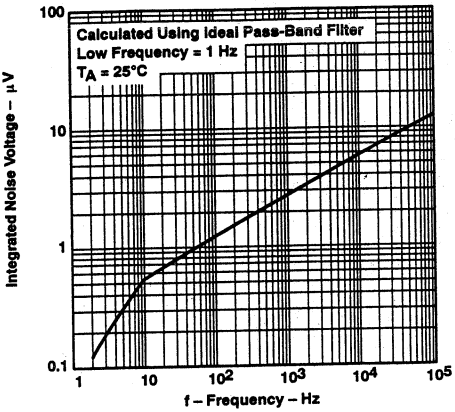


Figure 47

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

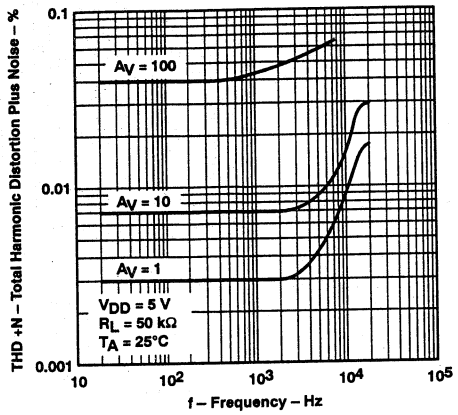


Figure 48

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

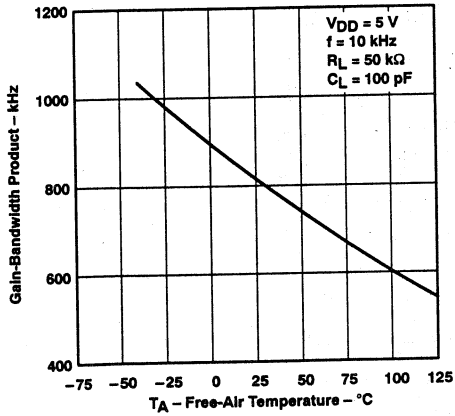


Figure 49

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

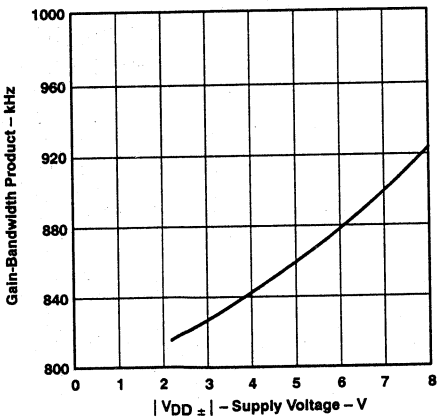


Figure 50

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

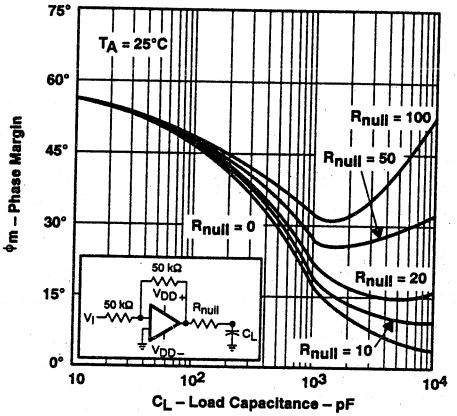


Figure 51

GAIN MARGIN
vs
LOAD CAPACITANCE

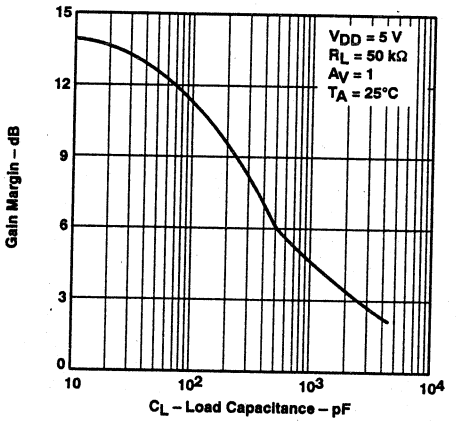


Figure 52

APPLICATION INFORMATION

loading considerations

The TLC2262 is a lower-power version of the TLC2272 with the appropriate design changes relative to the lower power level. The output drive performance to the negative rail for the TLC2262 is similar to the TLC2272 and is capable of driving several milliamperes.

The design topology used for the TLC2262 or the TLC2272 limits the drive to the positive rail to a value very close to the I_{DD} for the amplifier. Thus, while the TLC2272 is capable of greater than 1-mA drive from the positive rail, the TLC2262 is capable of only a few 100 micoamperes in proportion to the TLC2262's I_{DD}. When designing with lower impedance loads (less than 50 kΩ) with the TLC2262, the lower drive capability to the positive rail needs to be taken into consideration. Although the TLC2262 topology provides lower drive to the positive rail than other high-drive-output rail-to-rail operational amplifiers, it is a more stable topology.

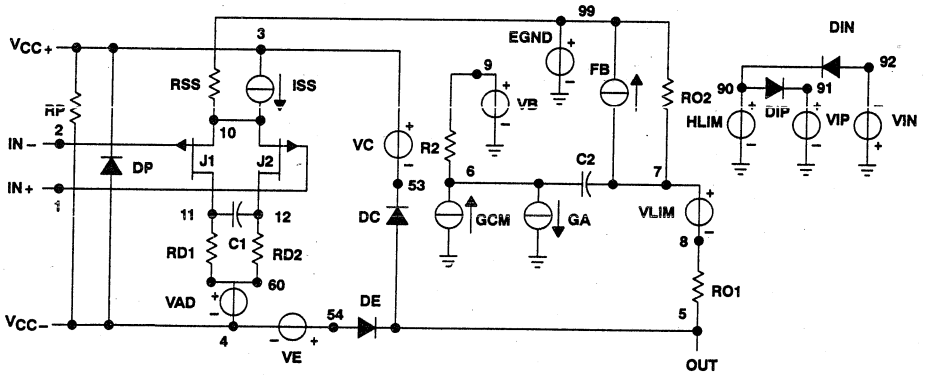
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice® Parts™* model generation software. The Boyle macromodel and subcircuit in Figure 53 are generated using the TLC2262 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE: 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLC2262 1 2 3 4 5
C1      11    12    3.520E–12
C2      6     7     15.00E–12
DC      5     53    DX
DE      54    5     DX
DLP     90    91    DX
DLN     92    90    DX
DP      4     3     DX
EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
FB      7     99    POLY (5) VB VC VE VLP
+ VLN 0 15.03E6 –30E6 30E6 30E6 –30E6
GA      6     0     11    12 47.12E–6
GCM     0     6     10    99 6.666E–9
ISS     3     10    DC 8.250E–6
HLIM    90    0     VLIM 1K
J1      11    2     10 JX
J2      12    1     10 JX
R2      6     9     100.0E3
RD1     60    11    21.22E3
RD2     60    12    21.22E3
R01     8     5     120
R02     7     99    120
RP      3     4     26.04E3
RSS     10    99    24.24E6
VAD     60    4     –.6
VB      9     0     DC 0
VC      3     53    DC .65
VE      54    4     DC .65
VLIM    7     8     DC 0
VLP     91    0     DC 0
VLN     0     92    DC 9.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=538.3E–6
+ VTO=–.031)
.ENDS
```

Figure 53. Boyle Macromodel and Subcircuit

PSpice is a registered trademark of MicroSim Corporation
Parts is a trademark of MicroSim Corporation

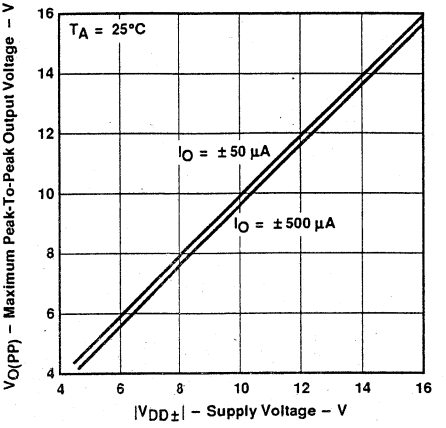
available features

- Output Swing Includes Both Supply Rails
- Low Noise . . . 9 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Common-Mode Input Voltage Range Includes Negative Rail
- High-Gain Bandwidth . . . 2 MHz Typ
- High Slew Rate . . . 3 V/μs Typ
- Low Input Offset Voltage 950 μV Max at T_A = 25°C
- Macromodel Included

description

The TLC2272 and TLC2272A are dual rail-to-rail operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices offer comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. In addition, the common-mode input voltage range is wider than typical standard CMOS type amplifiers. To take advantage of this improvement in performance, making this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ±5 mV. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. Also, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE



The TLC2272 and TLC2272A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices for inputs to ADCs in either the unipolar

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			CHIP FORM (Y)
		SMALL-OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	950 μV	TLC2272ACD	TLC2272ACP	TLC2272CPWLE	TLC2272Y
	2.5 mV	TLC2272CD	TLC2272CP		
– 40°C to 85°C	950 μV	TLC2272AID	TLC2272AIP	—	
	2.5 mV	TLC2272ID	TLC2272IP		
– 55°C to 125°C	950 μV	TLC2272AMD	TLC2272AMP	—	
	2.5 mV	TLC2272MD	TLC2272MP		

D packages are available taped and reeled. Add R suffix to device type, (e.g., TLE2272CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

Advanced LinCMOS™ is a trademark of Texas Instruments Incorporated.

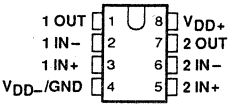
TEXAS INSTRUMENTS

description (continued)

or bipolar mode of operation. This feature, combined with its temperature performance, makes the TLC2272 family ideal for sonobuoys, pressure sensors, temperature control, active VR sensors, accelerometers, and many other applications.

The device inputs and outputs are designed to withstand 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

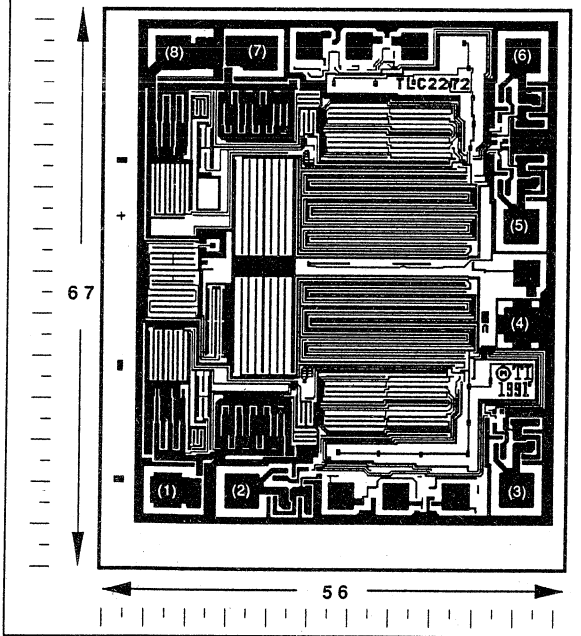
D, P, OR PW PACKAGE
(TOP VIEW)

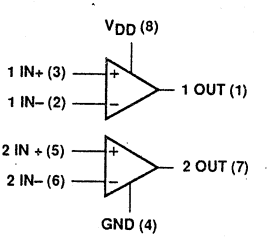


TLC2272Y chip information

These chips, properly assembled, display characteristics similar to the TLC2272C (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

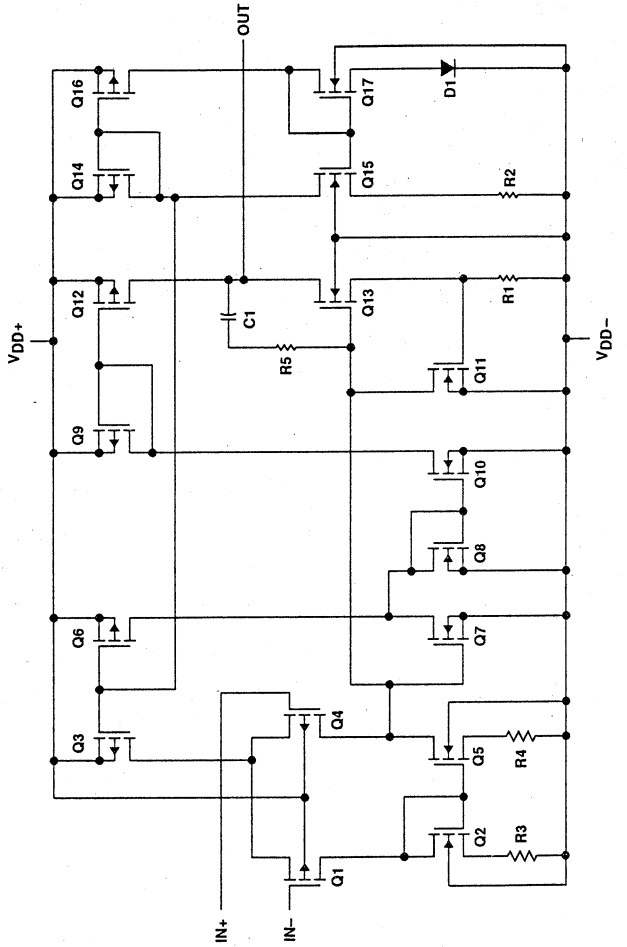
BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	38
Diodes	9
Resistors	26
Capacitors	3

†Includes both amplifiers and all ESD, bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) . . . . . 8 V
Supply voltage, V_{DD-} (see Note 1) . . . . . – 8 V
Differential input voltage (see Note 2) . . . . . ±16 V
Input voltage range, V_I (any input, see Note 1) . . . . . ±8 V
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} terminal . . . . . ±50 mA
Total current out of V_{DD-} terminal . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . –40°C to 85°C
M-suffix . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	336 mW	—	—

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	± 2.2	± 8	± 2.2	± 8	± 2.2	± 8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Operating free-air temperature, T_A	0	70	– 40	85	– 55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2272C			TLC2272AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, $V_{DD\pm}$ = ±2.5 V, V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\| \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA	25°C		4.99			4.99		V
		I_{OH} = −200 μA	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		I_{OH} = −1 mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
			Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 10 kΩ‡	25°C	15	35		15	35		V/mV
			Full range	15			15			
		R_L = 1 MΩ‡	25°C		175			175		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	75		70	75		dB
			Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, No load, V_{IC} = V_{DD}/2	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		2.2	3		2.2	3	mA
			Full range			3			3	

†Full range is 0°C to 70°C.
‡Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272C			TLC2272AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	2.5	3.6		2.5	3.6		V/ μs
				Full range	2			2			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272C			TLC2272AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			100			100	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\| \le$ 5 mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA		25°C		4.99			4.99		V
		I_O = −200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 μA		25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 μA		25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0, I_O = 5 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	25°C	25	50		25	50		V/mV
				Full range	25			25			
			R_L = 1 MΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10		25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0, R_S = 50 Ω		25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, No load, V_{IC} = 0		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0, No load		25°C		2.4	3		2.4	3	mA
				Full range			3			3	

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272C			TLC2272AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF		25°C	2.5	3.6		2.5	3.6		V/ μs
				Full range	2			2			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, f = 20 kHz, R_L = 10 kΩ	A_V = 1	25°C		0.0011%			0.0011%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF		25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ, C_L = 100 pF		25°C		0.54			0.54		MHz
	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 10 kΩ, C_L = 100 pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2272I			TLC2272AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_{DD}± = ±2.5 V, V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\| \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA	25°C		4.99			4.99		V
		I_{OH} = −200 μA	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		I_{OH} = −1 mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
			Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 10 kΩ‡	25°C	15	35		15	35		V/mV
			Full range	15			15			
		R_L = 1 MΩ‡	25°C		175			175		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	75		70	75		dB
			Full range	70			70			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, No load, V_{IC} = V_{DD}/2	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load,	25°C		2.2	3		2.2	3	mA
			Full range			3			3	

†Full range is – 40°C to 85°C.
‡Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	2.5	3.6		2.5	3.6		V/ μs
				Full range	2			2			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert \le$ 5 mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA		25°C		4.99			4.99		V
		I_O = −200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 μA		25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 μA		25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0, I_O = 5 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	25°C	25	50		25	50		V/mV
				Full range	25			25			
			R_L = 1 MΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10		25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0, R_S = 50 Ω		25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, No load, V_{IC} = 0		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0, No load		25°C		2.4	3		2.4	3	mA
				Full range			3			3	

†Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF		25°C	2.5	3.6		2.5	3.6		V/ μs
				Full range	2			2			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 10 kΩ, f = 20 kHz	A_V = 1	25°C		0.0011%			0.0011%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF		25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ, C_L = 100 pF		25°C		0.54			0.54		MHz
	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 10 kΩ, C_L = 100 pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

†Full range is − 40°C to 85°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272M			TLC2272AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_{DD}± = ±2.5 V, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\| \le$ 5 mV		25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_{OH} = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA		25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA		25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 5 mA		25°C		0.9	1.5		0.9	1.5	
				Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	10	35		10	35		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		175			175		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10		25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, No load, V_{IC} = V_{DD}/2		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load		25°C		2.2	3		2.2	3	mA
				Full range			3			3	

†Full range is − 55°C to 125°C.
‡Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272M			TLC2272AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	2.5	3.6		2.5	3.6		V/ μs
				Full range	2			2			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%	25°C		2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272M			TLC2272AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert \le$ 5 mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.99			4.99		V
		I_O = −200 µA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 µA		25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 µA		25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0, I_O = 5 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	25°C	20	50		20	50		V/mV
				Full range	20			20			
			R_L = 1 MΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10		25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0, R_S = 50 Ω		25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, No load, V_{IC} = 0		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0, No load		25°C		2.4	3		2.4	3	mA
				Full range			3			3	

†Full range is − 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272M			TLC2272AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF		25°C	2.5	3.6		2.5	3.6		V/ μs
				Full range	2			2			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 10 kΩ, f = 20 kHz	A_V = 1	25°C		0.0011%			0.0011%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF		25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ, C_L = 100 pF		25°C		0.54			0.54		MHz
	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 10 kΩ, C_L = 100 pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

†Full range is − 55°C to 125°C.

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, $V_{DD}\pm$ = ±2.5 V, V_O = 0, R_S = 50 Ω			300	2500	μV
I_{IO}	Input offset current				0.5	100	pA
I_{IB}	Input bias current				1	100	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO}\rvert \le$ 5 mV		0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA			4.99		V
		I_{OH} = −200 μA		4.85	4.93		
		I_{OH} = −1 mA		4.25	4.65		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA			0.09	0.15	
		V_{IC} = 2.5 V, I_{OL} = 5 mA			0.9	1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ†	15	35		V/mV
			R_L = 1 MΩ†		175		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		70	75		dB
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, No load, V_{IC} = V_{DD}/2		80	95		dB
I_{DD}	Supply current	V_O = 2.5 V, No load			2.2	3	mA

†Referenced to 2.5 V

electrical characteristics at $V_{DD\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω			300	2500	μV
I_{IO}	Input offset current				0.5	100	pA
I_{IB}	Input bias current				1	100	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\| \le$ 5 mV		−5 to 4	−5.3 to 4.2		V
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA			4.99		V
		I_O = −200 μA		4.85	4.93		
		I_O = −1 mA		4.25	4.65		
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 μA			−4.99		V
		V_{IC} = 0, I_O = 500 μA		−4.85	−4.91		
		V_{IC} = 0, I_O = 5 mA		−3.5	−4.1		
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	25	50		V/mV
			R_L = 1 MΩ		300		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0, R_S = 50 Ω		75	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, No load, V_{IC} = 0		80	95		dB
I_{DD}	Supply current	V_O = 0, No load			2.4	3	mA

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
		vs Common-mode voltage	3, 4
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I_{IB}/I_{IO}	Input bias and offset current	vs Temperature	7
V_I	Input voltage range	vs Supply voltage	8
		vs Temperature	9
V_{OH}	High-level output voltage	vs Output current	10
V_{OL}	Low-level output voltage	vs Output current	11, 12
V_{OM+}	Maximum positive peak output voltage	vs Output current	13
V_{OM-}	Maximum negative peak output voltage	vs Output current	14
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	15
I_{OS}	Short-circuit output current	vs Supply voltage	16
		vs Temperature	17
V_{ID}	Differential input voltage	vs Output voltage	18, 19
A_{VD}	Differential voltage amplification	vs Load resistance	20
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CMRR	Common-mode rejection ratio	vs Frequency	27
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k_{SVR}	Supply voltage rejection ratio	vs Frequency	29, 30
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I_{DD}	Supply current	vs Supply voltage	32
		vs Temperature	33
SR	Slew rate	vs Load capacitance	34
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V_O	Large-signal pulse response	vs Time	36, 37, 38, 39
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	Noise voltage (referred to input)	Over a 10-second period	46
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THD + N	Total harmonic distortion plus noise	vs Frequency	48
	Gain-bandwidth product	vs Temperature	49
		vs Supply voltage	50
ϕ_m	Phase margin	vs Load capacitance	51
		vs Frequency	21, 22
	Gain margin	vs Load capacitance	52

NOTE: For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE

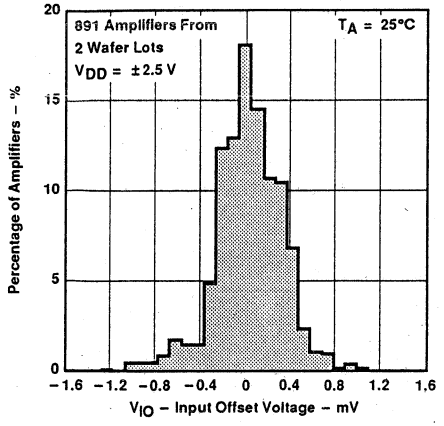


Figure 1

DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE

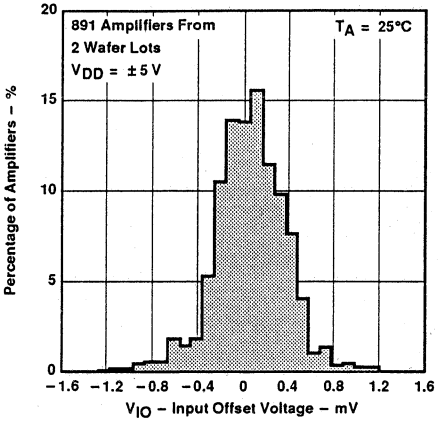


Figure 2

INPUT OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

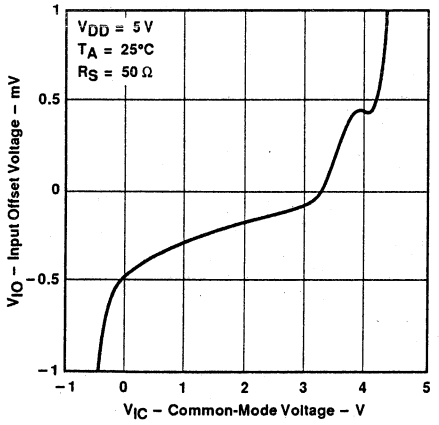


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

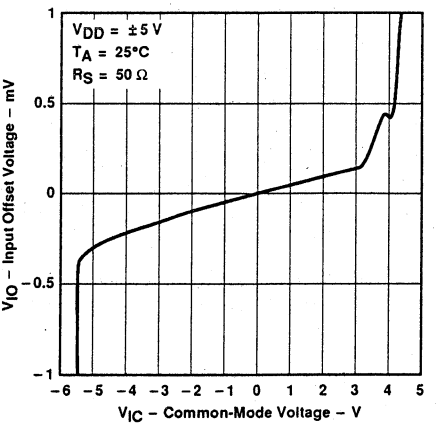


Figure 4

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC2272 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

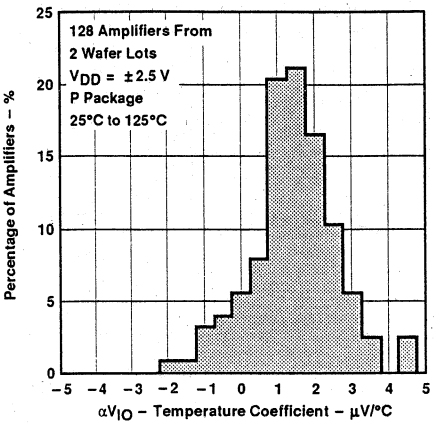


Figure 5

DISTRIBUTION OF TLC2272 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

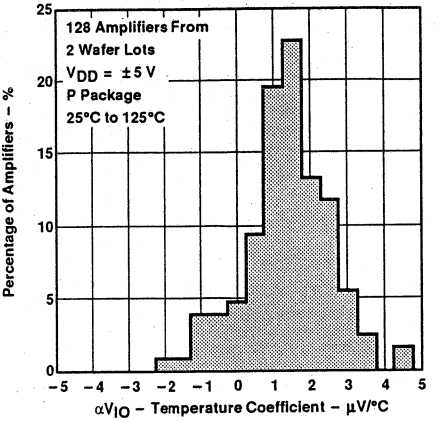


Figure 6

INPUT BIAS AND OFFSET CURRENT vs FREE-AIR TEMPERATURE

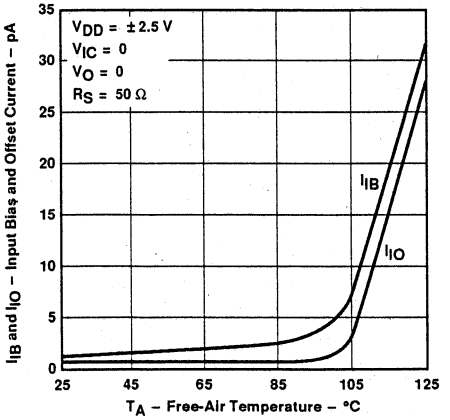


Figure 7

INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

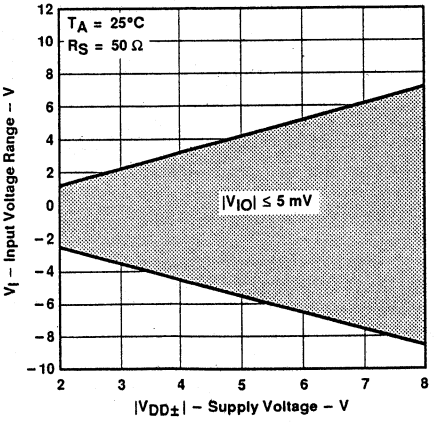


Figure 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

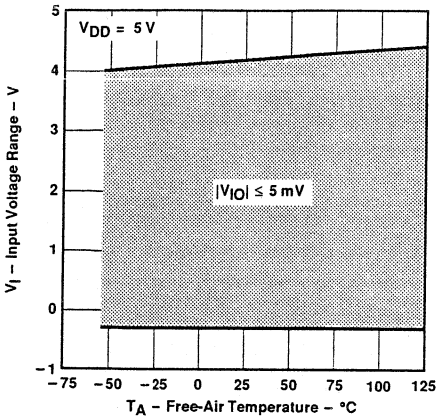


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

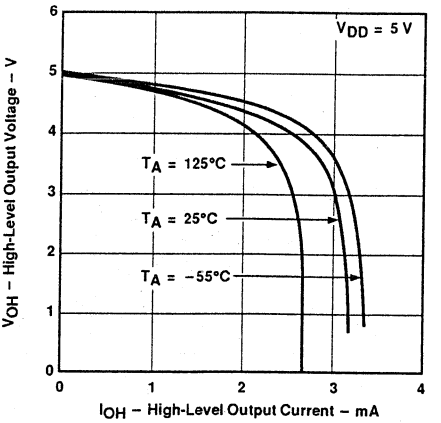


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

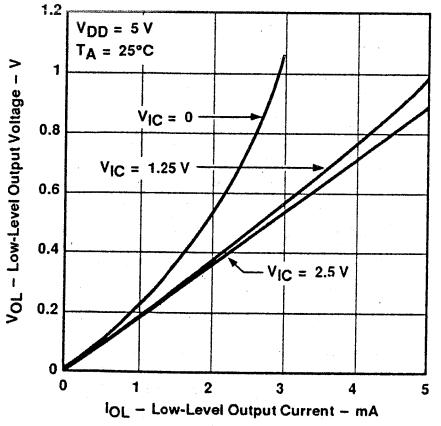


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

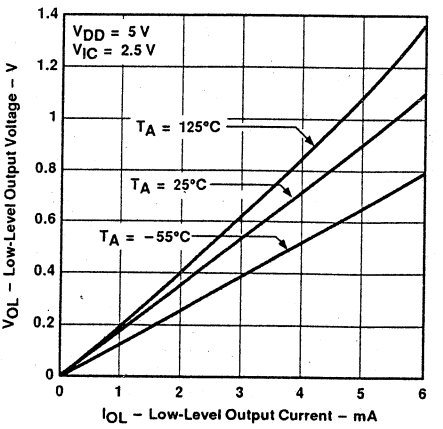


Figure 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

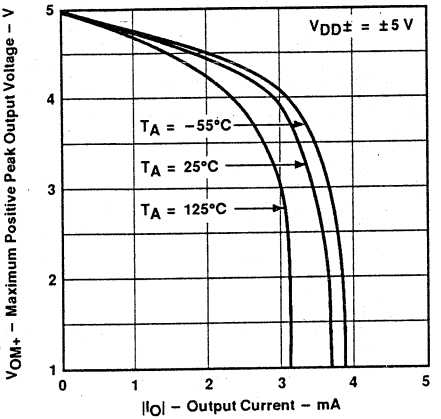


Figure 13

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

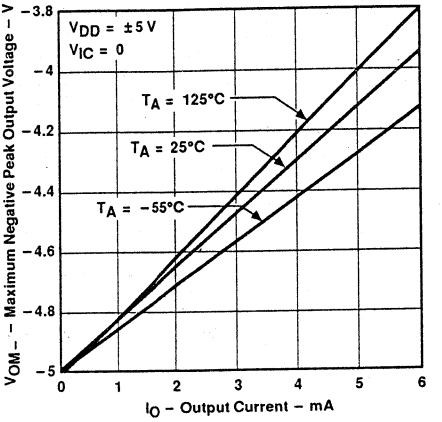


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

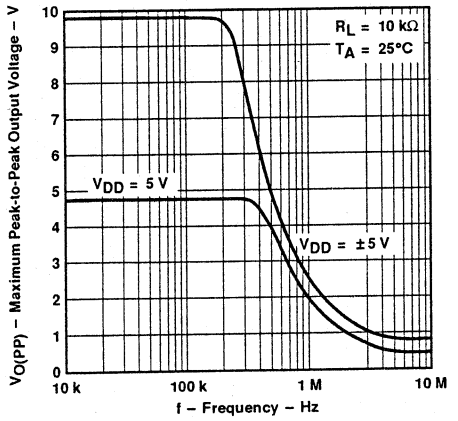


Figure 15

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

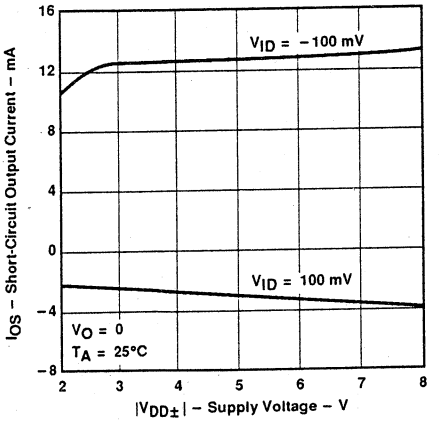


Figure 16

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

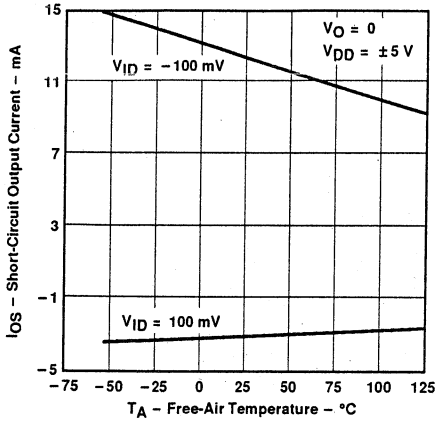


Figure 17

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

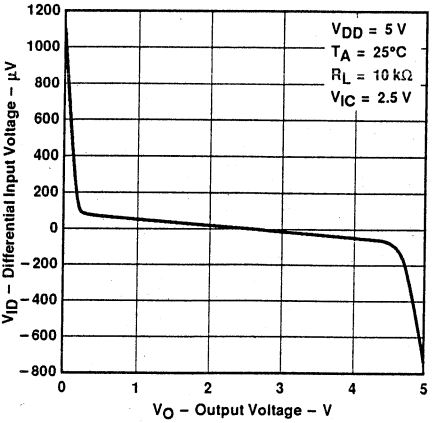


Figure 18

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

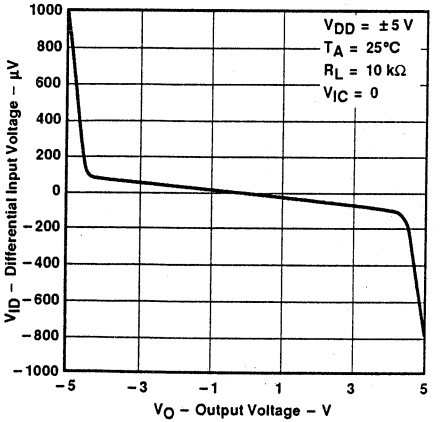


Figure 19

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

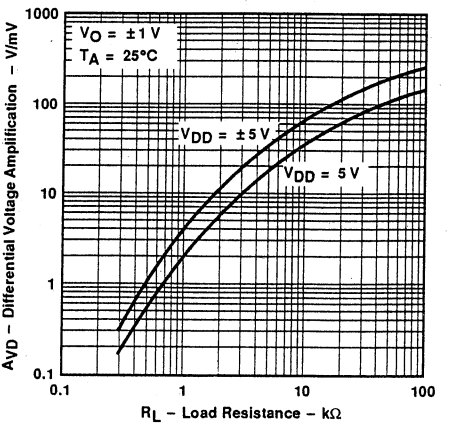


Figure 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION and PHASE MARGIN
vs
FREQUENCY

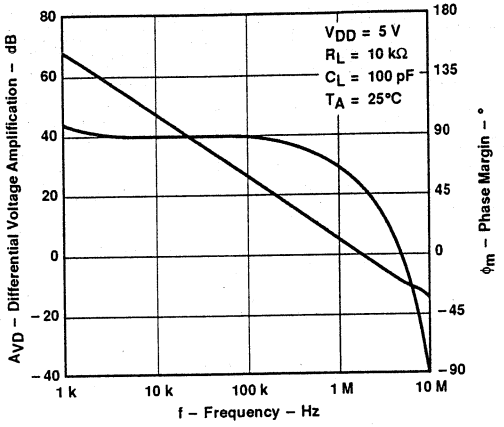


Figure 21

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION and PHASE MARGIN
vs
FREQUENCY

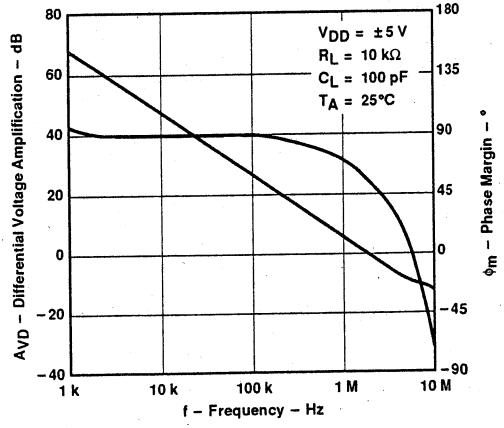


Figure 22

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

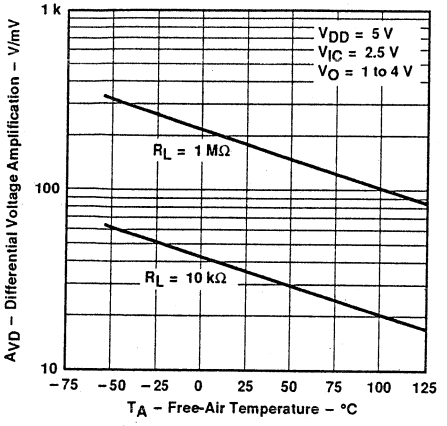


Figure 23

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

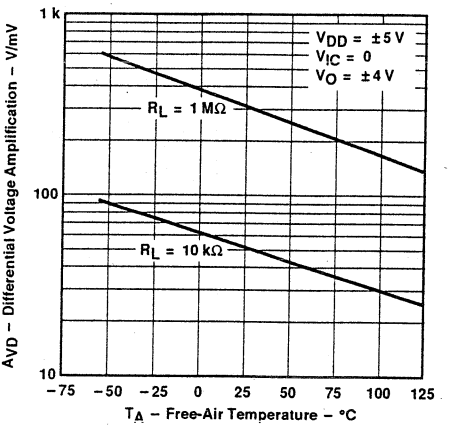


Figure 24

OUTPUT IMPEDANCE vs FREQUENCY

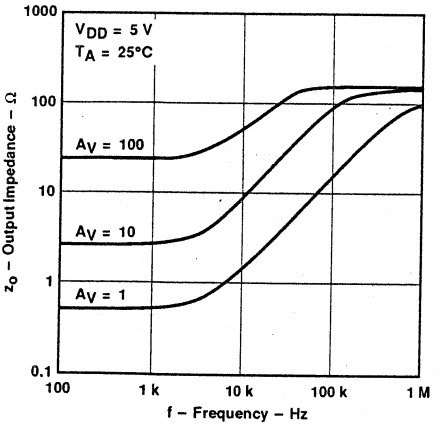


Figure 25

OUTPUT IMPEDANCE vs FREQUENCY

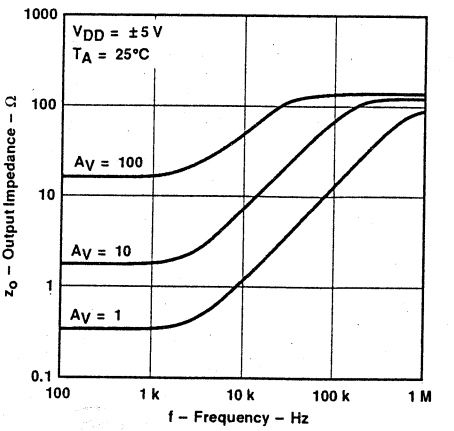


Figure 26

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

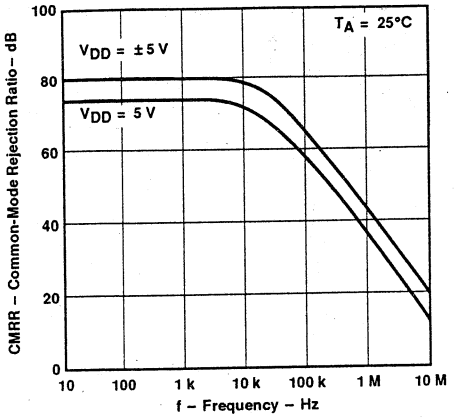


Figure 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

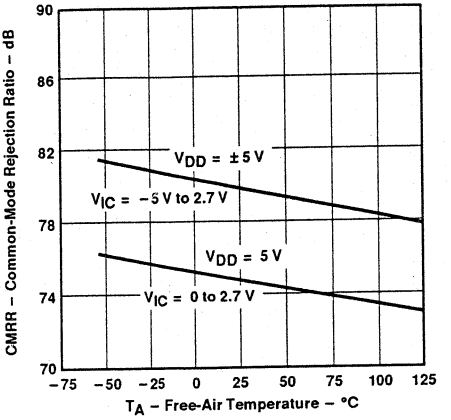


Figure 28

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

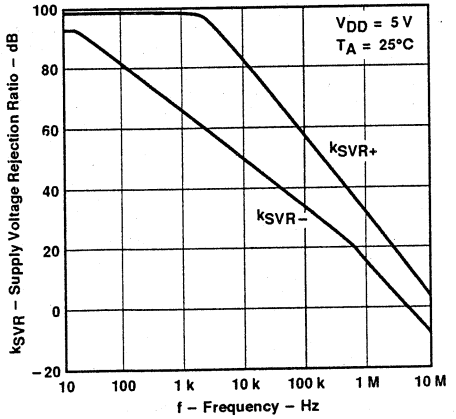


Figure 29

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

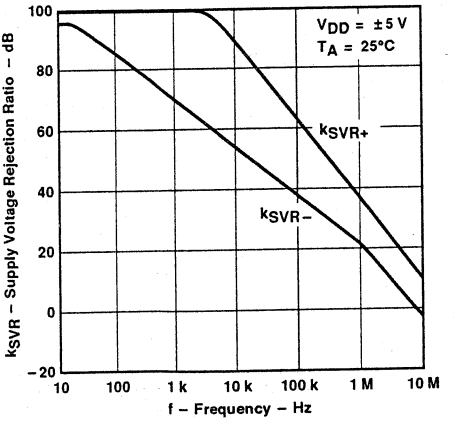


Figure 30

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

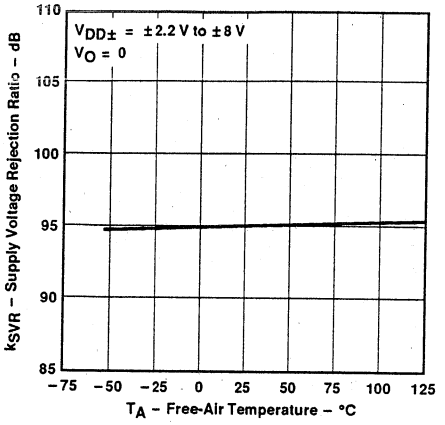


Figure 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

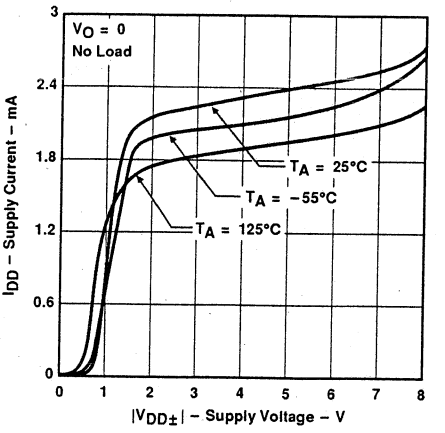


Figure 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

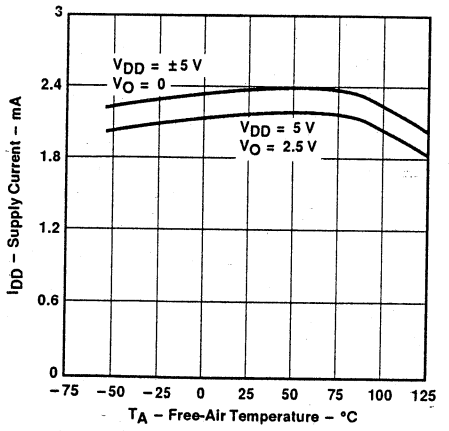


Figure 33

SLEW RATE
vs
LOAD CAPACITANCE

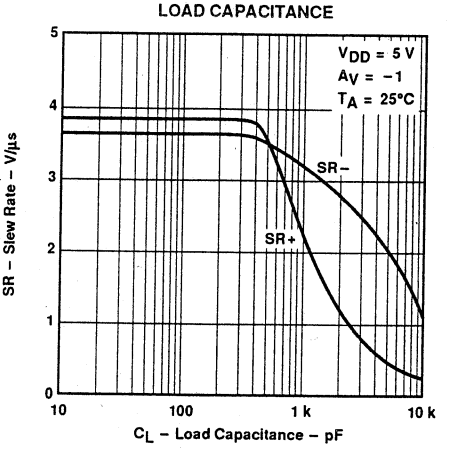


Figure 34

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
FREE-AIR TEMPERATURE

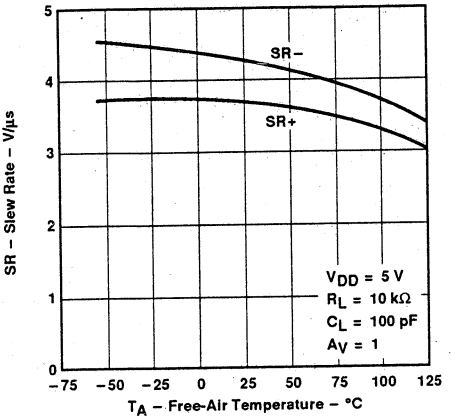


Figure 35

INVERTING LARGE-SIGNAL PULSE RESPONSE

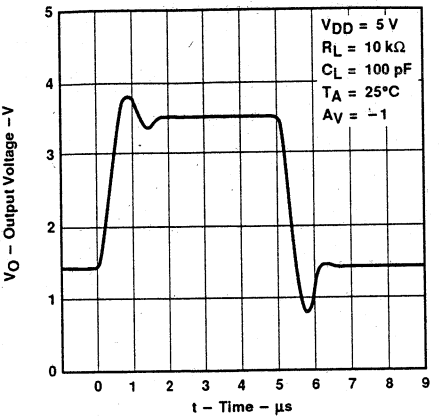


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE

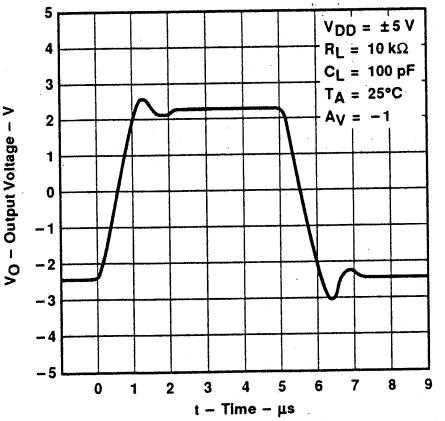


Figure 37

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

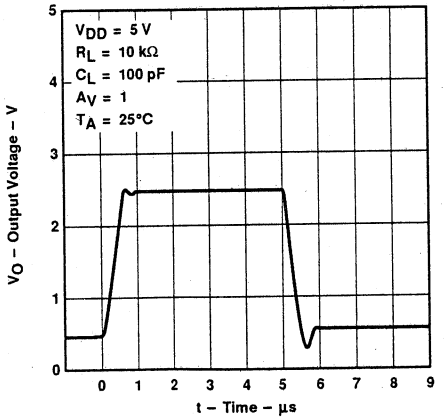


Figure 38

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

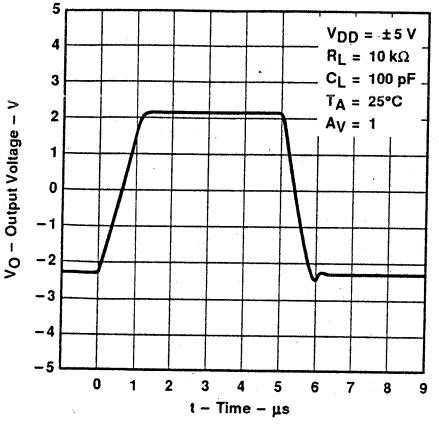


Figure 39

INVERTING SMALL-SIGNAL PULSE RESPONSE

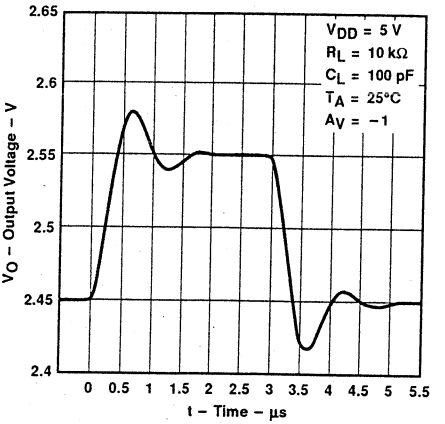


Figure 40

INVERTING SMALL-SIGNAL PULSE RESPONSE

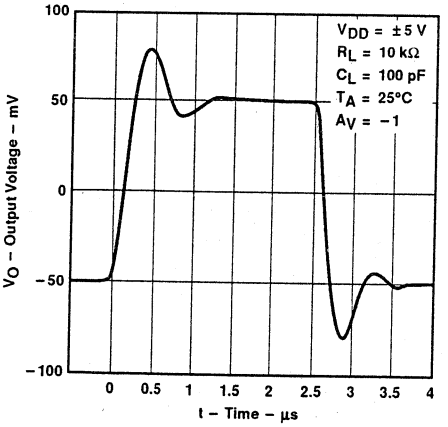


Figure 41

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

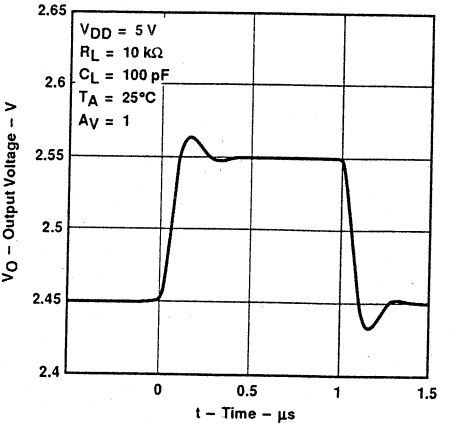


Figure 42

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

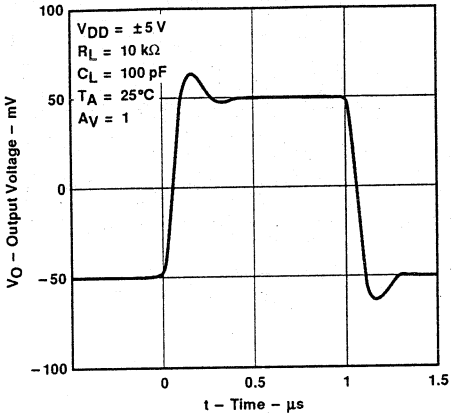


Figure 43

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

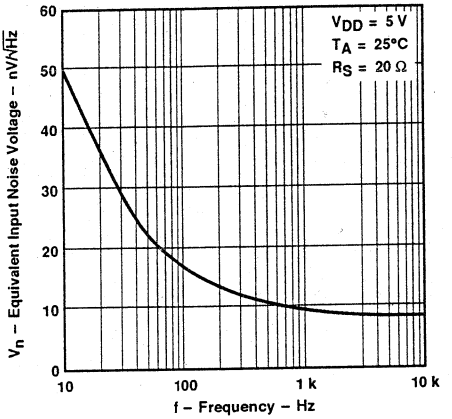


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

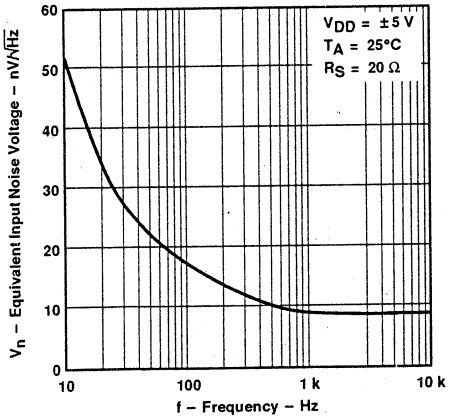


Figure 45

NOISE VOLTAGE
OVER A 10 SECOND PERIOD

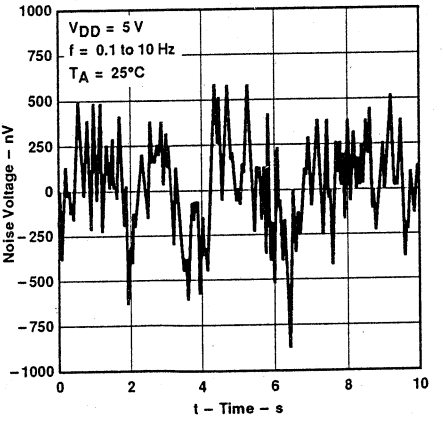


Figure 46

TYPICAL CHARACTERISTICS†

INTEGRATED NOISE VOLTAGE
vs
FREQUENCY

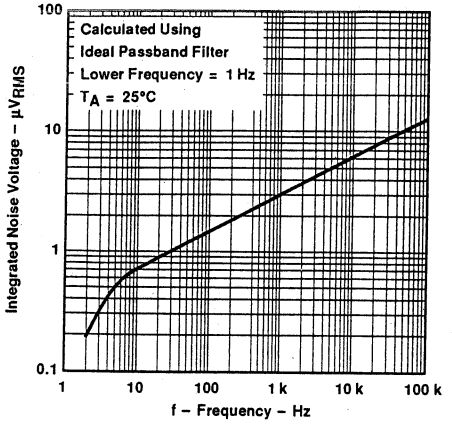


Figure 47

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

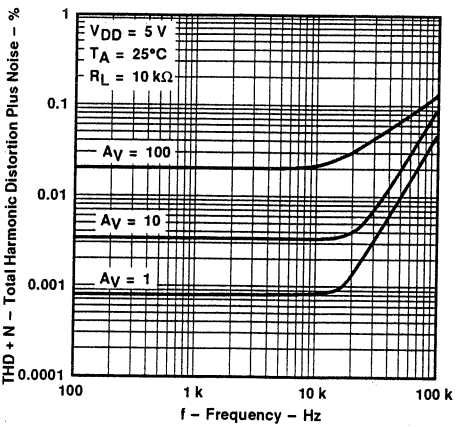


Figure 48

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

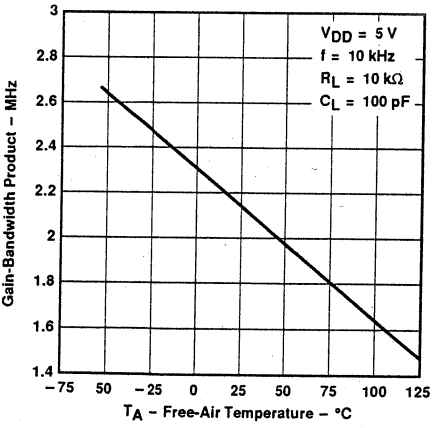


Figure 49

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

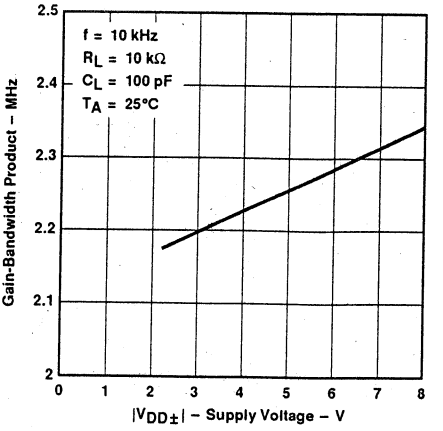


Figure 50

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

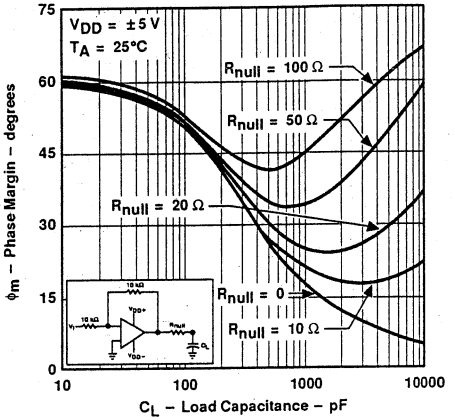


Figure 51

GAIN MARGIN
vs
LOAD CAPACITANCE

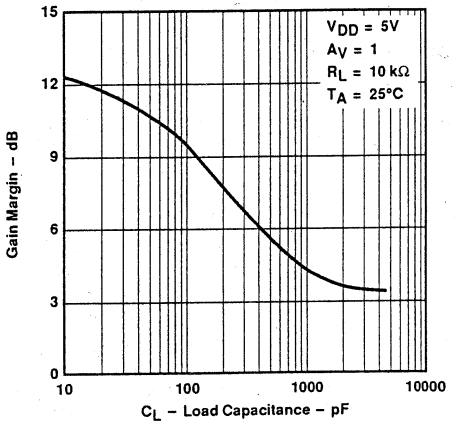


Figure 52

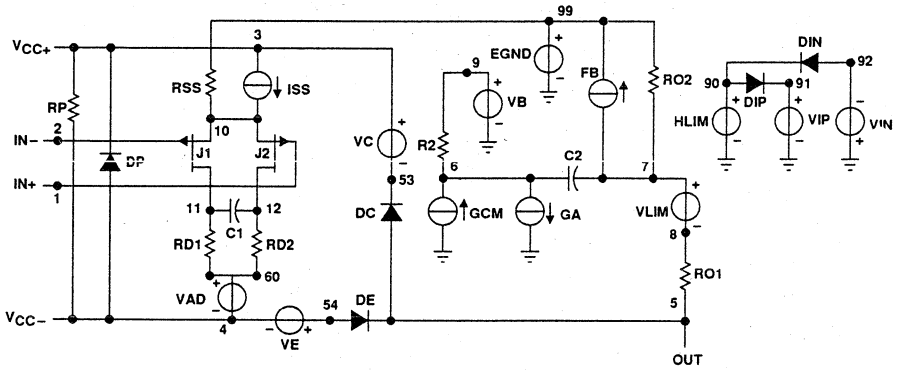
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 6) and subcircuit in Figure 53 were generated using the TLC2272 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- dc output resistance
- ac output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).



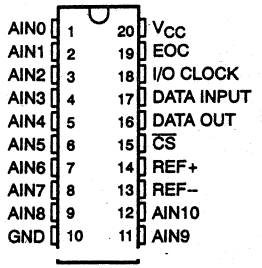

```
.SUBCKT TLC2272  1 2 3 4 5
  C1   11 12 14E-12
  C2    6  7 60.00E-12
  DC    5 53 DX
  DE   54  5 DX
  DLP  90 91 DX
  DLN  92 90 DX
  DP    4  3 DX
  EGND 99  0 POLY(2)  (3,0)  (4,0)  0 .5 .5
  FB 7 99 POLY(5) VB VC VE VLP VLN 0
+ 984.9E3 -1E6 1E6 1E6 -1E6
  GA    6  0 11 12 377.0E-6
  GCM 0  6 10 99 134E-9
  ISS   3 10 DC 216.0E-6
  HLIM 90  0 VLIM 1K
  J1   11  2 10 JX
  J2   12  1 10 JX
  R2    6  9 100.0E3
  RD1 60 11 2.653E3
  RD2 60 12 2.653E3
  RO1   8  5 50
  RO2   7 99 50
  RP    3  4 4.310E3
  RSS  10 99 925.9E3
  VAD  60  4 -.5
  VB    9  0 DC 0
  VC 3 53 DC .78
  VE   54  4 DC .78
  VLIM  7  8 DC 0
  VLP  91  0 DC 1.9
  VLN 0 92 DC 9.4
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=1.500E-12 BETA=1.316E 3
+ VTO=-.270)
.ENDS
```

Figure 53. Boyle Macromodel and Subcircuit

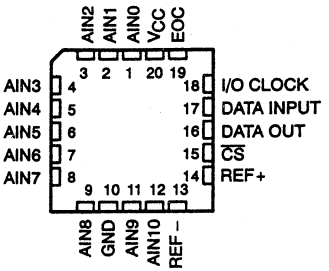
PSpice and *Parts* are trademarks of MicroSim Corporation.

- **Advanced LinEPIC™ Technology**
- **12-Bit-Resolution A/D Converter**
- **10-μs Conversion Time Over Operating Temperature**
- **11 Analog Input Channels**
- **3 Built-In Self-Test Modes**
- **Inherent Sample and Hold**
- **Linearity Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion (EOC) Output**
- **Unipolar or Bipolar Operation (Signed Binary)**
- **Programmable MSB or LSB First**
- **Programmable Power Down**
- **Programmable Output Data Length**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

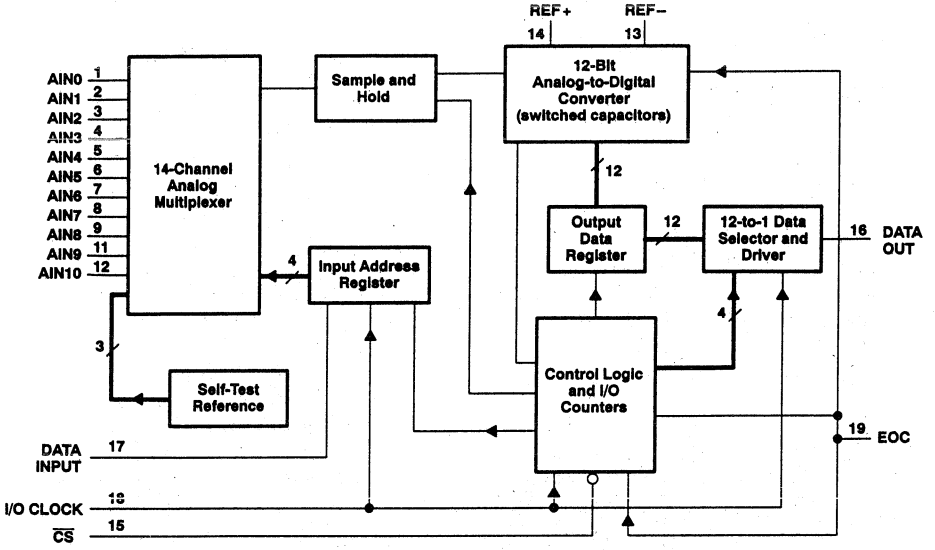
The TLC2543C and TLC2543I are Advanced LinEPIC™ 12-bit, switched-capacitor, successive-approximation, analog-to-digital converters. Each device has three control inputs [chip select ($\overline{CS}$), the input-output clock (I/O CLOCK), and the address input (DATA INPUT)] and is designed for communication with the serial port of a host processor or peripheral through a serial 3-state output. The device allows high-speed data transfers from the host.

In addition to the high-speed converter and versatile control capability, the device has an on-chip 14-channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.

The TLC2543 is available in the DW, FN, and N packages. The TLC2543C is characterized for operation from 0°C to 70°C, and the TLC2543I is characterized for operation from −40°C to 85°C.

Advanced LinEPIC is a trademark of Texas Instruments Incorporated.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AIN0 – AIN10	1–9, 11, 12	I	These 11 analog-signal inputs are internally multiplexed. The driving source impedance should be less than or equal to 50 Ω for 4.1-MHz I/O CLOCK operation and capable of slewing the analog input voltage into a capacitance of 60 pF.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT, DATA INPUT, and I/O CLOCK. A low-to-high transition disables DATA INPUT and I/O CLOCK within a setup time.
DATA INPUT	17	I	Serial-data input. A 4-bit serial address selects the desired analog input or test voltage to be converted next. The serial data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits are read into the address register, I/O CLOCK clocks the remaining bits in order.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid $\overline{CS}$, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB/LSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB/LSB, and the remaining bits are shifted out in order.
EOC	19	O	End of conversion goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10		The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial input and performs the following four functions: 1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge. 2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of I/O CLOCK. 3. It shifts the 11 remaining bits of the previous conversion data out on DATA OUT. Data changes on the falling edge of I/O CLOCK. 4. It transfers control of the conversion to the internal state controller on the falling edge of the last I/O CLOCK.
REF+	14	I	The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF– terminal.
REF–	13	I	The lower reference voltage value (nominally ground) is applied to REF–.
V_{CC}	20		Positive supply voltage

detailed description

Initially, with chip select ($\overline{CS}$) high, I/O CLOCK and DATA INPUT are disabled and DATA OUT is in the high-impedance state. $\overline{CS}$, going low, begins the conversion sequence by enabling I/O CLOCK and DATA INPUT and removes DATA OUT from the high-impedance state.

The input data is an 8-bit data stream consisting of a 4-bit analog channel address (D7–D4), a 2-bit data length select (D3–D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0) that are applied to DATA INPUT. The I/O CLOCK sequence applied to the I/O CLOCK terminal transfers this data to the input data register.

During this transfer, the I/O CLOCK sequence also shifts the previous conversion result from the output data register to DATA OUT. I/O CLOCK receives the input sequence of 8, 12, or 16 clocks long depending on the data-length selection in the input data register. Sampling of the analog input begins on the fourth falling edge of the input I/O CLOCK sequence and is held after the last falling edge of the I/O CLOCK sequence. The last falling edge of the I/O CLOCK sequence also takes EOC low and begins the conversion.

detailed description (continued)

converter operation

The operation of the converter is organized as a succession of two distinct cycles: 1) the I/O cycle and 2) the actual conversion cycle. The I/O cycle is defined by the externally provided I/O CLOCK and lasts 8, 12, or 16 clock periods, depending on the selected output data length.

1. I/O cycle

   During the I/O cycle, two operations take place simultaneously.

   a. An 8-bit data stream consisting of address and control information is provided to DATA INPUT. This data is shifted into the device on the rising edge of the first eight I/O CLOCKs. DATA INPUT is ignored after the first eight clocks during 12 or 16 clock I/O transfers.

   b. The data output, with a length of 8, 12, or 16 bits, is provided serially on DATA OUT. If $\overline{CS}$ is held low, the first output data bit occurs on the rising edge of EOC. If $\overline{CS}$ is negated between conversions, the first output data bit occurs on the falling edge of $\overline{CS}$. This data is the result of the previous conversion period, and after the first output data bit, each succeeding bit is clocked out on the falling edge of each succeeding I/O CLOCK.

2. Conversion cycle

   The conversion cycle is transparent to the user, and it is controlled by an internal clock synchronized to I/O CLOCK. During the conversion period, the device performs a successive-approximation conversion on the analog input voltage. The EOC output goes low at the start of the conversion cycle and goes high when conversion is complete and the output data register is latched. A conversion cycle is started only after the I/O cycle is completed, which minimizes the influence of external digital noise on the accuracy of the conversion.

power up and initialization

After power up, $\overline{CS}$ must be taken from high to low to begin an I/O cycle. EOC is initially high, and the input data register is set to all zeroes. The contents of the output data register are random, and the first conversion result should be ignored. To initialize during operation, $\overline{CS}$ is taken high and returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

operational terminology

Current (N) I/O cycle	The entire I/O CLOCK sequence that transfers address and control data into the data register and clocks the digital result from the previous conversion from DATA OUT
Current (N) conversion cycle	The conversion cycle starts immediately after the current I/O cycle. The end of the current I/O cycle is the last clock falling edge in the I/O CLOCK sequence. The current conversion result is loaded into the output register when conversion is complete.
Current (N) conversion result	The current conversion result is serially shifted out on the next I/O cycle.
Previous (N−1) conversion cycle	The conversion cycle just prior to the current I/O cycle
Next (N+1) I/O cycle	The I/O period that follows the current conversion cycle

Example: In the 12-bit mode, the result of the current conversion cycle is a 12-bit serial-data stream clocked out during the next I/O cycle. The current I/O cycle must be exactly 12 bits long to maintain synchronization, even if this corrupts the output data from the previous conversion. The current conversion is begun immediately after the 12th falling edge of the current I/O cycle.

detailed description (continued)

data input

The data input is internally connected to an 8-bit serial-input address and control register. The register defines the operation of the converter and the output data length. The host provides the data word with the MSB first. Each data bit is clocked in on the rising edge of the I/O CLOCK sequence (see Table 1 for the data register format).

data input address bits

The four MSBs (D7 – D4) of the data register are used to address one of the 11 input channels, a reference-test voltage, or the power-down mode. The address bits affect the current conversion, which is the conversion that immediately follows the current I/O cycle. The reference voltage is nominally equal to $V_{ref+} - V_{ref-}$.

data output length

The next two bits (D3 and D2) of the data register select the output data length. The data-length selection is valid for the current I/O cycle (the cycle in which the data is read). The data-length selection, being valid for the current I/O cycle, allows device start up without losing I/O synchronization. A data length of 8, 12, or 16 bits can be selected. Since the converter has 12-bit resolution, a data length of 12 bits is suggested.

With D3 and D2 set to 00 or 10, the device is in the 12-bit data-length mode and the result of the current conversion is output as a 12-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly 12 bits long for proper synchronization, even if this means corrupting the output data from a previous conversion. The current conversion is started immediately after the 12th falling edge of the current I/O cycle.

With bits D3 and D2 set to 11, the 16-bit data-length mode is selected, which allows convenient communication with 16-bit serial interfaces. In the 16-bit mode, the result of the current conversion is output as a 16-bit serial-data stream during the next I/O cycle with the four LSBs always set to 0 (pad bits). The current I/O cycle must be exactly 16 bits long to maintain synchronization even if this means corrupting the output data from the previous conversion. The current conversion is immediately started after the 16th falling edge of the current I/O cycle.

With bits D3 and D2 set to 01, the 8-bit data-length mode is selected, which allows fast communication with 8-bit serial interfaces. In the 8-bit mode, the result of the current conversion is output as an 8-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly 8 bits long to maintain synchronization, even if this means corrupting the output data from the previous conversion. The four LSBs of the conversion result are truncated and discarded. The current conversion is immediately started after the 8th falling edge of the current I/O cycle.

Since D3 and D2 take effect on the current I/O cycle when the data length is programmed, there can be a conflict with the previous cycle when the data-word length is changed from one cycle to the next. This may occur when the data format is selected to be least significant bit first, since at the time the data length change becomes effective (6 rising edges of I/O CLOCK), the previous conversion result has already started shifting out.

In actual operation, if different data lengths are required within an application and the data length is changed between two conversions, no more than one conversion result can be corrupted and only if it is shifted out in LSB first format.

detailed description (continued)

sampling period

During the sampling period, one of the analog inputs is internally connected to the capacitor array of the converter to store the analog input signal. The converter starts sampling the selected input immediately after the four address bits have been clocked into the input data register. Sampling starts on the 4th falling edge of I/O CLOCK. The converter remains in the sampling mode until the 8th, 12th, or 16th falling edge of the I/O CLOCK depending on the data-length selection. After the EOC delay time from the last I/O CLOCK falling edge, the EOC output goes low indicating that the sampling period is over and the conversion period has begun. After EOC goes low, the analog input can be changed without affecting the conversion result. Since the delay from the falling edge of the last I/O CLOCK to EOC low is fixed, time-varying analog input signals can be digitized at a fixed rate without introducing systematic harmonic distortion or noise due to timing uncertainty.

After the 8-bit data stream has been clocked in, DATA INPUT should be held at a fixed digital level until EOC goes high (indicating the conversion is complete) to maximize the sampling accuracy and minimize the influence of external digital noise.

data register, LSB first

D1 in the input data register (LSB first) is used to control the direction of the output binary data transfer. When D1 is set to 0, the conversion result is shifted out MSB first. When set to 1, the data is shifted out LSB first. Selection of MSB first or LSB first always affects the next I/O cycle and not the current I/O cycle. When changing from one data direction to another, the current I/O cycle is never disrupted.

data register, bipolar format

D0 in the input data register (BIP) is used to control the binary data format used to represent the conversion result. When D0 is set to 0, the conversion result is represented as unipolar (unsigned binary) data. Nominally, the conversion result of an input voltage equal to V_{ref-} is a code of all zeros (000 . . . 0), the conversion result of an input voltage equal to V_{ref+} is a code of all ones (111 . . . 1), and the conversion result of $(V_{ref+} + V_{ref-})/2$ is a code of a one followed by zeros (100 . . . 0).

When D0 is set to 1, the conversion result is represented as bipolar (signed binary) data. Nominally, conversion of an input voltage equal to V_{ref-} is a code of a 1 followed by zeros (100 . . . 0), conversion of an input voltage equal to V_{ref+} is a code of a 0 followed by all ones (011 . . . 1), and the conversion of $(V_{ref+} + V_{ref-})/2$ is a code of all zeros (000 . . . 0). The MSB is interpreted as the sign bit. The bipolar data format is related to the unipolar format in that the MSBs are always each other's complement.

Selection of the unipolar or bipolar format always affects the current conversion cycle, and the result is output during the next I/O cycle. When changing between unipolar and bipolar formats, the data output during the current I/O cycle is not affected.

EOC output

The EOC signal indicates the beginning and the end of conversion. In the reset state, EOC is always high. During the sampling period (beginning after the 4th falling edge of the I/O CLOCK sequence), EOC remains high until the internal sampling switch of the converter is safely opened. The opening of the sampling switch occurs after the 8th, 12th, or 16th I/O CLOCK falling edge, depending on the data-length selection in the input data register. After the EOC signal goes low, the analog input signal can be changed without affecting the conversion result.

The EOC signal goes high again after the conversion is completed and the conversion result is latched into the output data register. The rising edge of EOC returns the converter to a reset state and a new I/O cycle begins. On the rising edge of EOC, the first bit of the current conversion result is on DATA OUT if $\overline{CS}$ is low. If $\overline{CS}$ is negated between conversions, the first bit of the current conversion result occurs at DATA OUT on the falling edge of $\overline{CS}$.

detailed description (continued)

data format and pad bits

D3 and D2 of the input data register determine the number of significant bits in the digital output that represent the conversion result. The LSB-first bit determines the direction of the data transfer while the BIP bit determines the arithmetic conversion. The numerical data is always justified toward the MSB in any output format.

The internal conversion result is always 12 bits long. When an 8-bit data transfer is selected, the four LSBs of the internal result are discarded to provide a faster one-byte transfer. When a 12-bit transfer is used, all bits are transferred. When a 16-bit transfer is used, four LSB pad bits are always appended to the internal conversion result. In the LSB-first mode, four leading zeros are output. In the MSB-first mode, the last four bits output are zeros.

When $\overline{CS}$ is held low continuously, the first data bit of the just completed conversion occurs on DATA OUT on the rising edge of EOC. When a new conversion is started after the last falling edge of I/O CLOCK, EOC goes low and the serial output is forced to a logic zero until EOC goes high again.

When $\overline{CS}$ is negated between conversions, the first data bit occurs on DATA OUT on the falling edge of $\overline{CS}$. On each subsequent falling edge of I/O CLOCK after the first data bit appears, the data is changed to the next bit in the serial conversion result until the required number of bits has been output.

chip-select input ($\overline{CS}$)

The chip-select input ($\overline{CS}$) is used to enable and disable the device. During normal operation, $\overline{CS}$ should be low. Although the use of $\overline{CS}$ is not necessary to synchronize a data transfer, it can be brought high between conversions to coordinate the data transfer of several devices sharing the same bus.

When $\overline{CS}$ is brought high, the serial-data output is immediately brought to the high-impedance state, releasing its output data line to other devices that may share it. After an internally generated debounce time, I/O CLOCK is inhibited, thus preventing any further change in the internal state.

When $\overline{CS}$ is subsequently brought low again, the device is reset. $\overline{CS}$ must be held low for an internal debounce time before the reset operation takes effect. After $\overline{CS}$ is debounced low, I/O CLOCK must remain inactive (low) for a minimum time before a new I/O cycle can start.

$\overline{CS}$ can be used to interrupt any ongoing data transfer or any ongoing conversion. If $\overline{CS}$ is debounced low long enough before the end of the current conversion cycle, the previous conversion result is saved in the internal output buffer and shifted out during the next I/O cycle.

power-down features

When a binary address of 1110 is clocked into the input data register during the first four I/O CLOCK cycles, the power-down mode is selected. Power down is activated on the falling edge of the fourth I/O CLOCK pulse.

During power down, all internal circuitry is put in a low-current standby mode. No conversions are performed, and the internal output buffer keeps the previous conversion cycle data results, provided that all digital inputs are held above V_{CC} – 0.5 V or below 0.5 V. The I/O logic remains active so the current I/O cycle must be completed even when the power-down mode is selected. Upon power-on reset and before the first I/O cycle, the converter normally begins in the power-down mode. The device remains in the power-down mode until a valid (other than 1110) input address is clocked in. Upon completion of that I/O cycle, a normal conversion is performed with the results being shifted out during the next I/O cycle.

analog input, test, and power-down mode

The 11 analog inputs, three internal voltages, and power-down mode are selected by the input multiplexer according to the input addresses shown in Tables 2, 3, and 4. The input multiplexer is a break-before-make type to reduce input-to-input noise rejection resulting from channel switching. Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK and continues for the remaining I/O CLOCK pulses. The sample is held

detailed description (continued)

analog input, test, and power-down mode (continued)

on the falling edge of the last I/O CLOCK pulse. The three internal test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

Table 1. Input-Register Format

FUNCTION SELECT	INPUT DATA BYTE							
	ADDRESS BITS				L1	L0	LSBF	BIP
	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Select input channel								
AIN0	0	0	0	0				
AIN1	0	0	0	1				
AIN2	0	0	1	0				
AIN3	0	0	1	1				
AIN4	0	1	0	0				
AIN5	0	1	0	1				
AIN6	0	1	1	0				
AIN7	0	1	1	1				
AIN8	1	0	0	0				
AIN9	1	0	0	1				
AIN10	1	0	1	0				
Select test voltage								
$(V_{ref+} - V_{ref-})/2$	1	0	1	1				
V_{ref-}	1	1	0	0				
V_{ref+}	1	1	0	1				
Software power down	1	1	1	0				
Output data length								
8 bits					0	1		
12 bits					X	0		
16 bits					1	1		
Output data format								
MSB first							0	
LSB first							1	
Unipolar (binary)								0
Bipolar (2s complement)								1

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO DATA INPUT	
	BINARY	HEX
AIN0	0000	0
AIN1	0001	1
AIN2	0010	2
AIN3	0011	3
AIN4	0100	4
AIN5	0101	5
AIN6	0110	6
AIN7	0111	7
AIN8	1000	8
AIN9	1001	9
AIN10	1010	A

detailed description (continued)

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED†	VALUE SHIFTED INTO DATA INPUT		UNIPOLAR OUTPUT RESULT (HEX)‡
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

† V_{ref+} is the voltage applied to REF+, and V_{ref-} is the voltage applied to REF–.
‡ The output results shown are the ideal values and may vary with the reference stability and with internal offsets.

Table 4. Power-Down-Select Address

INPUT COMMAND	VALUE SHIFTED INTO DATA INPUT		RESULT
	BINARY	HEX	
Power down	1110	E	$I_{CC} \leq 25\ \mu A$

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, 12 capacitors are examined separately until all 12 bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 4096). Node 4096 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 4096-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 4096-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 2048-weight capacitor, the 1024-weight capacitor, and so forth, down the line until all bits are determined. With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

reference voltage inputs

There are two reference inputs used with the device, the voltages applied to the REF+ and REF– terminals. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading, respectively. These voltages and the analog input should not exceed the positive supply or be lower than ground consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ terminal voltage and at zero when the input signal is equal to or lower than REF– terminal voltage.

detailed description (continued)

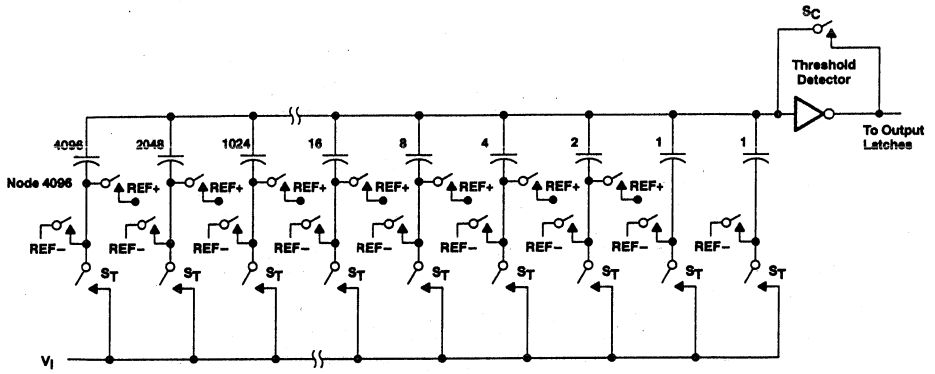


Figure 1. Simplified Model of the Successive-Approximation System

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 6.5 V
Input voltage range, V_I (any input) ..... −0.3 V to V_{CC} + 0.3 V
Output voltage range ..... −0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+} ..... V_{CC} + 0.1 V
Negative reference voltage, V_{ref-} ..... −0.1 V
Peak input current (any input) ..... ±20 mA
Peak total input current (all inputs) ..... ±30 mA
Operating free-air temperature range: TLC2543C ..... 0°C to 70°C
TLC2543I ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)			0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	V_{CC}+0.1	V
Analog input voltage (see Note 2)		0		V_{CC}	V
High-level control input voltage, V_{IH}	V_{CC} = 4.5 V to 5.5 V	2			V
Low-level control input voltage, V_{IL}	V_{CC} = 4.5 V to 5.5 V			0.8	V
Clock frequency at I/O CLOCK		0		4.1	MHz
Setup time, address bits at DATA INPUT before I/O CLOCK↑, $t_{su(A)}$ (see Figure 5)		100			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$ (see Figure 5)		0			ns
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(\overline{CS})}$ (see Figure 6)		0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(\overline{CS})}$ (see Note 3 and Figure 6)		1.425			µs
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$		190			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$		190			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 4 and Figure 7)				1	µs
Transition time, DATA INPUT and $\overline{CS}$, $t_{t(\overline{CS})}$				10	µs
Operating free-air temperature, T_A	TLC2543C	0		70	°C
	TLC2543I	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000).

3. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for a setup time after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 4.5$ V to 5.5 V, I/O CLOCK frequency = 4.1 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_{OH} = –1.6 mA	2.4			V
			V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –20 μA	V_{CC}–0.1			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 20 μA			0.1	
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}		1	2.5	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}		1	–2.5	
I_{IH}	High-level input current		$V_I = V_{CC}$			1	2.5	μA
I_{IL}	Low-level input current		V_I = 0			1	–2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1	2.5	mA
$I_{CC(PD)}$	Power-down current		For all digital inputs, $0 \le V_I \le 0.5$ V or $V_I \ge V_{CC} - 0.5$ V			4	25	μA
	Selected channel leakage current		Selected channel at V_{CC},	Unselected channel at 0 V			1	μA
			Selected channel at 0 V,	Unselected channel at V_{CC}			–1	
	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND		1	2.5	μA
C_i	Input capacitance	Analog inputs				30	60	pF
		Control inputs				5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

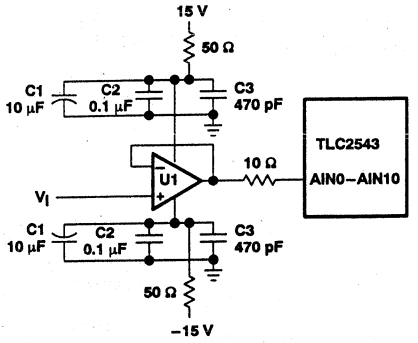
operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{ref+} = 4.5 V to 5.5 V, I/O CLOCK frequency = 4.1 MHz

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error (see Note 6)	See Figure 2			±1	LSB
	Differential linearity error	See Figure 2			±1	LSB
	Offset error (see Note 7)	See Note 2 and Figure 2			±1.5	LSB
	Gain error (see Note 7)	See Note 2 and Figure 2			±1	LSB
	Total unadjusted error (see Note 8)				±1.75	LSB
	Self-test output code (see Table 3 and Note 9)	DATA INPUT = 1011		2048		
		DATA INPUT = 1100		0		
		DATA INPUT = 1101		4095		
t_{conv}	Conversion time	See Figures 10–15		8	10	µs
t_c	Total cycle time (access, sample, and conversion)	See Figures 10–15 and Note 10			10 + total I/O CLOCK periods + $t_{d(I/O-EOC)}$	µs
t_{acq}	Channel acquisition time (sample)	See Figures 10–15 and Note 10	4		12	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 7	10			ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 7			150	ns
$t_{d(I/O-EOC)}$	Delay time, last I/O CLOCK↓ to EOC↓	See Figure 8		1.5	2.2	µs
$t_{d(EOC-DATA)}$	Delay time, EOC↑ to DATA OUT (MSB/LSB)	See Figure 9			100	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB/LSB driven)	See Figure 4		0.7	1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 4		70	150	ns
$t_{r(EOC)}$	Rise time, EOC	See Figure 9		15	50	ns
$t_{f(EOC)}$	Fall time, EOC	See Figure 8		15	50	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 7		15	50	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 7		15	50	ns
$t_{d(I/O-\overline{CS})}$	Delay time, last I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 11)				5	µs

† All typical values are at T_A = 25°C.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000).
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep value at the offset point.
8. Total unadjusted error comprises linearity, zero, and full-scale errors.
9. Both the input address and the output codes are expressed in positive logic.
10. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 7).
11. Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a setup time. $\overline{CS}$ must be taken low at ≤ 5 µs of the 10th I/O CLOCK falling edge to assure a conversion is aborted. Between 5 µs and 10 µs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.

PARAMETER MEASUREMENT INFORMATION



LOCATION	DESCRIPTION	PART NUMBER
U1	OP27	—
C1	10-μF 35-V tantalum capacitor	—
C2	0.1-μF ceramic NPO SMD capacitor	AVX 12105C104KA105 or equivalent
C3	470-pF porcelain high-Q SMD capacitor	Johanson 201S420471JG4L or equivalent

Figure 2. Analog Input Buffer to Analog Inputs AIN0–AIN10

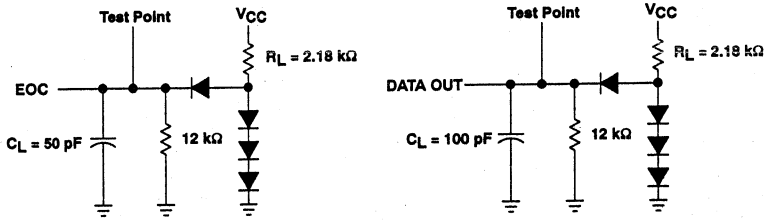


Figure 3. Load Circuits

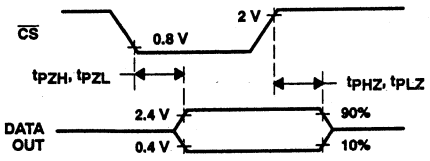


Figure 4. DATA OUT to HI-Z Voltage Waveforms

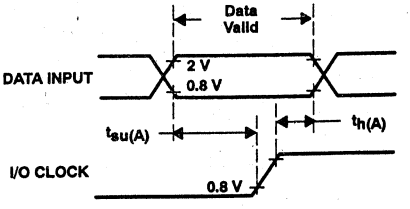


Figure 5. DATA INPUT and I/O CLOCK Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

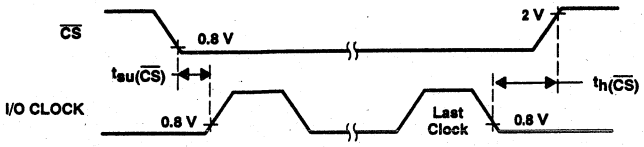


Figure 6. $\overline{CS}$ and I/O CLOCK Voltage Waveforms†

† To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

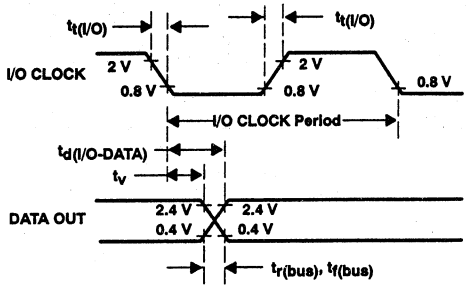


Figure 7. I/O CLOCK and DATA OUT Voltage Waveforms

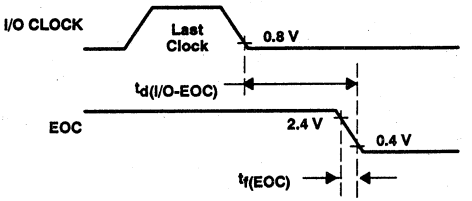


Figure 8. I/O CLOCK and EOC Voltage Waveforms

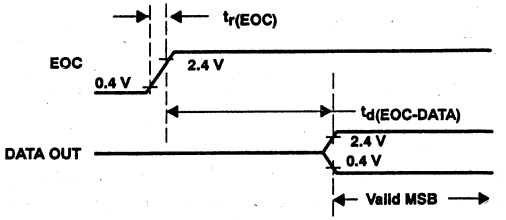


Figure 9. EOC and DATA OUT Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

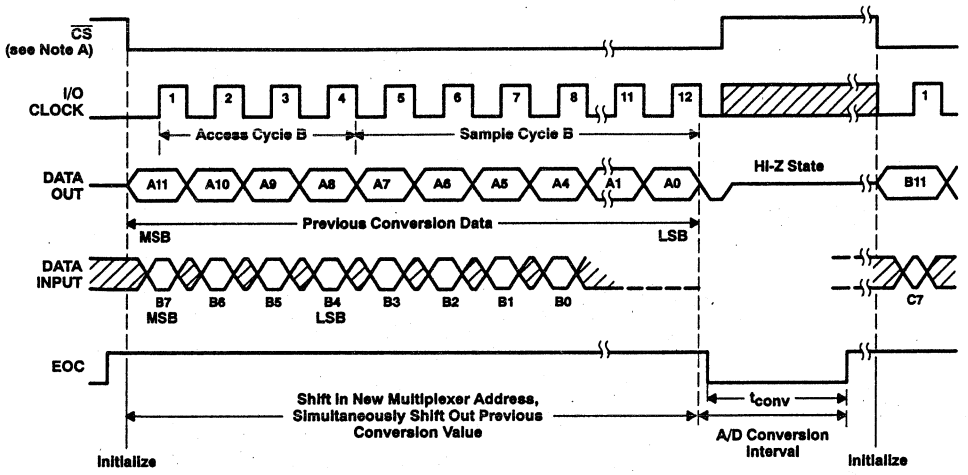


Figure 10. Timing for 12-Clock Transfer Using $\overline{CS}$ With MSB First

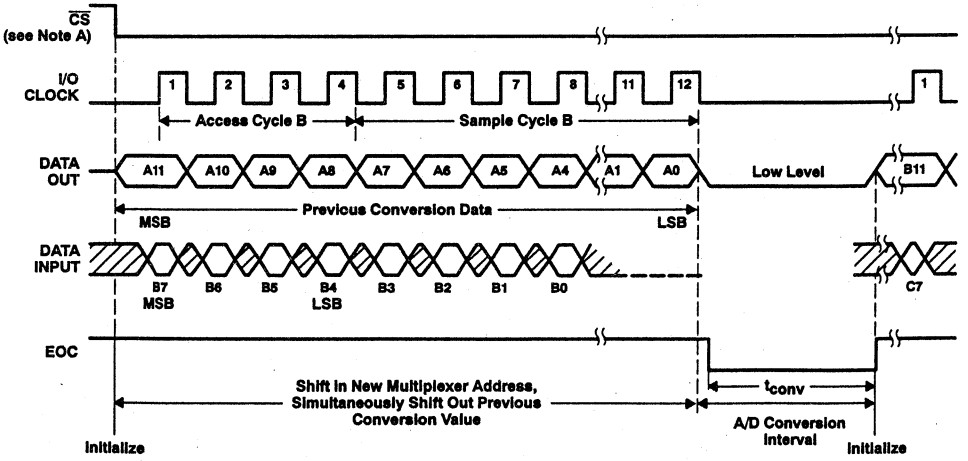


Figure 11. Timing for 12-Clock Transfer Not Using $\overline{CS}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

PARAMETER MEASUREMENT INFORMATION

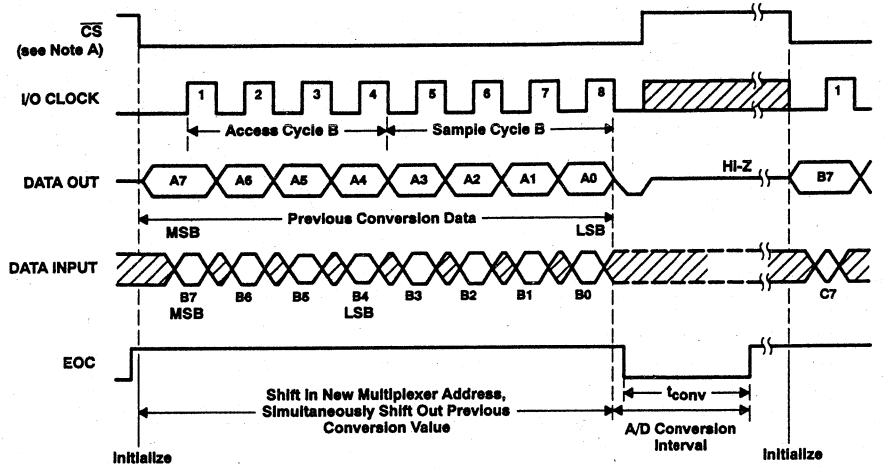


Figure 12. Timing for 8-Clock Transfer Using $\overline{CS}$ With MSB First

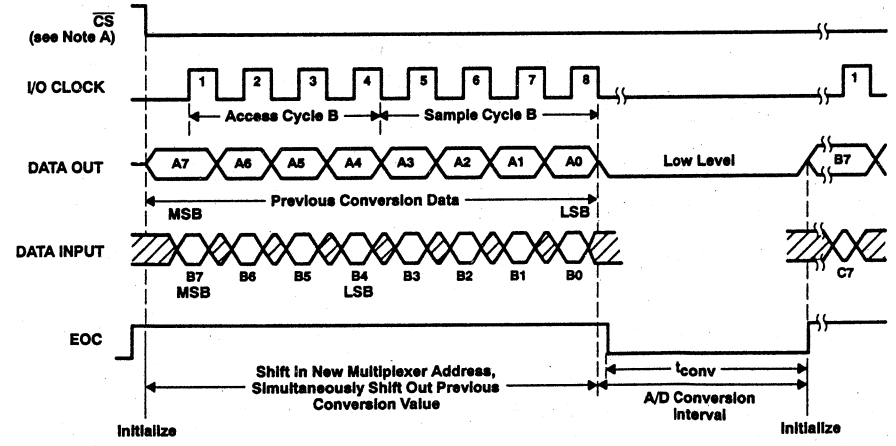


Figure 13. Timing for 8-Clock Transfer Not Using $\overline{CS}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

PARAMETER MEASUREMENT INFORMATION

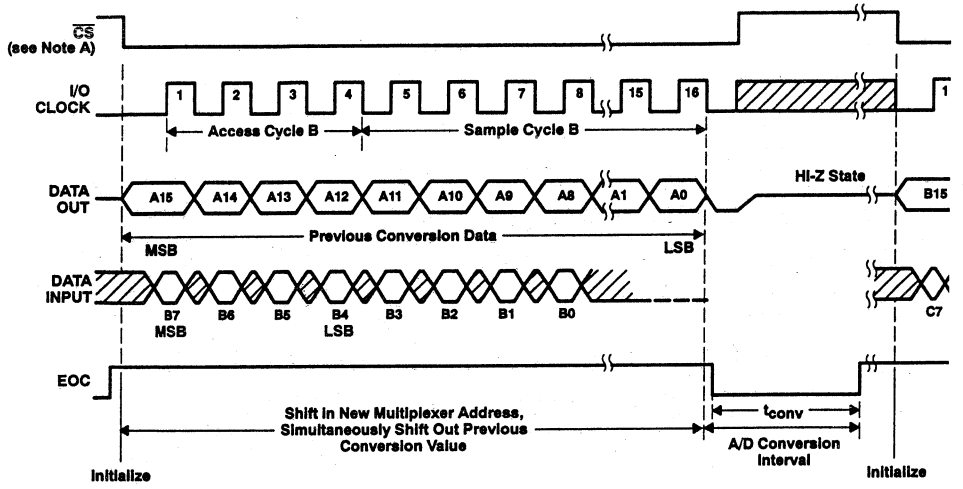


Figure 14. Timing for 16-Clock Transfer Using $\overline{CS}$ With MSB First

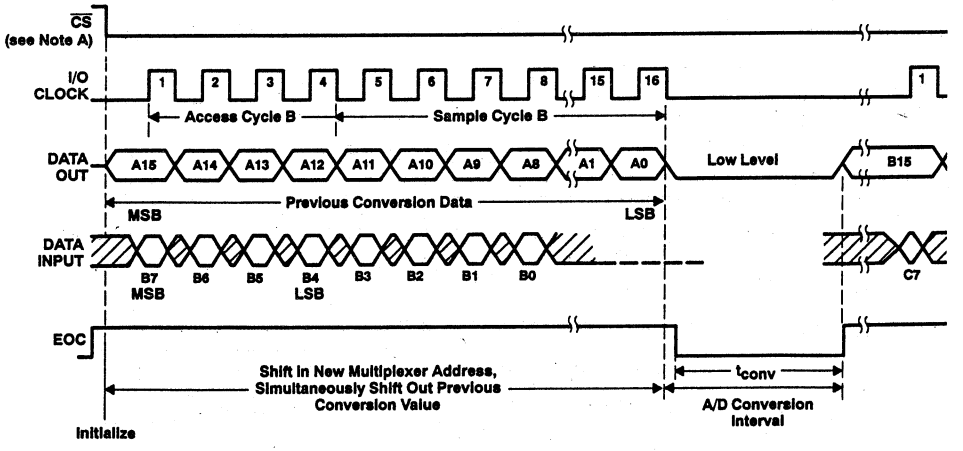
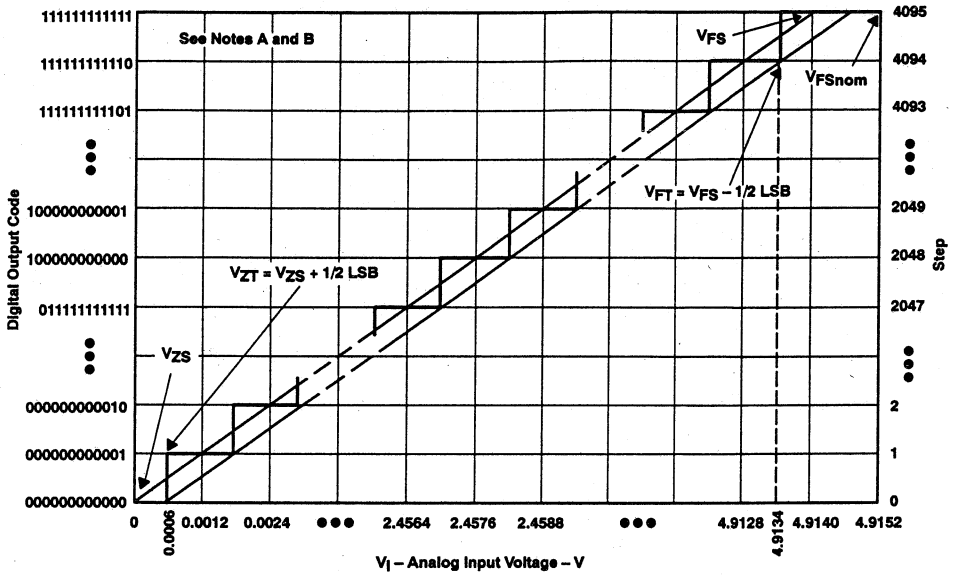


Figure 15. Timing for 16-Clock Transfer Not Using $\overline{CS}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0006 V and the transition to full scale (V_{FT}) is 4.9134 V. 1 LSB = 1.2 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 16. Ideal Conversion Characteristics

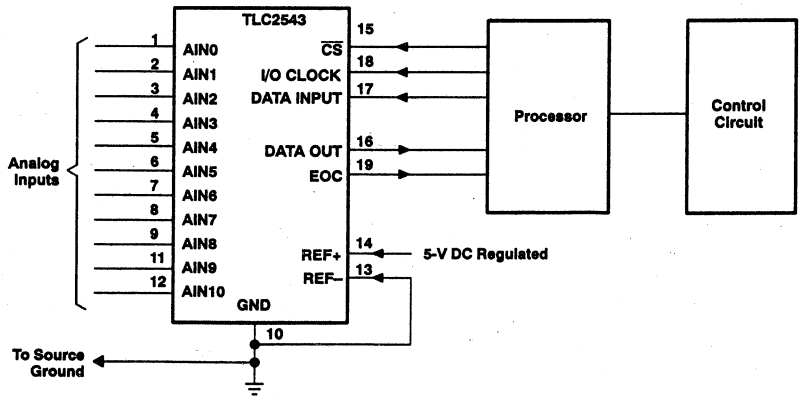
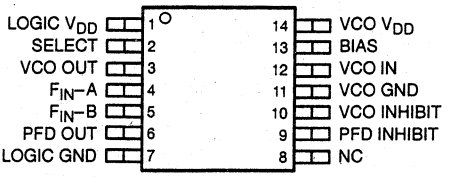


Figure 17. Serial Interface

- **VCO Section:**
  - **Complete Oscillation Using Only an External Resistor**
  - **Maximum Oscillation Frequency:**
    - **32 MHz Min at V_{DD} = 5 V, T_A = 25°C**
    - **15 MHz Min at V_{DD} = 3 V, T_A = 25°C**
  - **Output Frequency . . . ×1 and ×1/2 Selectable**
- **PFD Section:**
  - **High Speed, Edge Triggered With Internal Charge Pump**
- **Independent VCO, PFD Power Down Mode**
- **Thin Small Outline Package (14 pin)**
- **1 micron CMOS**
- **Operating Temperature . . . –20°C to 75°C**

PW PACKAGE
(TOP VIEW)

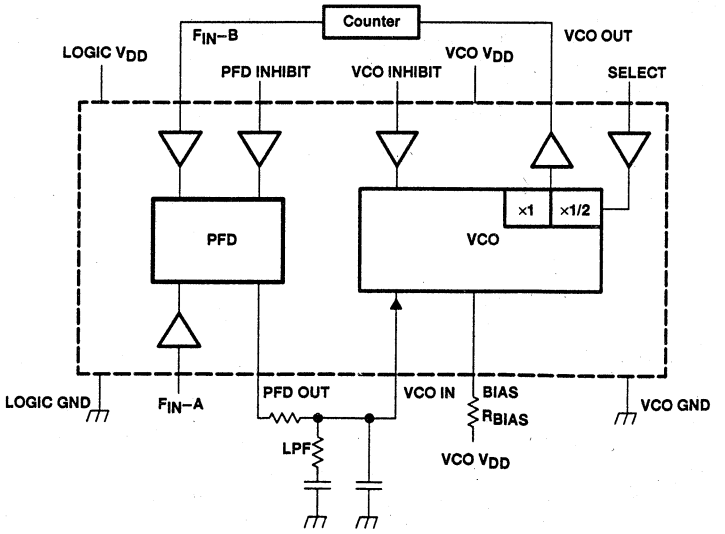


NC – No internal connection

description

The TLC2932I is designed for phase-locked-loop (PLL) systems and is composed of a voltage controlled oscillator (VCO) and edge trigger typed phase frequency detector (PFD). The oscillation frequency range of the VCO is set by an external resistor, as shown in the typical characteristics section. The VCO has a 1/2 frequency divider at the output stage. The high speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. Both the VCO and the PFD have inhibit functions, which can be used as a power down mode. Because of its high speed and stable oscillation capability, it is suitable for high performance PLL blocks.

PLL block diagram and simplified typical application



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
F_{IN}–A	4	I	Input reference frequency $f_{(REF\ IN)}$ is applied to F_{IN}–A.
F_{IN}–B	5	I	Input for VCO external counter output frequency $f_{(FIN-B)}$. F_{IN}–B is nominally provided from the external counter, see PLL block diagram, page 1.
LOGIC GND	7		GND for the internal logic.
LOGIC V_{DD}	1		Power supply for the internal logic. This power supply should be separate from VCO V_{DD} for stable oscillation.
NC	8		No internal connection.
PFD INHIBIT	9	I	PFD inhibit control. When PFD INHIBIT is high, PFD output is in the high impedance state, see Table 3.
PFD OUT	6	O	PFD output. When the PFD INHIBIT is high, PFD output is in the high impedance state.
BIAS	13	I	Bias supply. An external resistor between V_{DD} and BIAS supplies bias for adjusting the oscillation frequency range.
SELECT	2	I	VCO output frequency select. When SELECT is high, the VCO output frequency is divided by 1/2 and when low, the output frequency is ×1, see Table 1.
VCO IN	12	I	VCO control voltage input. Nominally the external loop filter output is connected to VCO IN to control VCO oscillation.
VCO INHIBIT	10	I	VCO inhibit control. When VCO INHIBIT is high, VCO OUT is low, see Table 3.
VCO GND	11		GND for VCO.
VCO OUT	3	O	VCO output. When the VCO INHIBIT is high, VCO output is low.
VCO V_{DD}	14		Power supply for VCO. This power supply should be separated from LOGIC V_{DD} for proper operation.

detailed description

VCO oscillation frequency

The VCO oscillation frequency is determined by an external resistor (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depends on this resistor value. The bias resistor value for the minimum temperature coefficient is nominally 3.3 kΩ with 3-V V_{DD} and nominally 2.2 kΩ with 5-V V_{DD}. For the lock frequency range, refer to the typical characteristics section. Figure 1 shows the typical frequency variation and VCO control voltage.

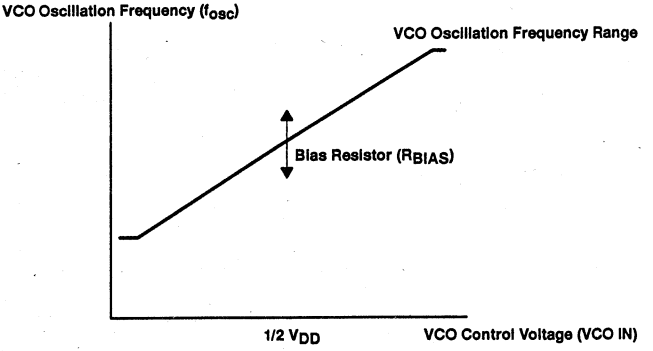


Figure 1. VCO Oscillation Frequency

VCO output frequency 1/2 divider

The TLC2932I VCO output multiplexes the f_{OSC} and 1/2 f_{OSC} frequencies. For normal operation, the 1/2 f_{OSC} output is recommended to minimize VCO output jitter. Refer to Table 1 for SELECT terminal control.

Table 1. VCO Output 1/2 Divider Function

SELECT	VCO OUTPUT
Low	f_{OSC}
High	1/2 f_{OSC}

VCO inhibit function

The VCO has an externally controlled inhibit function which intializes the VCO output. The VCO oscillation is stopped during a high level on the VCO INHIBIT terminal, so this also can be used as the power down mode. The VCO output maintains a low level during the power down mode, refer to Table 2.

Table 2. VCO Inhibit Function

VCO INHIBIT	VCO OSCILLATOR	VCO OUTPUT
Low	Active	Active
High	Stop	Low level

PFD operation

The phase frequency detector (PFD) is a high-speed edge-triggered detector with an internal charge pump. It detects the phase difference between two frequency inputs supplied to F_{IN}–A and F_{IN}–B. Nominally the reference is supplied to F_{IN}–A, and the frequency from the external counter output is fed to F_{IN}–B, refer to Figure 2.

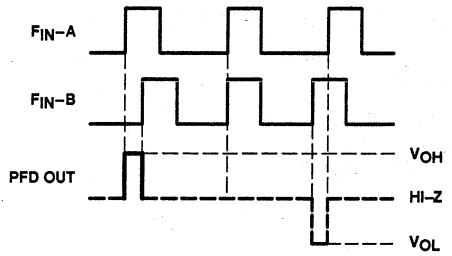


Figure 2. PFD Function Timing Chart

PFD output control

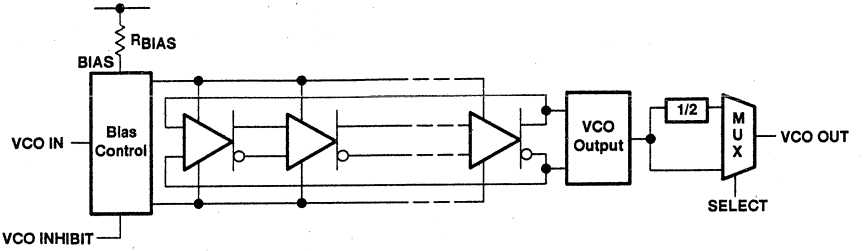
The PFD output can be placed in a high impedance state by a high level on the PFD INHIBIT terminal and the PFD stops phase detection. A high level also can be used as the power down mode for the PFD, refer to Table 3.

Table 3. VCO Output Control Function

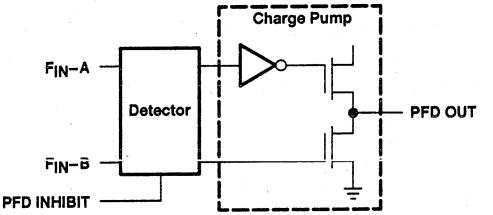
PFD INHIBIT	DETECTION	PFD OUTPUT
Low	Active	Active
High	Stop	Z

schematics

VCO block schematic



PFD block schematic



absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage (each supply), V_{DD} (see Note 1)	7 V
Input voltage range (each input), V_{IN} (see Note 1)	−0.5 V to V_{DD} + 0.5 V
Input current (each input), I_{IN}	±20 mA
Output current (each output) I_O	±20 mA
Continuous total dissipation, P_D	700 mW
Operating free-air temperature range, T_A (see Note 2)	−20°C to 75°C
Storage tempeature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 5.6 mW/°C.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (each supply, see Note 3)	V_{DD} = 3 V	2.85	3	3.15	V
	V_{DD} = 5 V	4.75	5	5.25	
Input voltage, V_{IN} (inputs except VCO IN)		0		V_{DD}	V
Output current, I_O (each output)		0		±2	mA
VCO control voltage at VCO IN		0.9		V_{DD}	V
Lock frequency (×1 output)	V_{DD} = 3 V	14		21	MHz
	V_{DD} = 5 V	22		50	
Lock frequency (×1/2 output)	V_{DD} = 3 V	7		10.5	MHz
	V_{DD} = 5 V	11		25	
Bias resistor, R_{BIAS}	V_{DD} = 3 V	2.2	3.3	4.3	kΩ
	V_{DD} = 5 V	1.5	2.2	3.3	
Operating free-air temperature, T_A		–20		75	°C

NOTE 3: It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) should be at the same voltage and are separate from each other.

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 MA			0.3	V
V_{IT}	Input threshold voltage at SELECT, VCO INHIBIT		0.9	1.5	2.1	V
I_I	Input current at SELECT, VCO INHIBIT	V_I = V_{DD} or GND			±1	µA
$Z_{i(VCO\ IN)}$	Input impedance	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 4		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current	See Note 5		5	15	mA

NOTES: 4. Current into LOGIC V_{DD}, VCO V_{DD}, when VCO INHIBIT = V_{DD}, PFD is inhibited.
5. Current into LOGIC V_{DD}, VCO V_{DD}, when VCO IN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCO INHIBIT = GND, and PFD is inhibited.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	Output current (high-impedance)	PFD INHIBIT = high, V_I = V_{DD} or GND			±1	µA
V_{IH}	High-level input voltage at F_{IN}–A, F_{IN}–B		2.7			V
V_{IL}	Low-level input voltage at F_{IN}–A, F_{IN}–B				0.5	V
V_{IT}	Input threshold voltage at PFD INHIBIT		0.9	1.5	2.1	V
C_i	Input capacitance at F_{IN}–A, F_{IN}–B			5		pF
Z_i	Input impedance at F_{IN}–A, F_{IN}–B		45	10	55	MΩ
$I_{DD(Z)}$	PFD supply current (high-impedance)	See Note 6		0.01	1	µA
$I_{DD(PFD)}$	PFD supply current	See Note 7		0.1	1.5	mA

NOTES: 6. Current into LOGIC V_{DD}, when F_{IN}–A, F_{IN}–B = GND, PFD INHIBIT = V_{DD}, no load, and VCO OUT is inhibited.
7. Current into LOGIC V_{DD}, when F_{IN}–A, F_{IN}–B = 1 MHz ($V_{I(PP)}$ = 3 V, rectangular wave), NC = GND, no load, and VCO OUT is inhibited.

operating characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}	15	19	23	MHz
$t_{s(fosc)}$	Time to stable oscillation	See Note 8			10	µs
t_r	Rise time	C_L = 15 pF, See Figure 3		7	14	ns
		C_L = 50 pF, See Figure 3		14		
t_f	Fall time	C_L = 15 pF, See Figure 3		6	12	ns
		C_L = 50 pF, See Figure 3		14		
	Duty cycle at VCO OUT	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD},	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		0.04		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1.5 V, V_{DD} = 2.85 V to 3.15 V		0.02		%/mV

NOTE 8: The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		20			MHz
t_{PLZ}	PFD output transition time to high-impedance state	See Figures 4 and 5 and Table 4		21	50	ns
t_{PHZ}				23	50	
t_{PZL}	PFD output transition time to active state			11	30	ns
t_{PZH}				10	30	
t_r	Rise time	C_L = 15 pF, See Figure 4		2.3	10	ns
t_f	Fall time			2.1	10	ns

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −2 mA	4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 MA			0.5	V
V_{IT}	Input threshold voltage at SELECT, VCO INHIBIT		1.5	2.5	3.5	V
I_I	Input current at SELECT, VCO INHIBIT	$V_I = V_{DD}$ or GND			±1	µA
$Z_{i(VCO\ IN)}$	Input impedance	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 4		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current	See Note 9		15	35	mA

NOTES: 4. Current into LOGIC V_{DD}, and VCO V_{DD}, when VCO INHIBIT = V_{DD}, and PFD is inhibited.
9. Current into LOGIC V_{DD}, and VCO V_{DD}, when VCO IN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCO INHIBIT = GND, and PFD is inhibited.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2 mA	4.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	Output current (high-impedance)	PFD INHIBIT = high, $V_I = V_{DD}$ or GND			±1	µA
V_{IH}	High-level input voltage at F_{IN}–A, F_{IN}–B		4.5			V
V_{IL}	Low-level input voltage at F_{IN}–A, F_{IN}–B				1	V
V_{IT}	Input threshold voltage at PFD INHIBIT		1.5	2.5	3.5	V
C_i	Input capacitance at F_{IN}–A, F_{IN}–B			5		pF
Z_i	Input impedance at F_{IN}–A, F_{IN}–B		45	10	55	MΩ
$I_{DD(Z)}$	PFD supply current (high-impedance)	See Note 6		0.01	1	µA
$I_{DD(PFD)}$	PFD supply current	See Note 10		0.15	3	mA

NOTES: 6. Current into LOGIC V_{DD}, when F_{IN}–A, F_{IN}–B = GND, PFD INHIBIT = V_{DD}, no load, and VCO OUT is inhibited.
10. Current into LOGIC V_{DD}, when F_{IN}–A, F_{IN}–B = 1 MHz ($V_{I(PP)}$ = 5 V, rectangular wave), PFD INHIBIT = GND, no load, and VCO OUT is inhibited.

operating characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD}	32	41	50	MHz
$t_{s(fosc)}$	Time to stable oscillation	See Note 8			10	μs
t_r	Rise time	C_L = 15 pF, See Figure 3		5.5	10	ns
		C_L = 50 pF, See Figure 3		8		
t_f	Fall time	C_L = 15 pF, See Figure 3		5	10	ns
		C_L = 50 pF, See Figure 3		6		
	Duty cycle at VCO OUT	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD},	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		0.06		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 2.5 V, V_{DD} = 4.75 V to 5.25 V		0.006		%/mV

NOTE 8: The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		40			MHz
t_{PLZ}	PFD output transition time to high-impedance state	See Figures 4 and 5 and Table 4		21	40	ns
t_{PHZ}				20	40	
t_{PZL}	PFD output transition time to active state			7.3	20	ns
t_{PZH}				6.5	20	
t_r	Rise time	C_L = 15 pF, See Figure 4		2.3	10	ns
t_f	Fall time			1.7	10	ns

PARAMETER MEASUREMENT INFORMATION

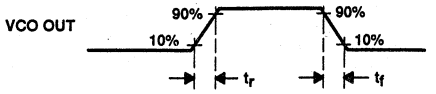
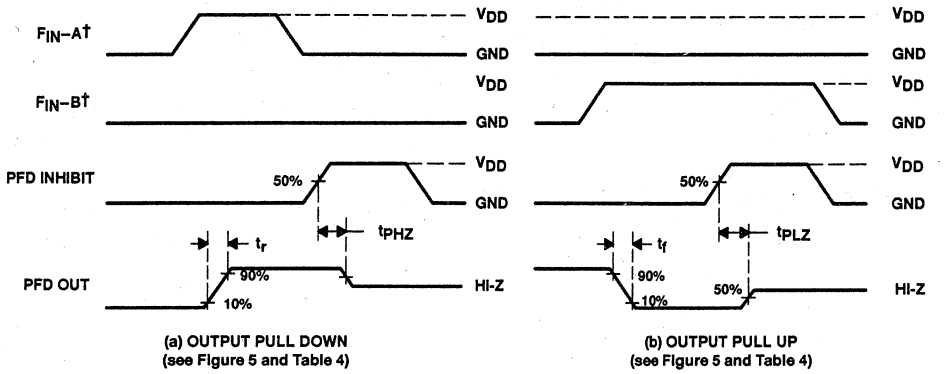
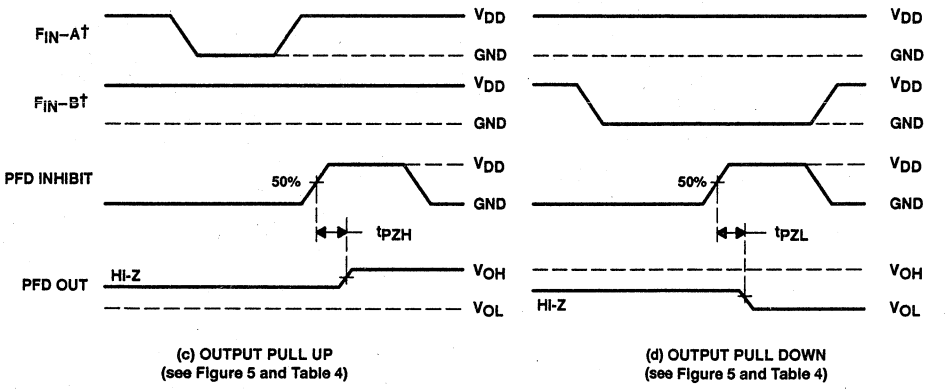


Figure 3. VCO Output Voltage Waveform



(a) OUTPUT PULL DOWN
(see Figure 5 and Table 4)

(b) OUTPUT PULL UP
(see Figure 5 and Table 4)



(c) OUTPUT PULL UP
(see Figure 5 and Table 4)

(d) OUTPUT PULL DOWN
(see Figure 5 and Table 4)

Figure 4. PFD Output Voltage Waveform

† F_{IN}–A and F_{IN}–B are for reference phase only, not for timing.

PARAMETER MEASUREMENT INFORMATION

Table 4. PFD Output Test Conditions

PARAMETER	R_L	C_L	S_1	S_2
t_{PZH}	1 kΩ	15 pF	Open	Close
t_{PHZ}				
t_r				
t_{PZL}			Close	Open
t_{PLZ}				
t_f				

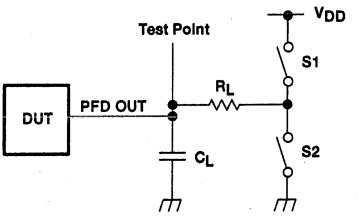


Figure 5. PFD Output Test Conditions

TYPICAL CHARACTERISTICS

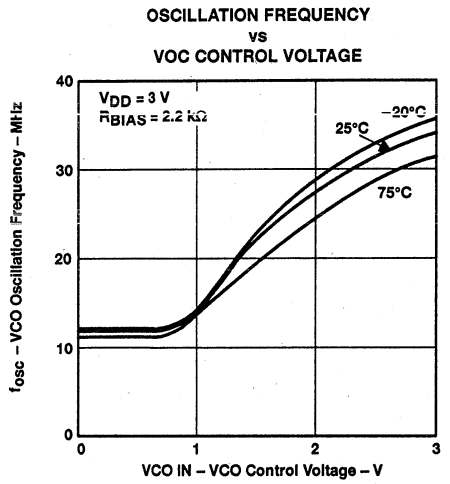


Figure 6

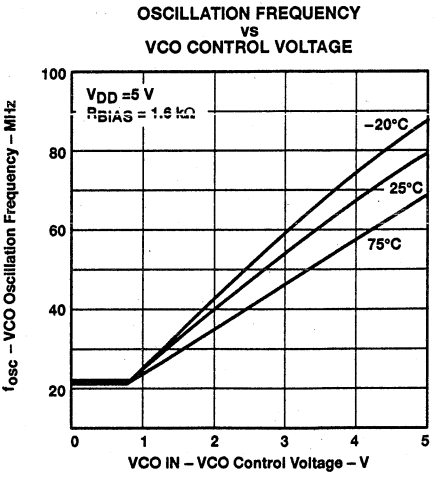


Figure 7

TYPICAL CHARACTERISTICS

OSCILLATION FREQUENCY
vs
VOC CONTROL VOLTAGE

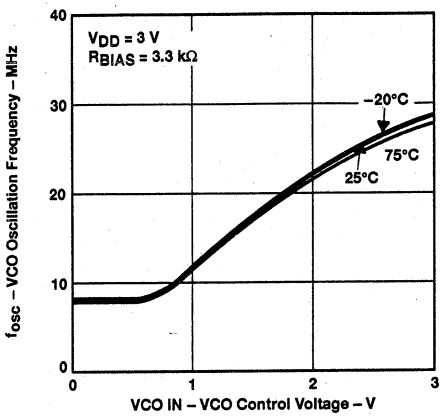


Figure 8

OSCILLATION FREQUENCY
vs
VOC CONTROL VOLTAGE

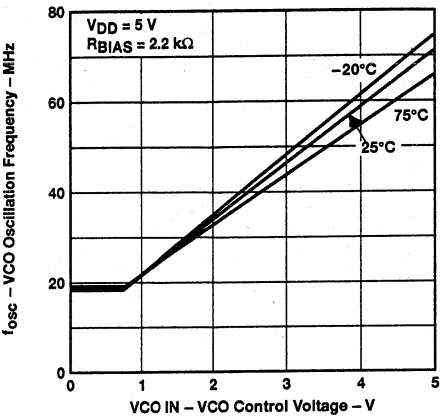


Figure 9

OSCILLATION FREQUENCY
vs
VOC CONTROL VOLTAGE

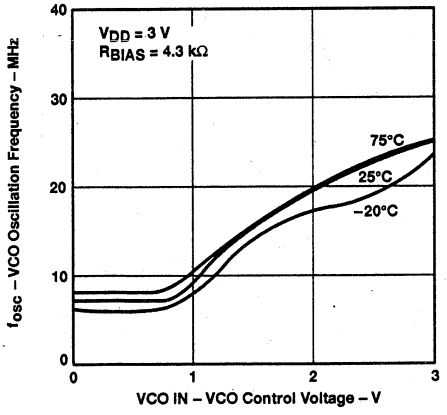


Figure 10

OSCILLATION FREQUENCY
vs
VOC CONTROL VOLTAGE

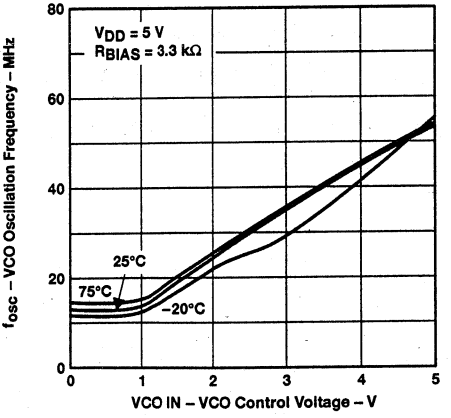


Figure 11

TYPICAL CHARACTERISTICS

OSCILLATION FREQUENCY
vs
BIAS RESISTOR

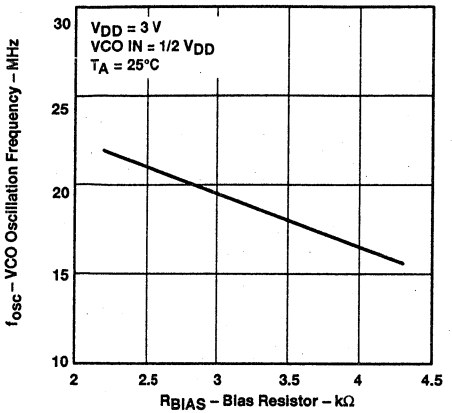


Figure 12

OSCILLATION FREQUENCY
vs
BIAS RESISTOR

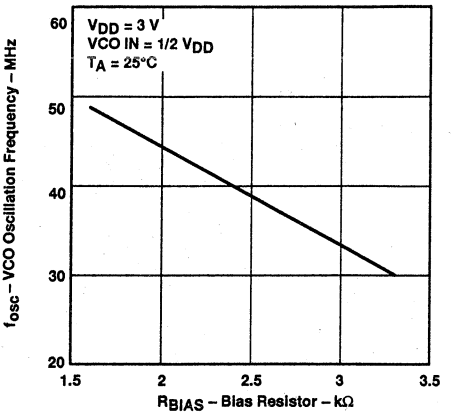


Figure 13

TEMPERATURE COEFFICIENT OF
OSCILLATION FREQUENCY
vs
BIAS RESISTOR

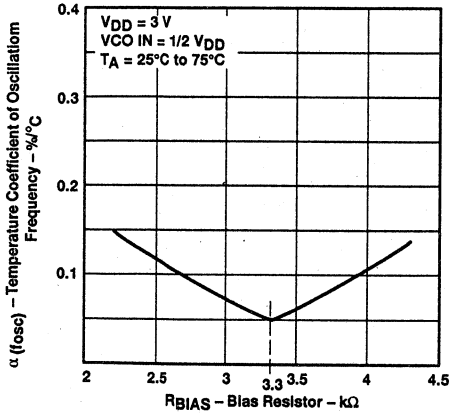


Figure 14

TEMPERATURE COEFFICIENT OF
OSCILLATION FREQUENCY
vs
BIAS RESISTOR

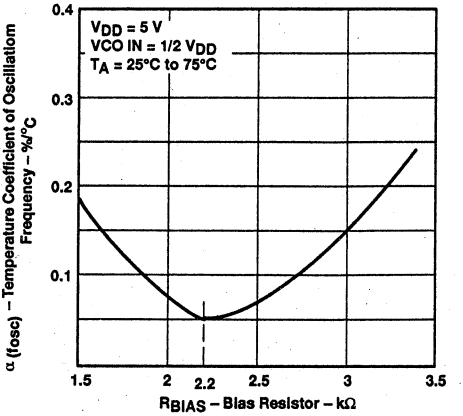


Figure 15

TYPICAL CHARACTERISTICS

OSCILLATION FREQUENCY
vs
VCO SUPPLY VOLTAGE

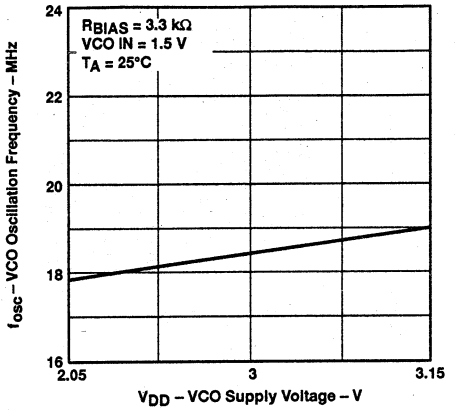


Figure 16

OSCILLATION FREQUENCY
vs
VCO SUPPLY VOLTAGE

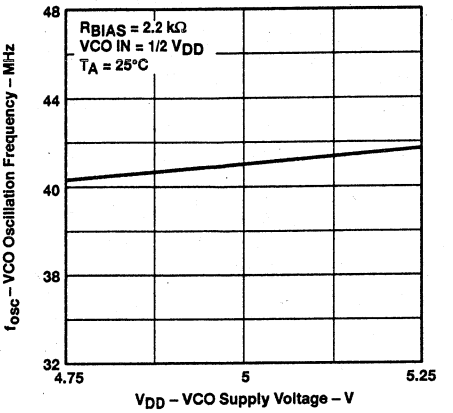


Figure 17

SUPPLY VOLTAGE COEFFICIENT OF
OSCILLATION FREQUENCY
vs
BIAS RESISTOR

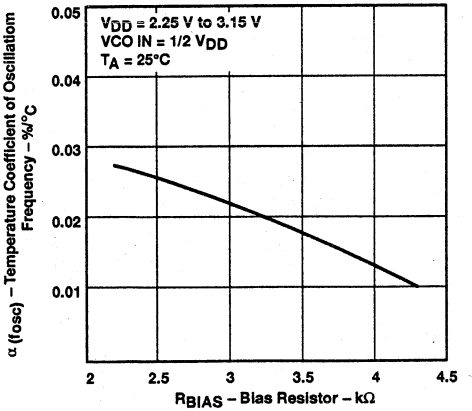


Figure 18

SUPPLY VOLTAGE COEFFICIENT OF
OSCILLATION FREQUENCY
vs
BIAS RESISTOR

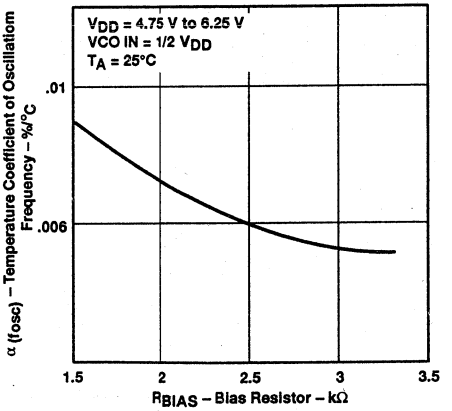


Figure 19

APPLICATION INFORMATION

RECOMMENDED LOCK FREQUENCY RANGE
(×1 OUTPUT)
vs
BIAS RESISTOR

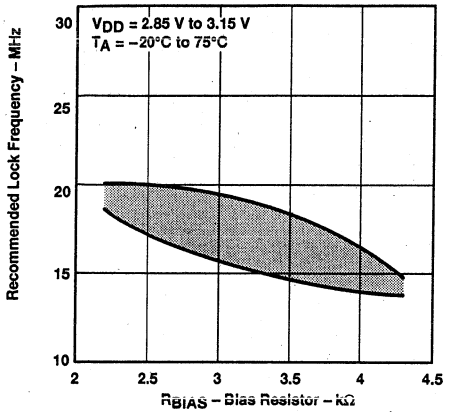


Figure 20

RECOMMENDED LOCK FREQUENCY RANGE
(×1 OUTPUT)
vs
BIAS RESISTOR

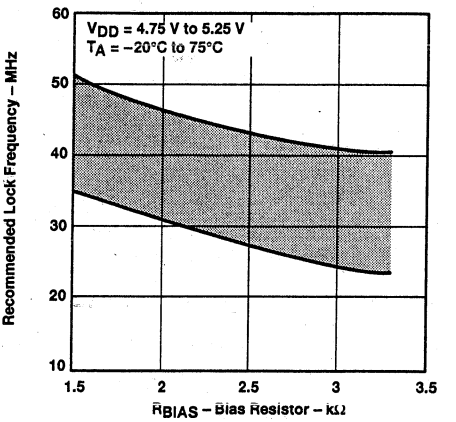


Figure 21

RECOMMENDED LOCK FREQUENCY RANGE
(×1/2 OUTPUT)
vs
BIAS RESISTOR

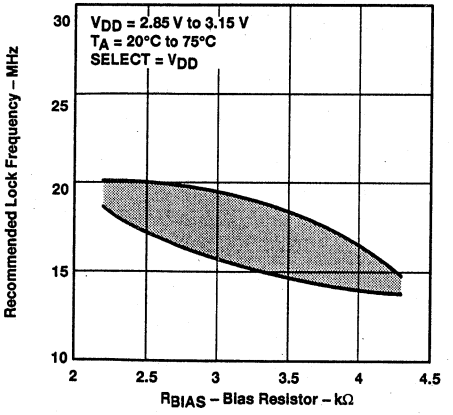


Figure 22

RECOMMENDED LOCK FREQUENCY RANGE
(×1/2 OUTPUT)
vs
BIAS RESISTOR

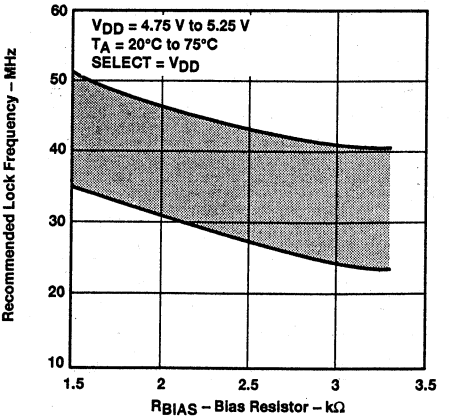


Figure 23

APPLICATION INFORMATION

gain of VCO and PFD

Figure 24 contains a PLL block diagram using the TLC2932 to examine specific gains. The K_ϕ, K_V, and N values depend on the frequency and application specific constants. K_f is defined by the selection of a type of LPF.

K_V : VCO gain (rad/s/V)
K_ϕ : PFD gain (V/rad)
K_f : LPF gain
K_N : divider gain (1/N)

external counter

When a large N counter is required by the application, there is a possibility that the PLL response will become slow due to the counter response delay time. In the case of a high frequency application, the counters delay time should be accounted for in the overall PLL design.

low pass filter (LPF)

Many excellent references are available that include detailed design information about LPFs. A lag-lead filter or active filter is often used. Examples of LPFs are shown in Figure 25.

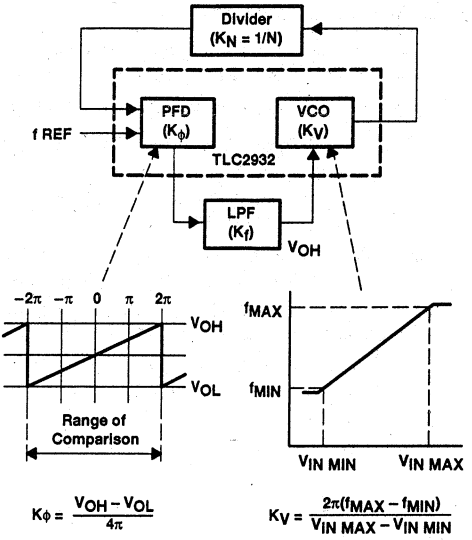


Figure 24. Example of a PLL Block Diagram

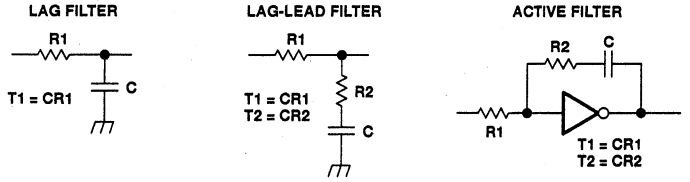


Figure 25. LPF Examples for PLL

APPLICATION INFORMATION

PCB layout considerations

The TLC2932I contains a high frequency analog oscillator; therefore, very careful bread boarding and PCB layout is required for evaluation.

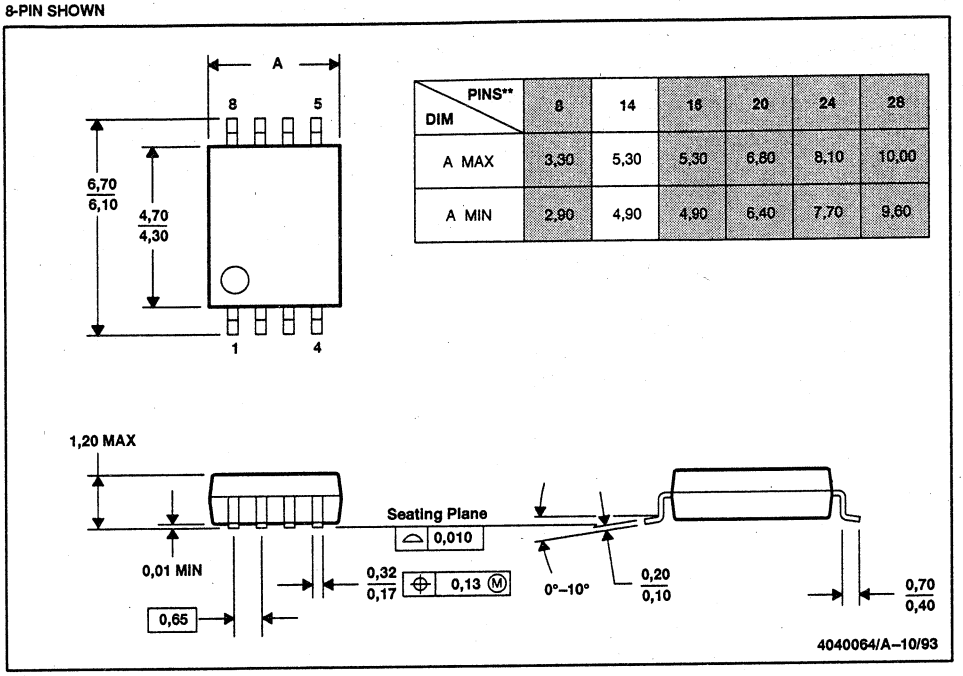
The following design recommendations benefit the TLC2932I user:

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- Logic V_{DD} and VCO V_{DD} should be separate PCB traces and connected to the best filtered supply point available in the system to minimize supply cross coupling.
- VCO V_{DD} to GND and LOGIC V_{DD} to GND should be decoupled with a 0.1-µF capacitor placed as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.1-µF capacitor.
- The no-connection (NC) terminal on the package should be connected to GND.

MECHANICAL DATA

PW (R-PDSO-G)** — **PLASTIC THIN SHRINK SMALL-OUTLINE PACKAGE**

8-PIN SHOWN



DIM \ PINS**	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,60	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

TLC320AD57C
Data Manual

Sigma-Delta Stereo Analog-to-Digital Converter

TEXAS INSTRUMENTS

1 Introduction

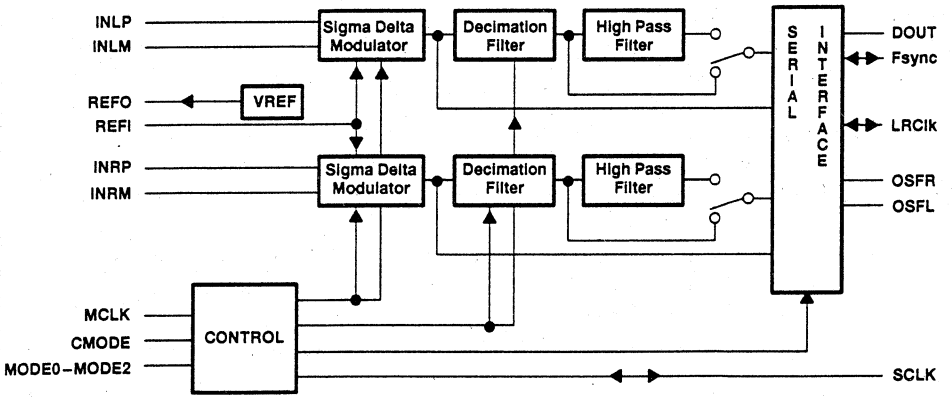
The TLC320AD57 provides high-resolution signal conversion from analog to digital using oversampling sigma delta technology. This device consists of two synchronous conversion paths. Also included is a decimation filter after the modulator as shown in the functional block diagram. Other functions provide analog filtering and on-chip timing and control.

A functional block diagram of the TLC320AD57 is included in Section 1.2. Each block is described in the detailed description section.

1.1 Features

- Single 5-V Power Supply
- Sample Rates up to 48 kHz
- 18-Bit Resolution
- Signal-to-Noise (EIAJ) of 97 dB
- Dynamic Range of 95 dB
- Total Signal-to-Noise+Distortion of 91 dB
- Internal Reference Voltage (V_{ref})
- Serial Port Interface
- Differential Architecture
- Power Dissipation of 200 mW. Power-Down Mode for Low-Power Applications
- One Micron Advanced LinEPIC1Z™ Process

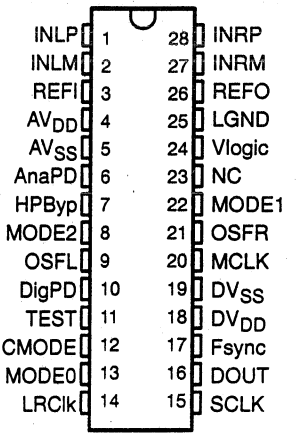
1.2 Functional Block Diagram



LinEPIC1Z is a trademark of Texas Instruments Incorporated.

1.3 Terminal Assignments

DWM PACKAGE
(TOP VIEW)



NC – No internal connection

1.4 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AnaPD	6	I	Analog power-down mode. The analog power-down mode disables the analog modulators. The single bit modulator outputs become invalid which renders the outputs of the digital filters invalid. When AnaPD is pulled low, normal operation of the device is resumed.
AV_{DD}	4	I	Analog supply
AV_{SS}	5	I	Analog ground
CMODE	12	I	Clock mode. CMODE is used to select between two methods of determining the master clock frequency. When high, the master clock input is 384× the conversion frequency. When low, the master clock input is 256× the conversion frequency.
DOUT	16	O	Data output. DOUT is used to transmit the sigma-delta audio ADC output data to a DSP serial port or other compatible serial interface and is synchronized to SCLK. This output is low when DigPD is high.
DV_{DD}	18	I	Digital supply
DV_{SS}	19	I	Digital ground
DigPD	10	I	Digital power-down mode. The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are brought to unasserted states. When DigPD is pulled low, normal operation of the device is resumed.
Fsync	17	I/O	Frame synchronization. Fsync is used to designate valid data from the ADC.
HPByp	7	I	High-pass filter bypass. When HPByp is high, the high-pass filter is bypassed. This allows dc analog signal conversion.
INLM	2	I	Inverting input to left analog input amplifier
INLP	1	I	Noninverting input to left analog input amplifier

1.4 Terminal Functions (Continued)

<table>
<tr><th colspan="2">TERMINAL
NAME NO.</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>INRM</td><td>27</td><td>I</td><td>Inerting input to right analog input amplifier</td></tr>
<tr><td>INRP</td><td>28</td><td>I</td><td>Noninverting input to right analog input amplifier</td></tr>
<tr><td>LGND</td><td>25</td><td>I</td><td>Logic power supply/ground for analog modulator</td></tr>
<tr><td>LRClk</td><td>14</td><td>I/O</td><td>Left/right clock. LRClk signifies whether the serial data is associated with the left channel ADC (when high) or the right channel ADC (when low). LRClk is low when DigPD is high.</td></tr>
<tr><td>MCLK</td><td>20</td><td>I</td><td>Master clock. MCLK is used to derive all of the key logic signals of the sigma-delta audio ADC. The nominal input frequency range is 18.432 MHz to 256 kHz.</td></tr>
<tr><td>MODE0–MODE2</td><td>8, 13, 22</td><td>I</td><td>Serial modes. MODE0–MODE2 configure this device for many different modes of operation. The different configurations are:
Master versus slave
16 bit versus 18 bit
MSB first versus LSB first
Slave: Fsync controlled versus Fsync high
Each of these modes is described in the serial interface section along with timing diagrams.
<table>
<tr><th>MODE
0 1 2</th><th>MASTER/
SLAVE</th><th>BITS</th><th>MSB/LSB
FIRST</th></tr>
<tr><td>0 0 0</td><td>slave</td><td>up to 18</td><td>MSB</td></tr>
<tr><td>0 0 1</td><td>slave</td><td>18</td><td>LSB</td></tr>
<tr><td>0 1 0</td><td>slave</td><td>up to 18</td><td>MSB</td></tr>
<tr><td>0 1 1</td><td>master</td><td>16</td><td>MSB</td></tr>
<tr><td>1 0 0</td><td>master</td><td>18</td><td>MSB</td></tr>
<tr><td>1 0 1</td><td>master</td><td>18</td><td>LSB</td></tr>
<tr><td>1 1 0</td><td>master</td><td>16</td><td>MSB</td></tr>
<tr><td>1 1 1</td><td>master</td><td>16</td><td>LSB</td></tr>
</table></td></tr>
<tr><td>OSFL/R</td><td>9, 21</td><td>O</td><td>Over scale flag left/right. If the left/right channel analog input exceeds the full scale input range for two consecutive conversions, this flag is set high for 4096 LRClk periods. OSFL/R is low when DigPD is high.</td></tr>
<tr><td>SCLK</td><td>15</td><td>I/O</td><td>Shift clock. SCLK is used to clock serial data out of the sigma-delta audio ADC. If configured as an output, SCLK stops clocking when DigPD is high.</td></tr>
<tr><td>TEST</td><td>11</td><td>I</td><td>Test mode. TEST should be low for normal operation.</td></tr>
<tr><td>REFI</td><td>3</td><td>I</td><td>Input voltage for modulator reference (normally connected to REFO, terminal 26).</td></tr>
<tr><td>REFO</td><td>26</td><td>I</td><td>Internal voltage reference</td></tr>
<tr><td>Vlogic</td><td>24</td><td>I</td><td>Logic power supply (5 V) for analog modulator</td></tr>
</table>

2 Detailed Description

2.1 Power Down and Reset Functions

2.1.1 Power Down

The power-down state is comprised of a separate digital and analog power down. The power consumption of each is detailed in the electrical characteristics section.

The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are set to an unasserted state. When the digital power-down terminal (DigPD) is pulled low, normal operation of the device is initiated.

In slave mode, the conversion process must synchronize to an input on the LRClk terminal as well as the SCLK terminal. Therefore, the conversion process is not initiated until the first rising edge of SCLK as well as the first rising edge of LRClk are detected after DigPD is pulled low. This synchronizes the conversion cycle; all conversions are performed at a fixed LRClk rate [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)] after the initial synchronization. After the digital power-down terminal is brought low, the output of the digital filters remains invalid for 50 LRClk cycles [see to Figures 2–1(a) and 2–1(b)].

In master mode, LRClk is an output; therefore, the conversion process initiates based on internal timing. The first valid data out occurs as shown in Figure 2–1(c).

The analog power-down mode disables the analog modulators. The single bit modulator outputs become invalid which renders the outputs of the digital filters invalid. When the analog power-down terminal is brought low, the modulators are brought back online; however, the outputs of the digital filters require 50 LRClk cycles for valid results.

2.1.2 Reset Function

The conversion process is not initiated until the first rising edge of SCLK as well as the first rising edge of LRClk are detected after DigPD is pulled low. This synchronizes the conversion cycle; all conversions are performed at a fixed LRClk rate [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)] after the initial synchronization.

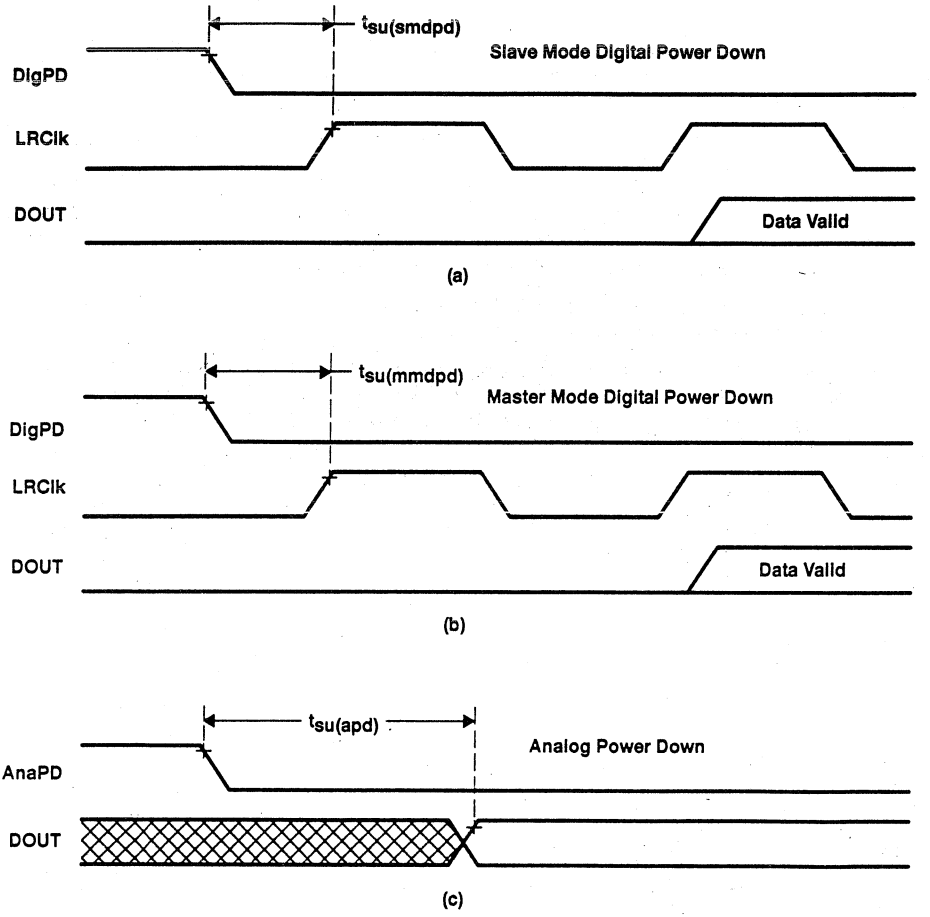


Figure 2–1. Power Down Timing Relationships

2.2 Differential Input

The input is differential in order to provide common mode noise rejection and increase the input dynamic range. Figure 2–2 shows the analog input signals used in a differential configuration to achieve 6.4-V_{pp} differential swing with 3.2-V_{pp} swing per input line.

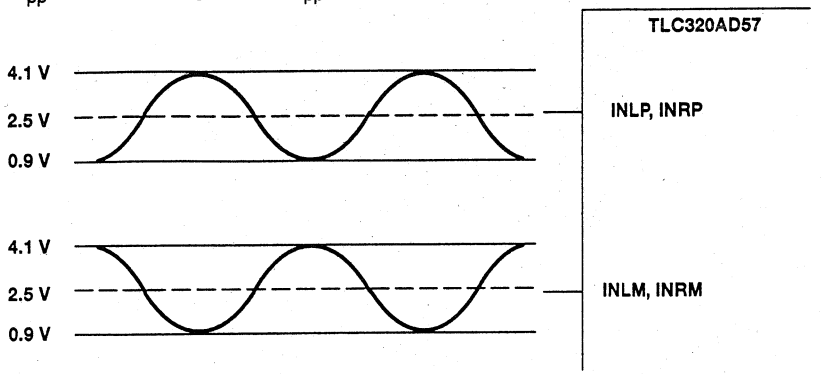


Figure 2–2. Differential Analog Input Configuration

2.3 Sigma-Delta Modulator

The modulator is a fourth order sigma-delta modulator with 64 times oversampling. The ADC provides high resolution, low noise performance from a one bit converter using oversampling techniques.

2.4 Decimation Filter

The decimation filter used after the sigma-delta modulator reduces the digital data rate to the sampling rate of LRClk. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a 2s complement data word of up to 18 bits serially clocked out.

If the input value exceeds the full range of the converter, the output of the decimator is held at the appropriate extreme until the input returns to within the dynamic range of the device.

2.5 High-Pass Filter

The high pass filter removes dc from the input. With this filtering, offset calibration is not needed. The high-pass filter can be circumvented by asserting the HPByp terminal to pass dc signals through the converter. However, an offset due to within the converter can be present when bypassing the high-pass filter.

2.6 Master-Clock Circuit

The master-clock circuit is used to generate and distribute necessary clocks throughout the device. MCLK is the external master clock input. CMODE is used to select the relationship of MCLK to the sample rate, LRClk. When CMODE is low, the sample rate of the data paths is set to LRClk = MCLK/256. When CMODE is high, the sample rate is set to LRClk = MCLK/384. With a fixed oversampling ratio of 64×, the effect of changing MCLK is shown in Table 2–1.

When in master mode, SCLK is derived from MCLK in order to provide clocking of the serial communications between the sigma-delta audio ADC and a DSP or control logic. This is equivalent to a clock running at 64× LRClk.

When in slave mode, SCLK is externally derived.

Table 2–1. Master Clock to Sample Rate Comparison (modes 1, 3, 4, 5)

MCLK (MHz)	CMODE	SCLK (MHz)	LRClk (kHz)
12.2880	Low	3.0720	48
18.4320	High		
11.2896	Low	2.8224	44.1
16.9344	High		
8.1920	Low	2.0480	32
12.2880	High		
0.2560	Low	0.0640	1
0.3840	High		

2.7 Test

When the TEST terminal is high, the test mode is selected which routes the high speed one bit modulator result to the serial port output. When in the test mode, SCLK is an output whose frequency is equal to the data output rate. LRClk is an input when the test mode is selected. This allows for the selection of the left or right modulator output to be routed to the serial port (high = left and low = right).

2.8 Serial Interface

Although the serial data is shifted out in two seperate time packets which represent the left and right channels, the inputs are sampled and converted simultaneously.

The serial interface protocol has master and slave modes each with different read out modes. The master mode is used to source the control signals for conversion synchronization while the slave mode allows an external controller to provide conversion synchronization signals.

The five master modes are shown in Figures 2–3(a) through 2–3(e) and the three slave modes are shown in Figures 2–4(a) through 2–4(c). For a 16-bit word, D15 is the most significant bit and D0 is the least significant bit. Unless otherwise specified, all values are in 2s complement format.

In master mode, SCLK is generated internally and is sourced as an output. The relationship of SCLK to LRClk is 64× (modes 1, 3, 4, 5) or 32× (modes 6, 7). In slave mode, SCLK is an input. SCLK timing must meet the timing specifications listed in the recommended operating conditions section.

2.8.1 Master Mode

As the master, the TLC320AD57 generates LRClk, Fsync, and SCLK from MCLK. These signals are provided for synchronizing the serial port of a DSP or other control devices.

Fsync is used to designate the valid data from the ADC, and this is accomplished in the master modes by one of two methods. The first is a single pulse on Fsync prior to valid data. This indicates the starting point for the data. The second method of frame synchronization is to hold Fsync high during the entire valid data cycle which provides boundaries for the data.

LRClk is generated internally from MCLK. The frequency of this signal is fixed at the sampling frequency Fs [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)]. During the high period of this signal, the left channel data is serially shifted to the output; during the low period, the right channel data is shifted to the output. The conversion cycle is synchronized with the rising edge of LRClk.

Five modes are available when the device is configured as a master. Two modes are for 18-bit communications. These modes differ from each other in that the MSB is transferred first in one mode while the LSB is transferred first in the second mode [see Figures 2–3(b) and 2–3(c)]. When the LSB is transferred first, the data is right justified to the LRClk [see Figures 2–3(a) through 2–3(e)]. The three other modes

available as a master are 16-bit modes. Once again, two of the modes differ as MSB first versus LSB first. These two modes set SCLK = LRClk × 32. This is one half the frequency used in the other transfer modes [see Figures 2–3(d) and 2–3(e)]. The third 16-bit mode provides the data MSB first with one clock delay after LRClk [see Figure 2–3(a)].

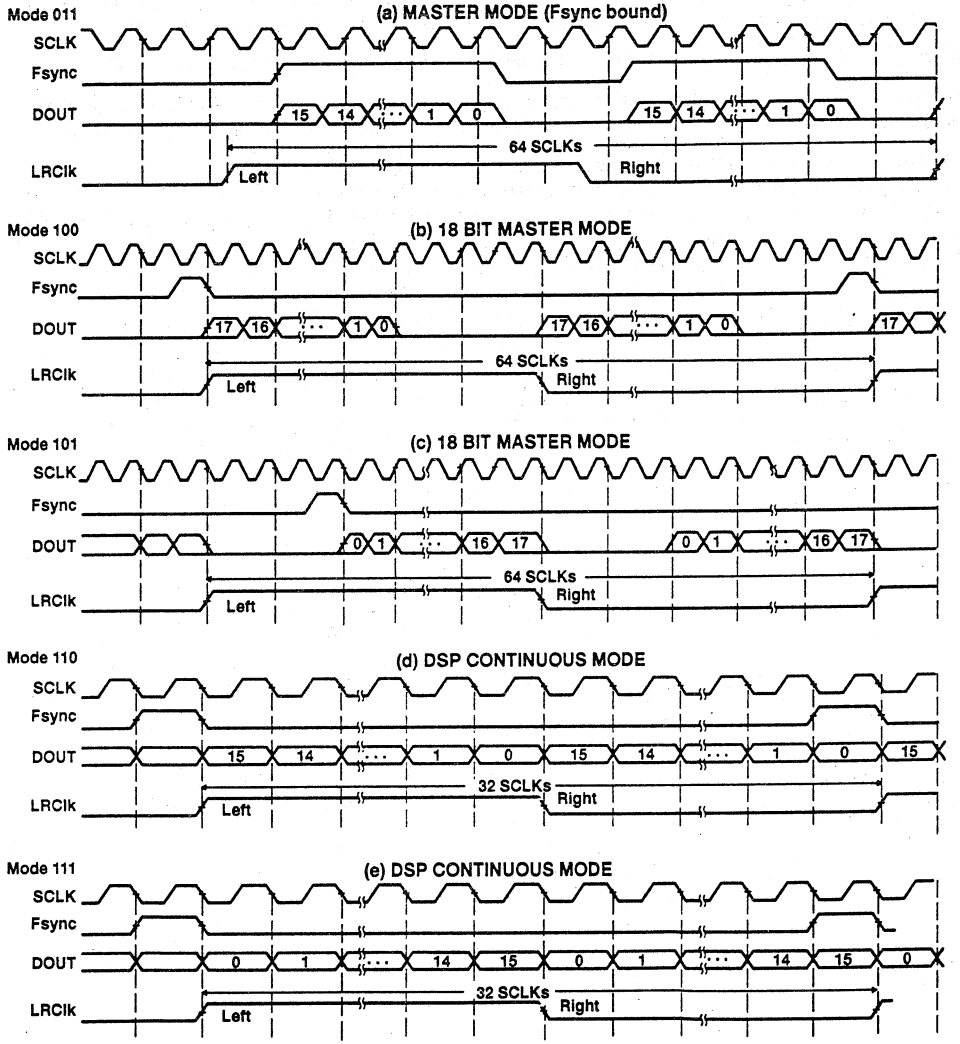


Figure 2–3. Serial Master Transfer Modes

2.8.2 Slave Mode

As a slave, the TLC320AD57 receives LRClk, Fsync, and SCLK as inputs. The conversion cycle is synchronized to the rising edge of LRClk, and the data is synchronized to the falling edge of SCLK. SCLK must meet the setup time requirements specified in the recommended operating conditions section. Synchronization of the slave modes is accomplished with the digital power-down control.

In slave mode, Fsync is an input. Three modes are provided as shown in Figures 2–4(a) – 2–4(c).

SCLK and LRClk are externally generated and sourced. The first rising edges of SCLK and LRClk after a power-down cycle initiate the conversion cycle. Refer to the master mode section for signal functions.

Several modes are available when configured as a slave. Using the Mode0, Mode1, and Mode2 terminals, the TLC320AD57 can be set to shift out the MSB first or the LSB first [see Figures 2–4(a) and 2–4(b)]. The number of bits shifted out, however, can be controlled by the number of valid SCLK cycles provided within the left or right channel period. If only enough clocks are provided to shift out 16 data bits before LRClk changes state, then this is equivalent to a 16-bit mode.

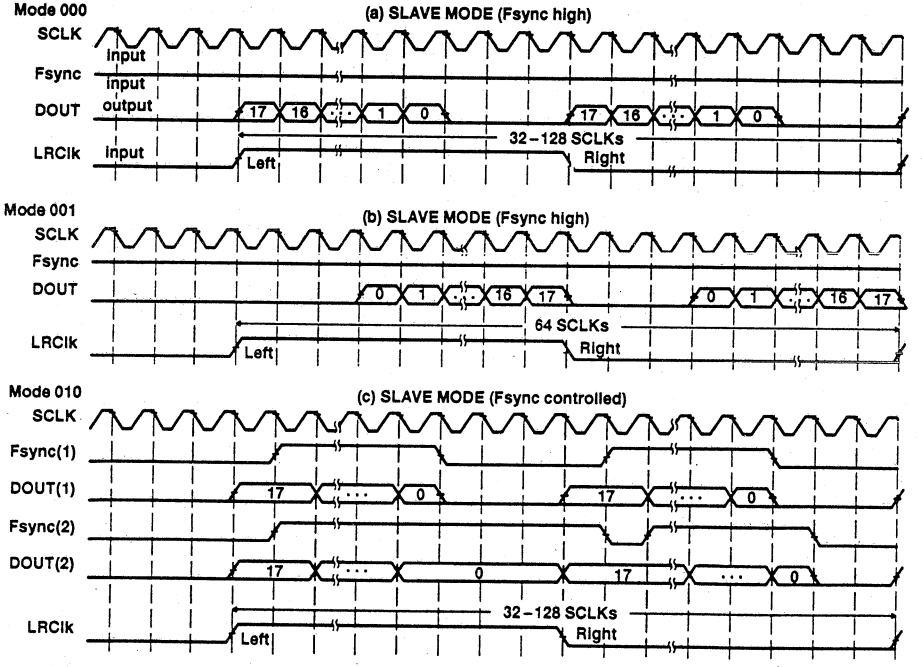


Figure 2–4. Serial Slave Transfer Modes

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Analog supply voltage range, AV_{DD} (see Note 1) ..... −0.3 V to 6.5 V
Digital supply voltage range, DV_{DD} (see Note 2) ..... −0.3 V to 6.5 V
Digital output voltage range, (externally applied) ..... −0.3 V to DV_{DD} + 0.3 V
Digital input voltage range, MODE0 – MODE2 ..... −0.3 V to DV_{DD} + 0.3 V
Analog input voltage range, INLP, INLM, INRP, INRM ..... −0.3 V to AV_{DD} + 0.3 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values for maximum ratings are with respect to AV_{SS}.
2. Voltage values for maximum ratings are with respect to DV_{SS}.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD} (see Note 3)	4.75	5	5.25	V
Digital supply voltage, DV_{DD}	4.75	5	5.25	V
Analog logic supply voltage, at Vlogic	4.75	5	5.25	V
Reference voltage, V_{ref}		3.2		V
Setup time, SCLK↑ to LRClk, slave mode, t_{su1}	30			ns
Setup time, LRClk to SCLK↑, slave mode, t_{su2}	30			ns
Setup time, SCLK↑ to Fsync, slave mode, t_{su3}	30			ns
Setup time, Fsync to SCLK↑, slave mode, t_{su4}	30			ns
Setup time, DigPD↓ to LRclk↑, slave mode, $t_{su(smdpd)}$		30		ns
Setup time, DigPD↓ to LRclk↑, master mode, $t_{su(mmdpd)}$		30		ns
Setup time, AnaPD↓ to DOUT valid, $t_{su(apd)}$		30		ns
Load resistance at DOUT, R_L		10		kΩ
Operating free-air temperature, T_A	0		70	°C

NOTE 3: Voltages at analog inputs and outputs and AV_{DD} are with respect to the AV_{SS} terminal.

3.3 Electrical Characteristics

3.3.1 Digital Interface, T_A = 25°C; AV_{DD}, DV_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2	4.6		V
V_{IL}	Low-level input voltage			0.2	0.8	V
V_{OH}	High-level output voltage, at DOUT	I_{OH} = 2 mA	2.4	4.6		V
V_{OL}	Low-level output voltage, at DOUT	I_{OL} = 2 mA		0.2	0.4	V
I_{IH}	High-level input current, any digital input			1		µA
I_{IL}	Low-level input current, any digital input			1		µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

3.3.2 Analog Interface

3.3.2.1 ADC Modulator, T_A = 25°C; AV_{DD}, DV_{DD} = 5 V; Fs = 48 kHz, Bandwidth = 24 kHz, HPByp = 1, CMODE = 0, MODE0 – 2 = 101

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			18		Bits
DYNAMIC PERFORMANCE					
Signal to noise (EIAJ)	INLP=INRP=2.5 V dc INLM=INRM=2.5 V dc	93	97		dB
Dynamic range	6.4 V differential input between INRP (INLP) and INRM (INLM)	91	95		dB
Signal to noise + distortion (THD + N)			91		dB
Total harmonic distortion			0.001%		
Interchannel isolation			108		dB
DC ACCURACY					
Gain error			±0.02		
Interchannel gain mismatch			±0.02		dB
Offset error (18-bit resolution)			±5		mV
Offset drift			±0.17		LSB/°C

3.3.2.2 Inputs/Supplies, T_A = 25°C; AV_{DD}, DV_{DD} = 5 V; Fs = 48 kHz, Bandwidth = 24 kHz, HPByp = 1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Input voltage			6.4		V
			3.2		
Input impedance			50		kΩ
POWER SUPPLIES					
Power supply current	I_{DD} (analog), operating		20	28	mA
	I_{DD} (digital), operating		24	32	mA
	I_{DD} (analog), power down		100		µA
	I_{DD} (digital), power down		40		µA
Power dissipation			220		mW

3.3.3 Channel Characteristics, T_A = 25°C; AV_{DD}, DV_{DD} = 5 V; Fs = 48 kHz, HPByp = 1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband (−3 dB)	HPByp = 0	0.001		24	kHz
Passband ripple	30 Hz – 21.8 kHz		±0.01		dB
Stopband attenuation	26.2 kHz – 3046 kHz	80			dB
Group delay			25 × Fs		s

3.4 Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(MFSD)}$	Delay time, SCLK↓ to Fsync, master mode	−20		20	ns
$t_{d(MDD)}$	Delay time, SCLK↓ to DOUT, master mode	0		50	ns
$t_{d(MIRD)}$	Delay time, SCLK↓ to LRClk, master mode	−20		20	ns
$t_{d(SDD1)}$	Delay time, LRClk to DOUT, slave mode			50	ns
$t_{d(SDD2)}$	Delay time, SCLK↓ to DOUT, slave mode			50	ns

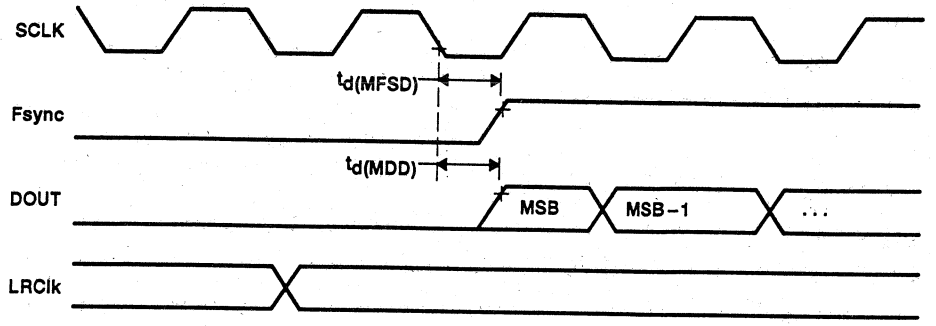


Figure 4–1. SCLK to Fsync and DOUT – Master Mode 3

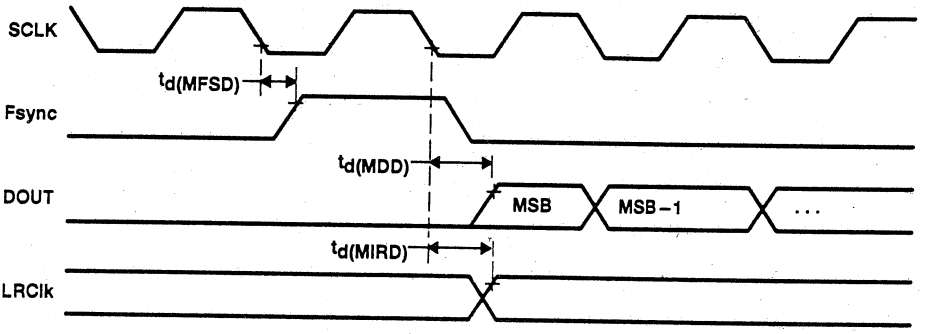


Figure 4–2. SCLK to Fsync, DOUT, and LRClk – Master Modes 4 and 6

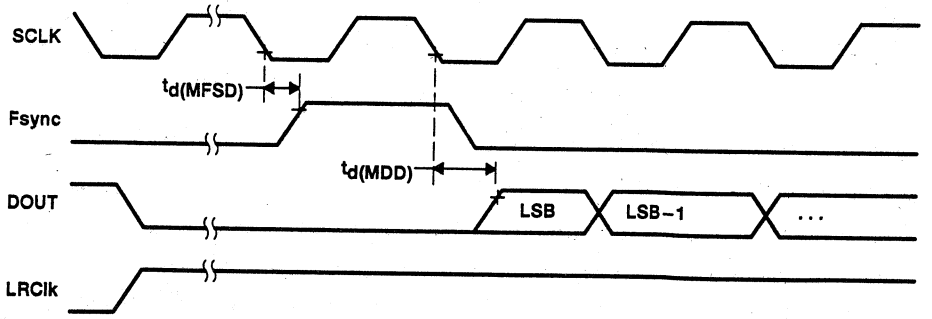


Figure 4–3. SCLK to Fsync, DOUT, and LRClk – Master Mode 5

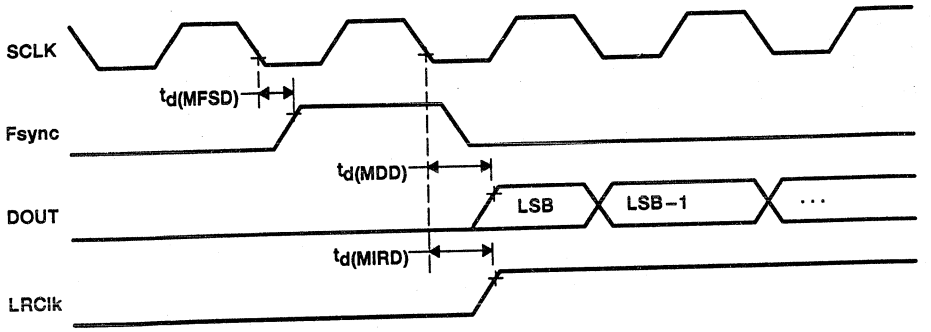


Figure 4–4. SCLK to Fsync, DOUT, and LRClk – Master Mode 7

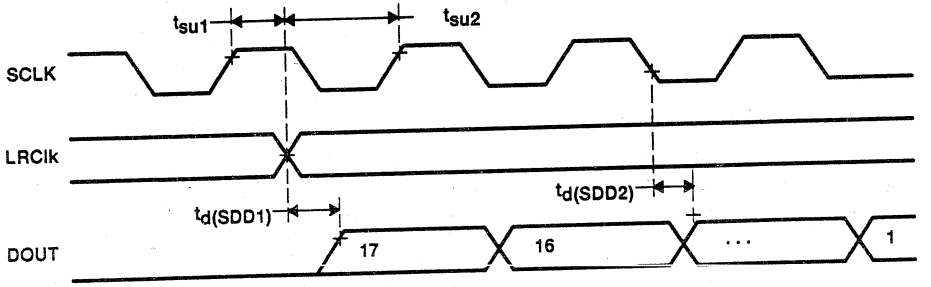


Figure 4–5. SCLK to LRClk and DOUT – Slave Mode (Fsync High) (Mode 0)

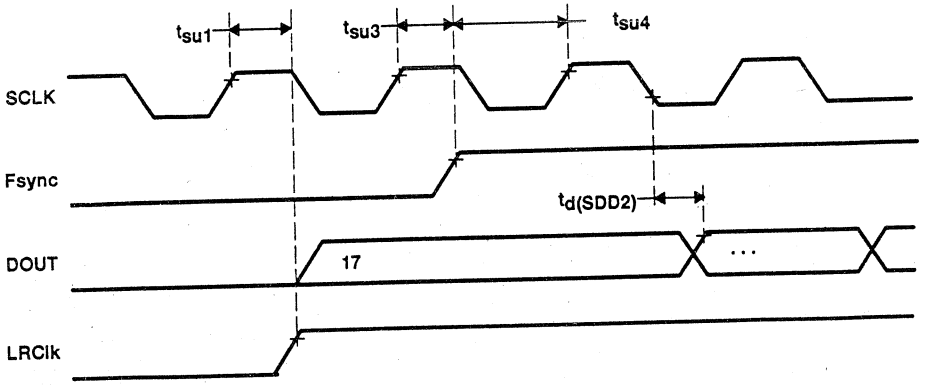
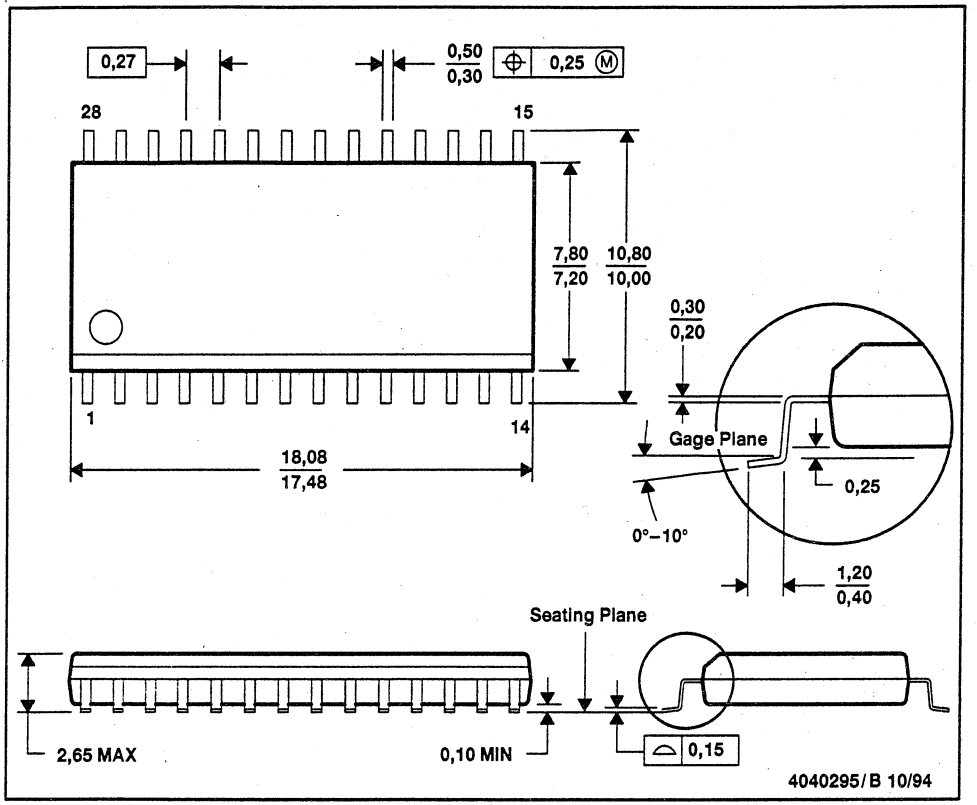


Figure 4–6. SCLK to Fsync, LRClk, and DOUT – Slave Mode (Fsync Controlled) (Mode 2)

Appendix A
Mechanical Data

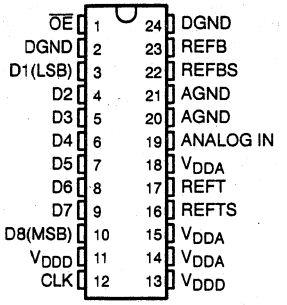
DWM (R-PDSO-G28) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

- 8-Bit Resolution
- Linearity Error
  - ±0.75 LSB Max (25°C)
  - ±1 LSB Max (–20°C to 75°C)
- Differential Linealty Error
  - ±0.5 LSB (25°C)
  - ±0.75 LSB Max(–20°C to 75°C)
- Maximum Conversion Rate
  - 20 Mega-Samples per Second (MSPS) Min
- Internal Voltage Reference
- 5-V Single-Supply Operation
- Low Power Consumption . . . 90 mW Typ
- Interchangeable With Sony CXD1175

NS PACKAGE† (TOP VIEW)



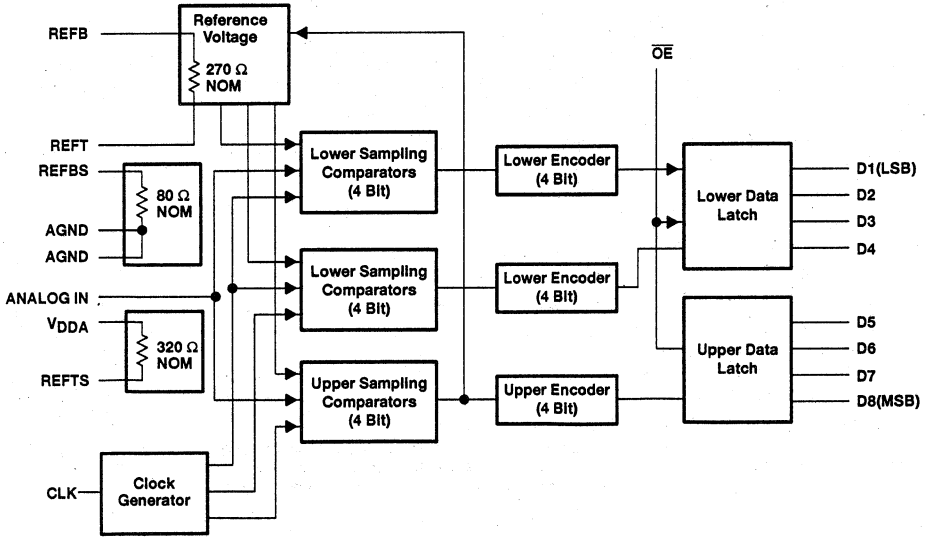
† Available in tape and reel only and ordered as the TLC5510INSLE.

description

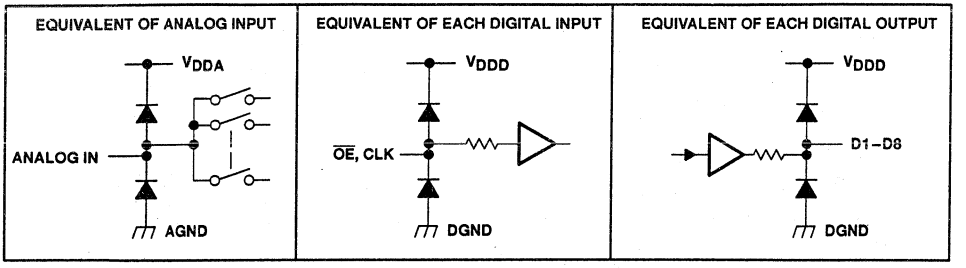
The TLC5510 is a CMOS 8-bit resolution semiflash analog-to-digital converter with 5-V single power supply and an internal reference voltage source. It converts a wide-band analog signal (such as a video signal) to a digital signal at a sampling rate of dc to 20 MHz.

Because of this high-speed capability and low power consumption, the TLC5510 is suitable for digital TV, portable VCR, or video signal processing.

functional block diagram



schematics of inputs and outputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock in
DGND	2, 24		Digital ground
D1–D8	3–10	O	Digital data out. D1:LSB, D8:MSB
$\overline{OE}$	1	I	Output enable. When $\overline{OE}$ = L, data is enabled. When $\overline{OE}$ = H, D1–D8 is high impedance.
V_{DDA}	14, 15, 18		Analog V_{DD}
V_{DDD}	11, 13		Digital V_{DD}
REFB	23	I	Reference voltage in (bottom)
REFBS	22		Reference voltage (bottom). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFB terminal and the REFTS terminal is shorted to the REFT terminal (see Figure 3).
REFT	17	I	Reference voltage in (top)
REFTS	16		Reference voltage (top). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFT terminal and the REFBS terminal is shorted to the REFB terminal (see Figure 3).

absolute maximum ratings†

Supply voltage, V_{DDA}, V_{DDD} ..... 7 V
Reference voltage input range, $V_{ref(T)}$, $V_{ref(B)}$, $V_{ref(BS)}$, $V_{ref(TS)}$ ..... AGND to V_{DDA}
Analog input voltage range, $V_{I(ANLG)}$ ..... AGND to V_{DDA}
Digital input voltage range, $V_{I(DGTL)}$ ..... DGND to V_{DDD}
Digital output voltage range, $V_{O(DGTL)}$ ..... DGND to V_{DDD}
Operating free-air temperature range, T_A ..... –20°C to 75°C
Storage temperature range ..... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{DDA}–AGND	4.75	5	5.25	V
	V_{DDD}–AGND	4.75	5	5.25	
	AGND–DGND	–100	0	100	mV
Reference input voltage (top), $V_{ref(T)}$		$V_{ref(B)}$+2	$V_{ref(B)}$+2	2.7	V
Reference input voltage (bottom), $V_{ref(B)}$		0	0.6	$V_{ref(T)}$–2	V
Analog input voltage range, $V_{I(ANLG)}$ (see Note 1)		$V_{ref(B)}$		$V_{ref(T)}$	V
High-level input voltage, V_{IH}		4			V
Low-level input voltage, V_{IL}				1	V
Pulse duration, clock high, $t_{w(H)}$		25			ns
Pulse duration, clock low, $t_{w(L)}$		25			ns

NOTE 1: REFT – REFB ≥ 2.4 V maximum

electrical characteristics at V_{DD} = 5 V, $V_{ref(T)}$ = 2.5 V, $V_{ref(B)}$ = 0.5 V, f_{conv} = 20 MSPS, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
E_L	Linearity error	f_{conv} = 20 MSPS, V_I = 0.5 V to 2.5 V	T_A = 25°C			±0.4	±0.75	LSB
			T_A = –20°C to 75°C				±1	
E_D	Linearity error, differential		T_A = 25°C			±0.3	±0.5	
			T_A = –20°C to 75°C				±0.75	
	Self bias (1)	Short REFB to REFBS,	Short REFT to REFTS		0.57	0.61	0.65	V
	Self bias (2)				1.9	2.02	2.15	
	Self bias (3)	Short REFB to AGND,	Short REFT to REFTS		2.18	2.29	2.4	
I_{ref}	Reference voltage current	$V_{ref(T)} - V_{ref(B)}$ = 2 V			5.2	7.5	10.5	mA
R_{ref}	Reference voltage resistor	Between REFT and REFB terminals			190	270	350	Ω
C_I	Analog input capacitance	$V_{I(ANLG)}$ = 1.5 V + 0.07 V_{rms}				16		pF
E_{ZS}	Zero scale error	V_{ref} = REFT – REFB = 2 V			–18	–43	–68	mV
E_{FS}	Full scale error				–20	0	20	
I_{IH}	High-level input current	V_{DD} = MAX,	V_{IH} = V_{DD}				5	µA
I_{IL}	Low-level input current	V_{DD} = MAX,	V_{IL} = 0				5	
I_{OH}	High-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN,	V_{OH} = V_{DD}–0.5 V	–1.5			mA
I_{OL}	Low-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN,	V_{OL} = 0.4 V	2.5			
I_{OZH}	High-level high-impedance-state output leakage current	$\overline{OE}$ = V_{DD},	V_{DD} = MAX	V_{OH} = V_{DD}			16	µA
I_{OZL}	Low-level high-impedance-state output leakage current	$\overline{OE}$ = V_{DD},	V_{DD} = MIN	V_{OL} = 0			16	
I_{DD}	Supply current	f_s = 20 MSPS,	NTSC ramp wave input			18	27	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

operating characteristics at V_{DD} = 5 V, V_{RT} = 2.5 V, V_{RB} = 0.5 V, f_S = 20 MSPS, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{conv}	Maximum conversion rate	$V_{I(ANLG)}$ = 0.5 V – 2.5 V, f_I = 1-kHz ramp wave form	20			MSPS
BW	Analog input bandwidth	At – 1 dB		14		MHz
t_{pd}	Digital output delay time	$C_L \leq$ 10 pF (see Note 2)		18	30	ns
	Differential gain	NTSC 40 IRE modulation wave, f_{conv} = 14.3 MSPS		1%		
	Differential phase			0.7		°
t_{AJ}	Aperture jitter time			30		ps
t_{pS}	Sampling delay time			4		ns

NOTE 2: C_L includes probe and jig capacitance

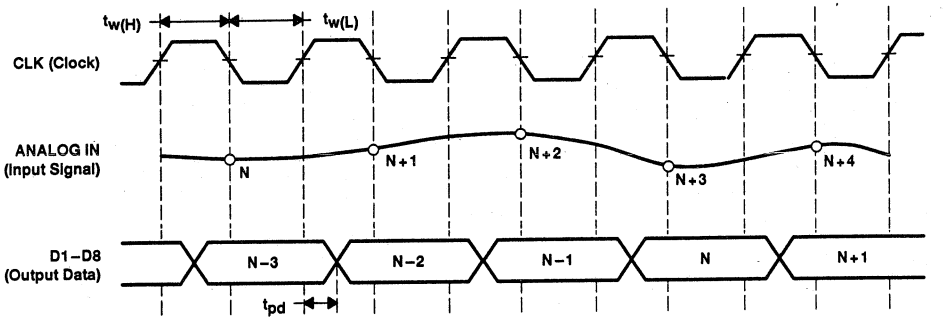


Figure 1. I/O Timing Diagram

PRINCIPLES OF OPERATION

functional description

The TLC5510 is a semiflash analog-to-digital converter featuring two lower comparator blocks of four bits each.

As shown in Figure 2, input voltage $V_I(1)$ is sampled with the falling edge of CLK1 to the upper comparators block and the lower comparators block(A), S(1), as shown in Figure 2. The upper comparators block finalizes the upper data UD(1) with the rising edge of CLK2, and simultaneously, the lower reference voltage generates the voltage RV(1) corresponding to the upper data. The lower comparators block (A) finalizes the lower data LD(1) with the rising edge of CLK3. UD(1) and LD(1) are combined and output as OUT(1) with the rising edge of CLK4. According to the above internal operation described, output data is delayed 2.5 clocks from the analog input voltage sampling point.

Input voltage $V_I(2)$ is sampled with the falling edge of CLK2. UD(2) is finalized with the rising edge of CLK3, and LD(2) is finalized with the rising edge of CLK4 at the lower comparators block(B). OUT(2) is output with the rising edge of CLK5.

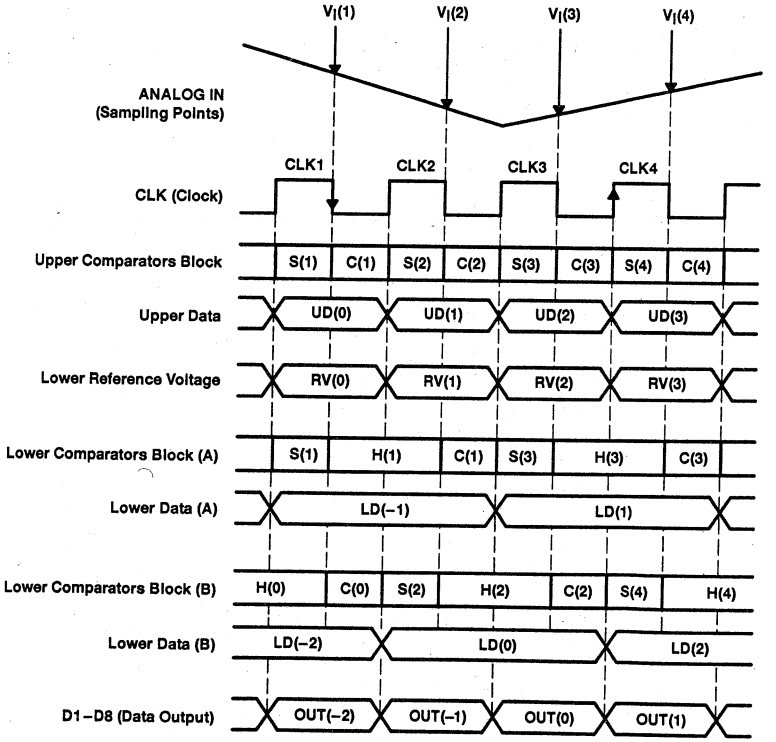


Figure 2. Internal Functional Timing Diagram

PRINCIPLES OF OPERATION

internal referencing

Three internal resistors are provided such that the device can generate an internal reference voltage. These resistors are brought out on terminals V_{DDA}, REFTS, REFT, REFB, REFBS, and AGND.

To use the internally generated reference voltage, terminal connections should be made as shown in Figure 3. This connection will provide the standard video 2-V reference for the nominal digital output.

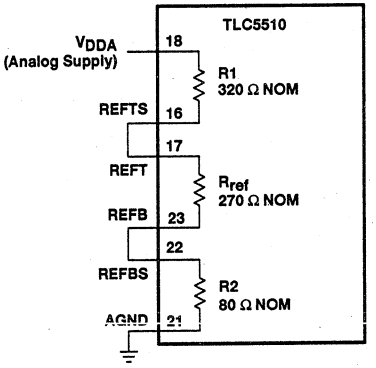


Figure 3. External Connections for Using the Internal Reference Resistor Divider

functional operation

The TLC5510 functions as shown in the following table.

Table 1. Functional Operation

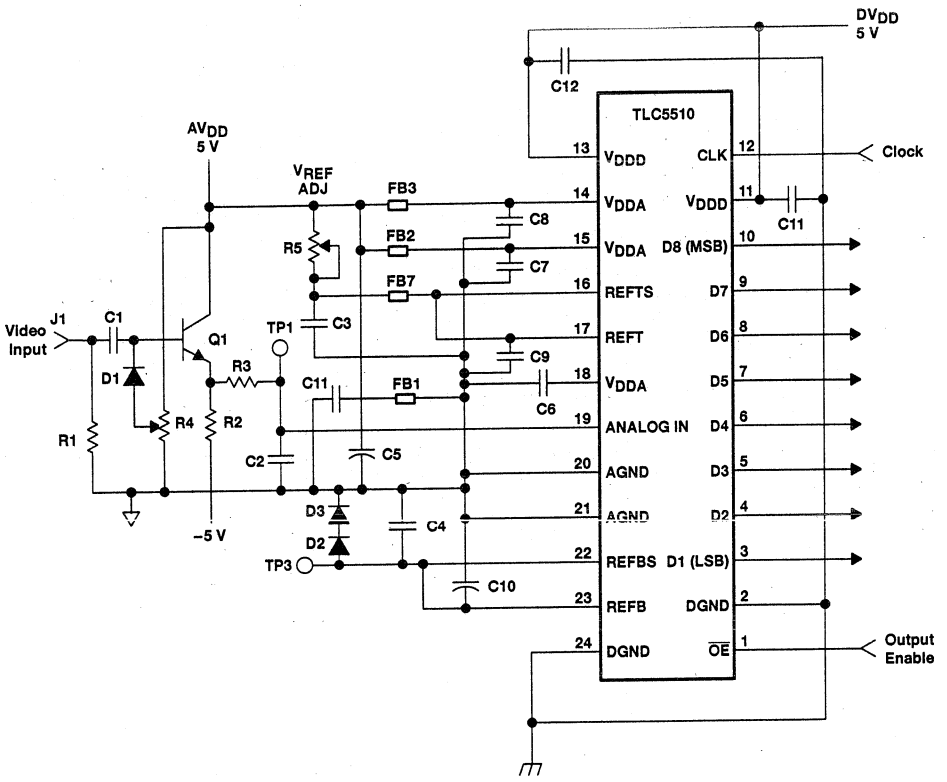
INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
$V_{ref(T)}$	0	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	127	1	0	0	0	0	0	0	0
•	128	0	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
$V_{ref(B)}$	255	0	0	0	0	0	0	0	0

APPLICATION INFORMATION

The following notes are design recommendations that should be used with the TLC5510.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
- Since AGND and DGND are not connected internally, these terminals need to be connected externally. With breadboards, these ground lines should be connected through separate leads with proper supply bypassing. A good method to use is separate twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts.
- V_{DDA} to AGND and V_{DDD} to DGND should be decoupled with 1-μF and 0.01-μF capacitors, respectively, placed as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.01-μF capacitor. Care should be exercised to assure a solid noise-free ground connection for the analog and digital grounds.
- V_{DDA}, AGND, and ANALOG IN terminals should be shielded from the higher frequency terminals, CLK and D0–D7. If possible, AGND traces should be placed on both sides of the ANALOG IN traces on the PCB for shielding.
- In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

APPLICATION INFORMATION



LOCATION	DESCRIPTION
C1, C3–C4, C6–C12	0.1 μF Capacitor
C2	10 pF Capacitor
C5	47 μF Capacitor
FB1, FB2, FB3, FB7	Ferrite Bead
R1, R3	75 Ω resistor
R2	1 kΩ resistor
R4	10 kΩ resistor, clamp voltage adjust
R5	300 Ω resistor, reference voltage fine adjust

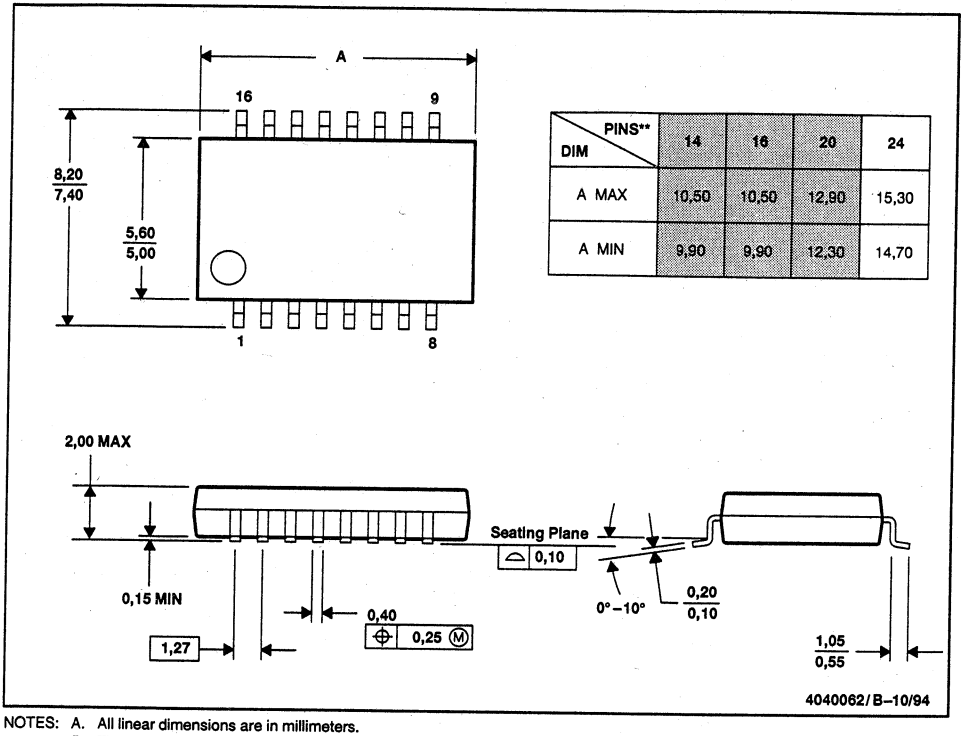
Figure 4. Application and Test Schematic

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN

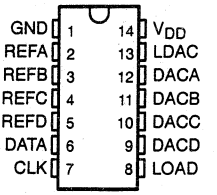


DIM \ PINS**	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

- Four 8-Bit Voltage Output DACS
- 5-V Single-Supply Operation
- Serial Interface
- High-Impedance Reference Inputs
- Programmable 1 or 2 Times Output Range
- Simultaneous-Update Facility
- Internal Power-On Reset
- Low Power Consumption
- Half-Buffered Output

N OR D PACKAGE
(TOP VIEW)



applications

- Programmable Voltage Sources
- Digitally Controlled Amplifiers/Attenuators
- Mobile Communications
- Automatic Test Equipment
- Process Monitoring and Control
- Signal Synthesis

description

The TLC5620C and TLC5620I are quad 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND and are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

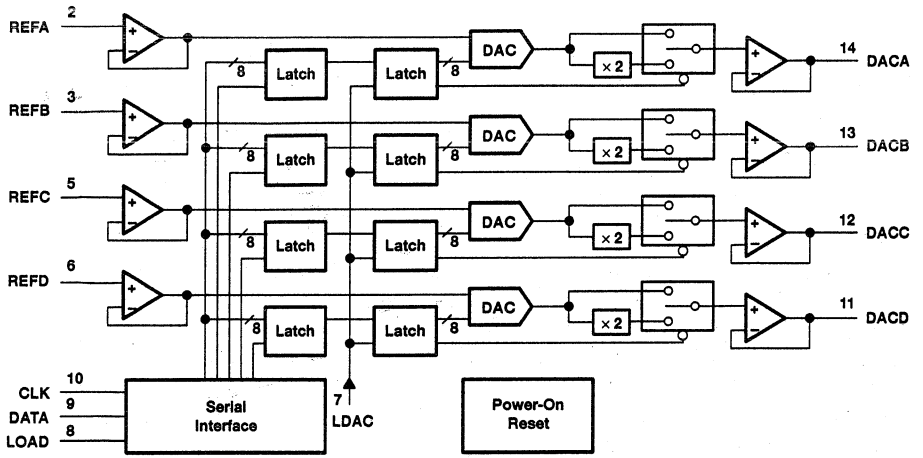
Digital control of the TLC5620C and TLC5620I are via a simple three-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 11-bit command word comprises 8 bits of data, 2 DAC select bits and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs updated simultaneously through control of the LDAC terminal. The digital inputs feature Schmitt triggers for high noise immunity.

The 14-pin small-outline (SO) package allows digital control of analog functions in space-critical applications. The TLC5620C is characterized for operation from 0°C to 70°C. The TLC5620I is characterized for operation from –40°C to 85°C. The TLC5620C and TLC5620I do not require external trimming.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	TLC5620CD	TLC5620CN
–40°C to 85°C	TLC5620ID	TLC5620IN

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	7	I	Serial-interface clock, data entered on the negative edge
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial-interface digital-data input
GND	1	I	Ground return and reference terminal
LDAC	13	I	DAC-update latch control
LOAD	8	I	Serial-interface load control
REFA	2	I	Reference voltage input to DACA
REFB	3	I	Reference voltage input to DACB
REFC	4	I	Reference voltage input to DACC
REFD	5	I	Reference voltage input to DACD
V_{DD}	14	I	Positive supply voltage

detailed description

The TLC5620 is implemented using four resistor-string digital-to-analog converters (DACs). The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 2. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Because the inputs are buffered, the DACs always presents a high-impedance load to the reference source.

detailed description (continued)

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times 1 or times 2 gain. The output amplifiers feature rail-to-rail output stages, allowing outputs over the full-supply range to be achieved in times 2 configuration, with a reference voltage of $V_{DD}/2$. Used in this way, a slight degradation in linearity is encountered over the last few codes as the output approaches V_{DD}.

On powerup, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACAIBICID}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the RNG bit is a 0 or 1 within the serial-control word.

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial-input register to the selected DAC as shown in Figure 1. If LDAC is low, the selected DAC output voltage is updated and LOAD goes low. If LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered MSB first.

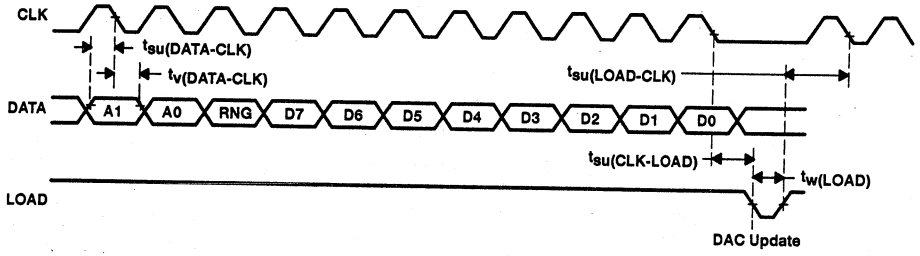


Figure 1. LOAD-Controlled Update (LDAC = Low)

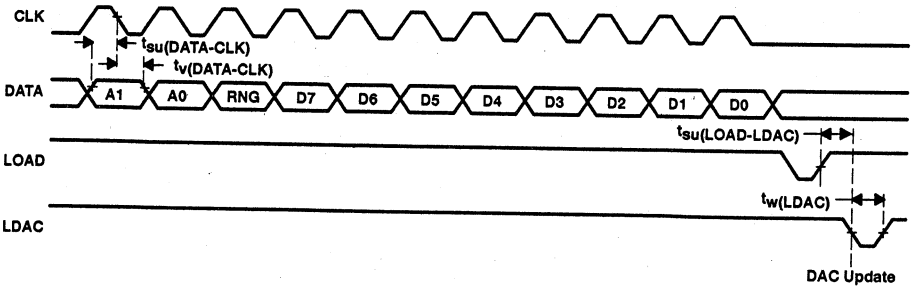


Figure 2. LDAC-Controlled Update

data interface (continued)

Table 1 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = Low, the output range is between the applied reference voltage and GND, and when RNG = High, the range is between twice the applied reference voltage and GND.

Table 1. Serial-Input Decode

A1	A0	DAC UPDATED
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

Table 2. Ideal-Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND) ..... 7 V
Digital input voltage range ..... GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range, V_{ID} ..... GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLC5620C ..... 0°C to 70°C
TLC5620I ..... –25°C to 85°C
Storage temperature range ..... –50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 230°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75		5.25	V
High-level digital input voltage, V_{IH}		0.8 V_{DD}			V
Low-level digital input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} [AIBICID]			0.5 V_{DD}		V
Load resistance, R_L		10			kΩ
Setup time, data input, $t_{su(DATA-CLK)}$		50			ns
Valid time, data input valid after CLK↓, $t_{v(DATA-CLK)}$		50			ns
Setup time, CLK 11th falling edge to LOAD, $t_{su(CLK-LOAD)}$		50			ns
Setup time, LOAD↑ to CLK↓, $t_{su(LOAD-CLK)}$		50			ns
Pulse duration, LOAD, $t_{w(LOAD)}$		250			ns
Pulse duration, LDAC, $t_{w(LDAC)}$		250			ns
Setup time, LOAD↑ to LDAC↓, $t_{su(LOAD-LDAC)}$		0			ns
CLK frequency				1	MHz
Operating free-air temperature, T_A	TLC5620C	0		70	°C
	TLC5620I	−40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			±10	µA
I_{IL}	Low-level digital input current	V_I = 0 V			±10	µA
$I_{O(sink)}$	Output sink current	Each DAC output	20			µA
$I_{O(source)}$	Output source current		2			mA
C_i	Input capacitance			15		pF
	Reference input capacitance			15		
I_{DD}	Supply current	V_{DD} = 5 V			2	mA
I_{ref}	Reference input current	V_{DD} = 5 V, V_{ref} = 2 V			±10	µA
E_L	Linearity error	End point corrected			±1	LSB
E_D	Differential-linearity error	V_{ref} = 2 V, ×2 gain			±0.9	LSB
E_{ZS}	Zero-scale error	V_{ref} = 2 V, ×2 gain			±30	mV
E_{FS}	Full-scale error	V_{ref} = 2 V, ×2 gain			±60	mV
	Full-scale error temperature coefficient	V_{ref} = 2 V, ×2 gain		±25		µV/°C
PSRR	Power-supply rejection ratio			−50		dB

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C_L = 100 pF, R_L = 10 kΩ		1		V/µs
Output settling time	To 0.5 LSB, C_L = 100 pF, R_L = 10 kΩ		10		µs
Large-signal bandwidth	Measured at −3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACD		−50		dB

PARAMETER MEASUREMENT INFORMATION

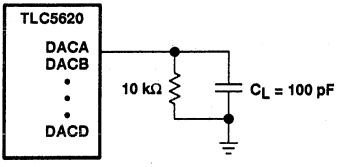
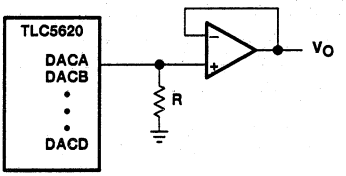


Figure 3. Slewing Settling Time and Linearity Measurements

APPLICATION INFORMATION



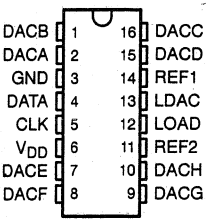
NOTE: Resistor R ≥ 10 kΩ

Figure 4. Output Buffering Schemes

SLAS089 – NOVEMBER 1994

- Eight 8-Bit Voltage Output DACs
- 5-V Single-Supply Operation
- Serial Interface
- High-Impedance Reference Inputs
- Programmable 1 or 2 Times Output Range
- Simultaneous-Update Facility
- Internal Power-On Reset
- Low Power Consumption
- Half-Buffered Output

N OR D PACKAGE
(TOP VIEW)



applications

- Programmable Voltage Sources
- Digitally Controlled Amplifiers/Attenuators
- Mobile Communications
- Automatic Test Equipment
- Process Monitoring and Control
- Signal Synthesis

description

The TLC5628C and TLC5628I are octal 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND and are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

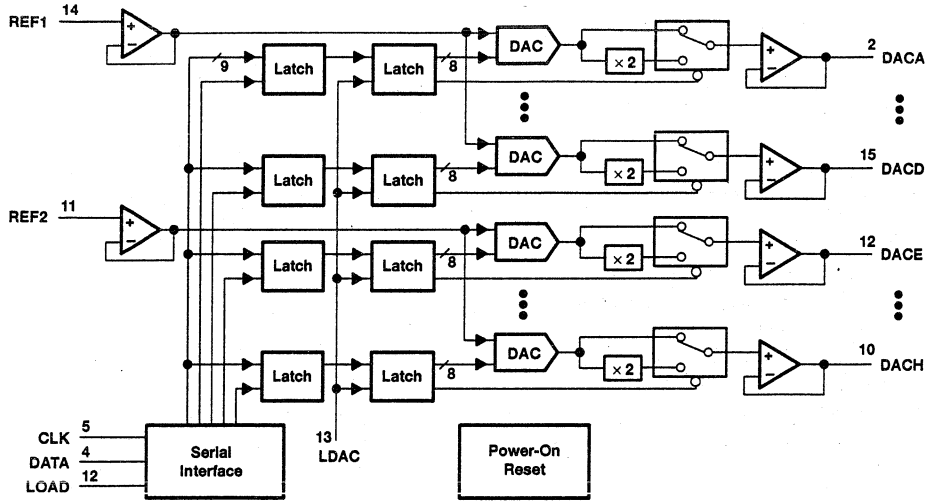
Digital control of the TLC5628C and TLC5628I are via a simple three-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 12-bit command word comprises 8 bits of data, 3 DAC select bits and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs updated simultaneously through control of the LDAC terminal. The digital inputs feature Schmitt triggers for high noise immunity.

The 16-pin small-outline (D) package allows digital control of analog functions in space-critical applications. The TLC5628C is characterized for operation from 0°C to 70°C. The TLC5628I is characterized for operation from −40°C to 85°C. The TLC5628C and TLC5628I do not require external trimming.

AVAILABLE OPTIONS

	PACKAGE	
T_A	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	TLC5628CD	TLC5628CN
−40°C to 85°C	TLC5628ID	TLC5628IN

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	5	I	Serial-interface clock, data entered on the negative edge
DACA	2	O	DACA analog output
DACB	1	O	DACB analog output
DACC	11	O	DACC analog output
DACD	15	O	DACD analog output
DACE	7	O	DACE analog output
DACF	8	O	DACF analog output
DACG	9	O	DACG analog output
DACH	10	O	DACH analog output
DATA	4	I	Serial-interface digital data input
GND	3	I	Ground return and reference terminal
LDAC	13	I	DAC-update latch control
LOAD	12	I	Serial-interface load control
REF1	14	I	Reference voltage input to DACA
REF2	11	I	Reference voltage input to DACB
V_{DD}	6	I	Positive supply voltage

detailed description

The TLC5628 is implemented using eight resistor-string digital-to-analog converters (DACs). The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 2. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Because the inputs are buffered, the DACs always present a high-impedance load to the reference sources. There are two input reference terminals; REF1 is used for DACA through DACD and REF2 is used by DACE through DACH.

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times 1 or times 2 gain. The output amplifiers feature rail-to-rail output stages, allowing outputs over the full-supply range to be achieved in times 2 configuration, with a reference voltage of $V_{DD}/2$. Used in this way, a slight degradation in linearity is encountered over the last few codes as the output approaches V_{DD}.

On powerup, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA|B|C|D|E|F|G|H}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the RNG bit is a 0 or 1 within the serial-control word.

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial-input register to the selected DAC as shown in Figure 1. If LDAC is low, the selected DAC output voltage is updated and LOAD goes low. If LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered MSB first.

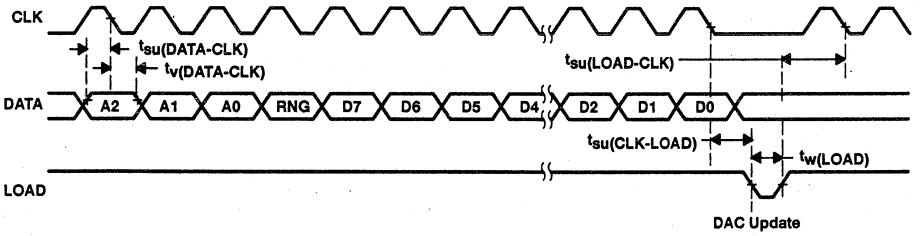


Figure 1. LOAD-Controlled Update (LDAC = Low)

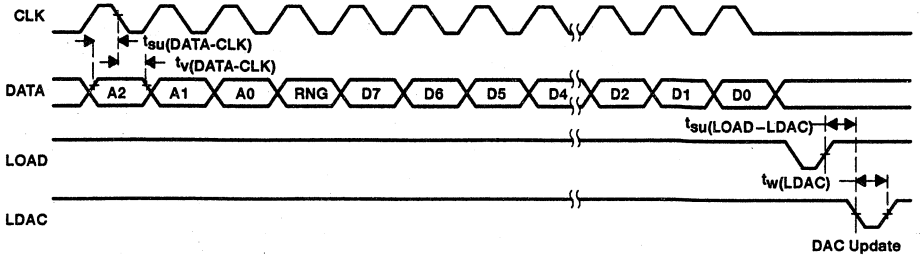


Figure 2. LDAC-Controlled Update

data interface (continued)

Table 1 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = Low, the output range is between the applied reference voltage and GND, and when RNG = High, the range is between twice the applied reference voltage and GND.

Table 1. Serial-Input Decode

A2	A1	A0	DAC UPDATED
0	0	0	DACA
0	0	1	DACB
0	1	0	DACC
0	1	1	DACD
1	0	0	DACE
1	0	1	DACF
1	1	0	DACG
1	1	1	DACH

Table 2. Ideal-Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND) ..... 7 V
Digital input voltage range, V_{ID} ..... GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range ..... GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLC5628C ..... 0°C to 70°C
TLC5628I ..... –25°C to 85°C
Storage temperature range ..... –50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 230°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75		5.25	V
High-level digital input voltage, V_{IH}		0.8 V_{DD}			V
Low-level digital input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} [AIBICIDIEIFIGIH]			0.5 V_{DD}		V
Load resistance, R_L		10			kΩ
Setup time, data input $t_{su(DATA-CLK)}$		50			ns
Valid time, data input valid after CLK↓, $t_{v(DATA-CLK)}$		50			ns
Setup time, CLK 11th falling edge to LOAD, $t_{su(CLK-LOAD)}$		50			ns
Setup time, LOAD↑ to CLK↓, $t_{su(LOAD-CLK)}$		50			ns
Pulse duration, LOAD, $t_{w(LOAD)}$		250			ns
Pulse duration, LDAC, $t_{w(LDAC)}$		250			ns
Setup time, LOAD↑ to LDAC↓, $t_{su(LOAD-LDAC)}$		0			ns
CLK frequency				1	MHz
Operating free-air temperature, T_A	TLC5628C	0		70	°C
	TLC5628I	−40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			±10	µA
I_{IL}	Low-level digital input current	V_I = 0 V			±10	µA
$I_{O(sink)}$	Output sink current	Each DAC output	20			µA
$I_{O(source)}$	Output source current		2			mA
C_i	Input capacitance			15		pF
	Reference input capacitance			15		
I_{DD}	Supply current	V_{DD} = 5 V			2	mA
I_{ref}	Reference input current	V_{DD} = 5 V, V_{ref} = 2 V			±10	µA
E_L	Linearity error	End point corrected			±1	LSB
E_D	Differential-linearity error	V_{ref} = 2 V, ×2 gain			±0.9	LSB
E_{ZS}	Zero-scale error	V_{ref} = 2 V, ×2 gain			±30	mV
E_{FS}	Full-scale error	V_{ref} = 2 V, ×2 gain			±60	mV
	Full-scale error temperature coefficient	V_{ref} = 2 V, ×2 gain		±25		µV/°C
PSRR	Power-supply rejection ratio			−50		dB

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C_L = 100 pF, R_L = 10 kΩ		1		V/µs
Output settling time	To 0.5 LSB, C_L = 100 pF, R_L = 10 kΩ		10		µs
Large-signal bandwidth	Measured at −3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACH		−50		dB

PARAMETER MEASUREMENT INFORMATION

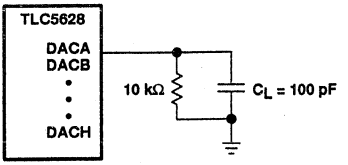
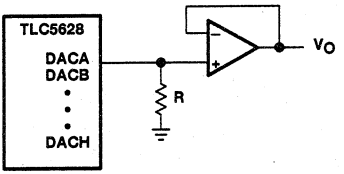


Figure 3. Slewing Settling Time and Linearity Measurements

APPLICATION INFORMATION



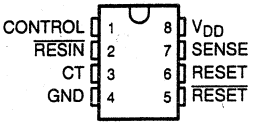
NOTE: Resistor R ≥ 10 kΩ

Figure 4. Output Buffering Schemes

SLVS087 – DECEMBER 1994

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Voltage Sensor of 1.5% Maximum Accuracy, Compensated Over Full Temperature Range**
- **Programmable Delay Time By External Capacitor**
- **Minimum Supply Voltage of 2 V**
- **Defined $\overline{\text{RESET}}$ Output from $V_{DD} \geq 1$ V**
- **Power-Down Control Support for Static RAM With Battery Backup**
- **Maximum Supply Current of 20 μA**
- **SO and DIP Package Options**

D OR P PACKAGE
(TOP VIEW)



description

The TLC7705 is a micropower supply voltage supervisor designed for reset control, primarily in microcomputer and microprocessor systems.

During power-on, $\overline{\text{RESET}}$ is asserted when V_{DD} reaches 1 V. After minimum V_{DD} is established, the circuit tests SENSE voltage and keeps the reset outputs active as long as SENSE voltage remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time, t_d, is determined by an external capacitor:

$$t_d = 2.1 \times 10^4 \times C_T$$

where

C_T is in farads
t_d is in seconds

The TLC7705 has a fixed SENSE threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns to above threshold voltage.

The TLC7705 is a low-power enhancement of the TL7705A. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select ($\overline{\text{CS}}$) of the memory circuit with the RESET output of the TLC7705 and with the CONTROL driven by the memory bank select signal ($\overline{\text{CH1}}$) of the microprocessor (see Figure 4), the memory circuit is automatically disabled during a power loss. (In this application the TLC7705 power has to be supplied by the battery.)

The TLC7705 is characterized for operation over a temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	THRESHOLD VOLTAGE	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
–40°C to 85°C	4.55 V	TLC7705ID	TLC7705IP

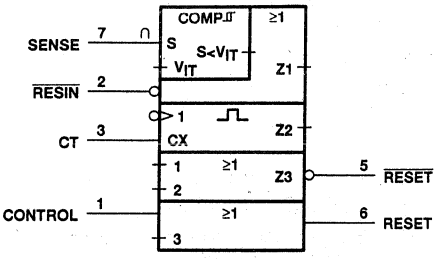
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC7705IDR).

FUNCTION TABLE

CONTROL	$\overline{\text{RESIN}}$	$V_{I(SENSE)} > V_T$	RESET	$\overline{\text{RESET}}$
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L†	H†
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H†

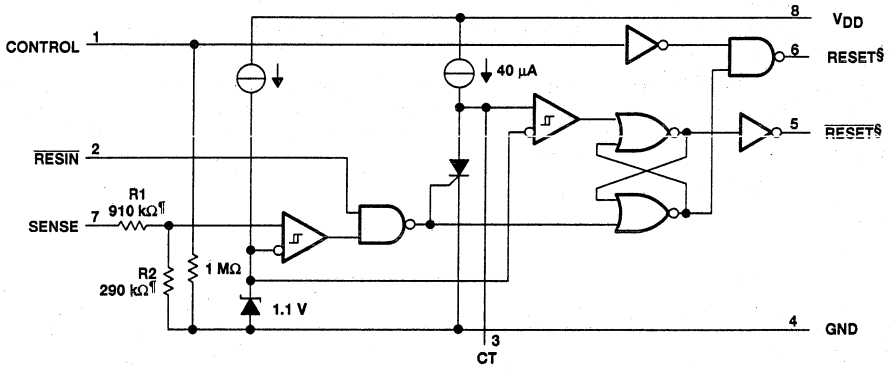
† $t > t_d$

logic symbol‡



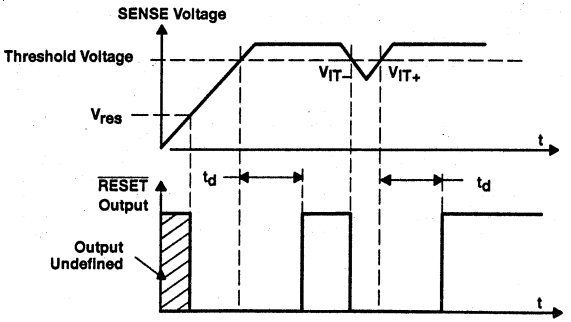
‡ This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617-12.

functional block diagram



§ Outputs are push-pull. External pullup or pulldown resistors are not required.
¶ Nominal value

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 7 V
Input voltage range (see Note 1) ..... −0.3 V to 7 V
Maximum low output current ..... 10 mA
Maximum high output current ..... −10 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) ..... ±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±10 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW

recommended operating conditions at specified temperature range

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	6	V
Timing capacitor, C_t (see Note 2)			100	µF
Input voltage, V_I		0	6	V
High-level input voltage at $\overline{RESIN}$ and CONTROL‡, V_{IH}	V_{DD} = 2 V	1.7		V
	V_{DD} = 2.7 V	1.8		
	V_{DD} = 4.5 V	2		
Low-level input voltage at $\overline{RESIN}$ and CONTROL‡, V_{IL}	V_{DD} = 2 V		0.3	V
	V_{DD} = 2.7 V		0.4	
	V_{DD} = 4.5 V		0.8	
High-level output current, I_{OH}	V_{DD} = 2.7 V		−2.5	mA
	V_{DD} = 4.5 V		−4	
Low-level output current, I_{OL}	V_{DD} = 2.7 V		2.5	mA
	V_{DD} = 4.5 V		4	
Input transition rise and fall rate at $\overline{RESIN}$ and CONTROL input, $\Delta t/\Delta V$			100	ns/V
Operating free-air temperature range, T_A		−40	85	°C

‡ To ensure a low supply current, V_{IL} should be kept <0.3 V and $V_{IH} > V_{DD} - 0.3$ V.

NOTE 2: Limited by the leakage current of the capacitor.

electrical characteristics over recommended operating conditions (unless otherwise noted) (see Note 3)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −20 μA	V_{DD} = 2 V	1.9			V
			V_{DD} = 2.7 V	2.6			
			V_{DD} = 4.5 V	4.4			
		I_{OH} = −4 mA	V_{DD} = 4.5 V	3.7			
V_{OL}	Low-level output voltage	I_{OL} = 20 μA	V_{DD} = 2 V			0.1	V
			V_{DD} = 2.7 V			0.1	
			V_{DD} = 4.5 V			0.1	
		I_{OL} = 4 mA	V_{DD} = 4.5 V			0.4	
V_{IT-}	Negative-going threshold voltage, SENSE (see Note 4)		V_{DD} = 2 V to 6 V	4.5	4.55	4.6	V
V_{hys}	Hysteresis, SENSE		V_{DD} = 2 V to 6 V		40		mV
V_{res}	Power-up reset voltage‡		I_{OL} = 20 μA			1	V
I_I	Input current	RESIN	V_I = 0 V to V_{DD}	−1		1	μA
		CONTROL	V_I = V_{DD}		5	10	
		SENSE	V_I = 5 V		4	8	
I_{DD}	Supply current		V_I = 0 V, $\overline{RESIN}$ = V_{DD}, CONTROL = 0 V, SENSE = V_{DD}, Outputs open		10	20	μA
$I_{DD(d)}$	Supply current during t_d		V_{DD} = 5 V, V_{CT} = 0 V		120	150	μA
C_I	Input capacitance, SENSE		V_I = 0 V to V_{DD}		50		pF

† Typical values apply at T_A = 25°C.

‡ The lowest supply voltage at which $\overline{RESET}$ becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

NOTES: 3. All characteristics are measured with C_T = 0.1 μF.

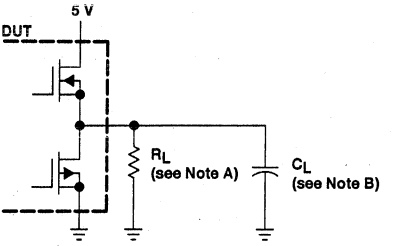
4. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near the supply terminals.

switching characteristics at V_{DD} = 5 V, R_L = 500 Ω, C_L = 50 pF, T_A = 25°C

PARAMETER		DELAY TIME FROM (INPUT)	DELAY TIME TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(H)}$	Effective high-level-input pulse duration	SENSE	RESET and $\overline{\text{RESET}}$	$V_{IH} = V_{IT(max)} + 0.2$ V, $V_{IL} = V_{IT(min)} - 0.2$ V, $\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, CT = NC†	20			µs
$t_{w(L)}$	Effective low-level-input pulse duration				2			
$t_{w(H)}$	Effective high-level-input pulse duration	$\overline{\text{RESIN}}$	RESET and $\overline{\text{RESET}}$	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = $V_{IT(max)} + 0.2$ V, CONTROL = 0.4 V, CT = NC†	20			µs
$t_{w(L)}$	Effective low-level-input pulse duration				2			
t_d	Delay time	SENSE	RESET and $\overline{\text{RESET}}$	$V_{IH} = V_{IT(max)} + 0.2$ V, $\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, CT = 100 nF, See timing diagram	1.5	2.1	3.5	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT(max)} + 0.2$ V, $V_{IL} = V_{IT(min)} - 0.2$ V, $\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						2	
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				2	
t_{PHL}	Propagation delay time, high-to-low-level output						20	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = $V_{T(max)} + 0.2$ V, CONTROL = 0.4 V, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						35	ns
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				45	
t_{PHL}	Propagation delay time, high-to-low-level output						20	µs
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = $V_{T(max)} + 0.2$ V, $\overline{\text{RESIN}}$ = 2.7 V, CT = NC†			30	ns
t_{PHL}	Propagation delay time, high-to-low-level output						35	
t_r	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%		8		ns/V
t_f	Fall time			90% to 10%		4		

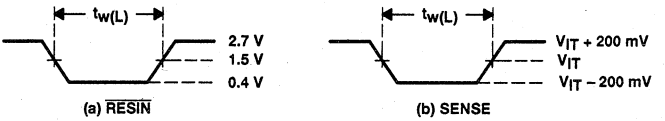
† NC includes up to 100-pF probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. For switching characteristics, R_L = 500 Ω.
B. C_L = 50 pF includes jig and probe capacitance.

Figure 1. RESET AND $\overline{\text{RESET}}$ Output Configurations



WAVEFORMS

Figure 2. Input Pulse Definition

APPLICATION INFORMATION

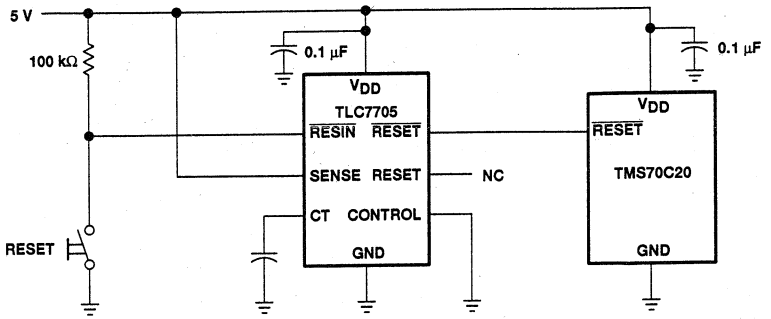


Figure 3. Reset Controller in a Microcomputer System

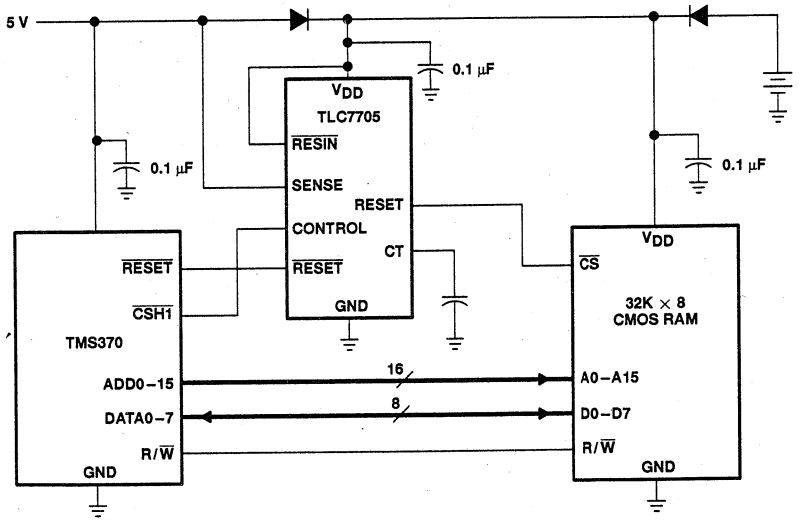


Figure 4. Data Retention During Power Down Using Static CMOS RAMs

D3824, MARCH 1991, REVISED JUNE 1991

- 2.5-V Virtual Ground for 5-V/GND Analog Systems
- Self-Contained in Small Outline, Dual-In-Line or 3-Terminal TO-226AA Packages
- High Output-Current Capability
  Sink or Source . . . 20 mA Typ
- Micropower Operation . . . 170 µA Typ
- Excellent Regulation Characteristics
  Output Regulation = ±45 µV Typ,
  I_O = 0 to ±10mA
  Input Regulation = 1.5 µV/V Typ
- Low-Impedance Output . . . 0.0075 Ω Typ
- Macromodel Included

description

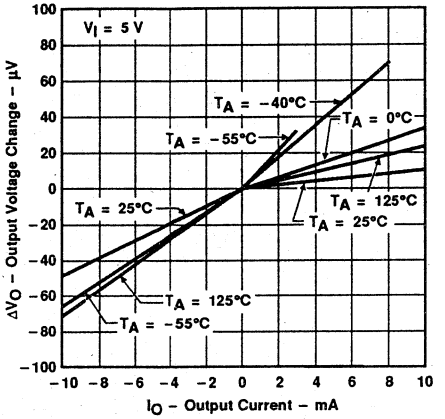
In signal-conditioning applications using a single power source, a reference voltage is required for termination of all signal grounds. To accomplish this, engineers have typically used solutions consisting of resistors, capacitors, operational amplifiers, and voltage references. Texas Instruments has eliminated all of those components with one easy-to-use 3-terminal device. That device is the TLE2425 precision virtual ground.

Use of the TLE2425 over other typical circuit solutions gives the designer increased dynamic signal range, improved signal-to-noise ratio, lower distortion, improved signal accuracy, and easier interfacing to ADCs and DACs. These benefits are the result of combining a precision micropower voltage reference and a high-performance precision operational amplifier in a single silicon chip. It is the precision and performance of these two circuit functions together that yield such dramatic system-level performance.

The TLE2425 improves input regulation as well as output regulation, and in addition reduces output impedance and power dissipation in a majority of virtual-ground-generation circuits. Both input regulation and load regulation exceed 12 bits of accuracy on a single 5-V system. Signal-conditioning front-ends of data acquisition systems that push 12 bits and beyond can use the TLE2425 to eliminate a major source of system error.

The TLE2425C is characterized for operation from 0°C to 70°C. The TLE2425I is characterized for operation from –40°C to 85°C. The TLE2425M is characterized for operation over the full military temperature range of –55°C to 125°C.

OUTPUT REGULATION



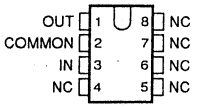
AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC TO-226AA (LP)	CHIP FORM (Y)
0°C to 70°C	TLE2425CD	——	TLE2425CLP	TLE2425Y
–40°C to 85°C	TLE2425ID	——	TLE2425ILP	
–55°C to 125°C	TLE2425MD	TLE2425MJG	TLE2425MLP	

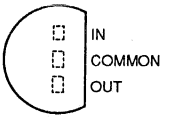
D and LP packages are available taped and reeled in the commercial temperature range only. Add "R" suffix to device type (e.g., TLE2425CDR).

TEXAS INSTRUMENTS

D OR JG PACKAGE
(TOP VIEW)



LP PACKAGE
(TOP VIEW)

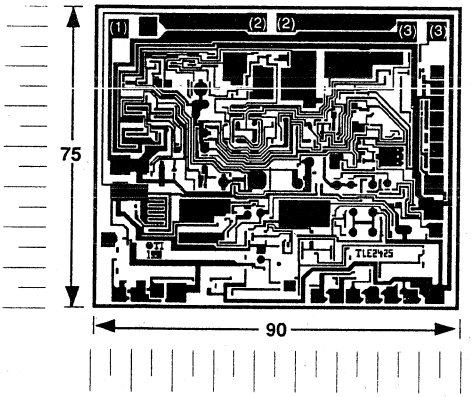


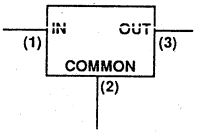
NC – No internal connection.

TLE2425Y chip information

These chips, properly assembled, display characteristics similar to the TLE2425, (see electrical table on page 7). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

Note: Both number-2 bonding pads and both number-3 bonding pads must be bonded out to the corresponding pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Continuous input voltage . . . . . 40 V
Output current, I_O . . . . . ±80 mA
Duration of short-circuit current at (or below) 25°C (see Note 1) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . –40°C to 85°C
M-suffix . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or LP package . . . . . 300°C

NOTE 1: The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
LP	775 mW	6.2 mW/°C	496 mW	403 mW	155 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I	4	40	4	40	4	40	V
Operating free-air temperature, T_A	0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage			25°C	2.48	2.5	2.52	V
			Full range	2.47		2.53	
Temperature coefficient of output voltage			25°C		20		ppm/°C
Bias current	I_O = 0		25°C		170	250	μA
			Full range			250	
Input regulation	V_I = 4.5 V to 5.5 V		25°C		1.5	20	μV
			Full range			25	
	V_I = 4 V to 40 V		25°C		1.5	20	μV/V
			Full range			25	
Ripple rejection	f = 120 Hz, $\Delta V_{I(PP)}$ = 1 V		25°C		80		dB
Output regulation‡ (source current)	I_O = 0 to −10 mA		25°C	−160	−45	160	μV
			Full range	−250		250	
	I_O = 0 to −20 mA		25°C	−450	−150	450	
Output regulation‡ (sink current)	I_O = 0 to 10 mA		25°C	−160	15	160	μV
			Full range	−250		250	
	I_O = 0 to 20 mA		25°C	−235	65	235	
Long-term drift of output voltage	Δt = 1000 h, Noncumulative		25°C		15		ppm
Output impedance			25°C		7.5	22.5	mΩ
Short-circuit output current	Sink current, V_O = 5 V		25°C	30	55		mA
	Source current, V_O = 0			−30	−50		
Output noise voltage, rms	f = 10 Hz to 10 kHz		25°C		100		μV
Output voltage response to output current step	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		110		μs
		C_L = 100 pF			115		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0			180		
		C_L = 100 pF			180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V, V_O to 0.1%		25°C		12		μs
	V_I = 4.5 to 5.5 V, V_O to 0.01%				30		
Output voltage turn-on response	V_I = 0 to 5 V, V_O to 0.1%		25°C		125		μs
	V_I = 0 to 5 V, V_O to 0.01%				210		

†Full range is 0°C to 70°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage			25°C	2.48	2.5	2.52	V
			Full range	2.47		2.53	
Temperature coefficient of output voltage			25°C		20		ppm/°C
Bias current	I_O = 0		25°C		170	250	μA
			Full range			250	
Input regulation	V_I = 4.5 V to 5.5 V		25°C		1.5	20	μV
			Full range			75	
	V_I = 4 V to 40 V		25°C		1.5	20	μV/V
			Full range			75	
Ripple rejection	f = 120 Hz, $\Delta V_{I(PP)}$ = 1 V		25°C		80		dB
Output regulation‡ (source current)	I_O = 0 to −10 mA		25°C	−160	−45	160	μV
			Full range	−250		250	
	I_O = 0 to −20 mA		25°C	−450	−150	450	
Output regulation‡ (sink current)	I_O = 0 to 8 mA		25°C	−160	15	160	μV
			Full range	−250		250	
	I_O = 0 to 20 mA		25°C	−235	65	235	
Long-term drift of output voltage	Δt = 1000 h, Noncumulative		25°C		15		ppm
Output impedance			25°C		7.5	22.5	mΩ
Short-circuit output current	Sink current, V_O = 5 V		25°C	30	55		mA
	Source current, V_O = 0			−30	−50		
Output noise voltage, rms	f =10 Hz to 10 kHz		25°C		100		μV
Output voltage response to output current step	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		110		μs
		C_L = 100 pF			115		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0			180		
		C_L = 100 pF			180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V, V_O to 0.1%		25°C		12		μs
	V_I = 4.5 to 5.5 V, V_O to 0.01%				30		
Output voltage turn-on response	V_I = 0 to 5 V, V_O to 0.1%		25°C		125		μs
	V_I = 0 to 5 V, V_O to 0.01%				210		

†Full range is −40°C to 85°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage			25°C	2.48	2.5	2.52	V
			Full range	2.47		2.53	
Temperature coefficient of output voltage			25°C		20		ppm/°C
Bias current	I_O = 0		25°C		170	250	μA
			Full range			250	
Input regulation	V_I = 4.5 V to 5.5 V		25°C		1.5	20	μV
			Full range			100	
	V_I = 4.5 V to 40 V		25°C		1.5	20	μV/V
			Full range			100	
Ripple rejection	f = 120 Hz, $\Delta V_{I(PP)}$ = 1 V		25°C		80		dB
Output regulation‡ (source current)	I_O = 0 to −10 mA		25°C	−160	−45	160	μV
			Full range	−250		250	
	I_O = 0 to −20 mA		25°C	−450	−150	450	
Output regulation‡ (sink current)	I_O = 0 to 3 mA		25°C	−160	15	160	μV
			Full range	−250		250	
	I_O = 0 to 20 mA		25°C	−235	65	235	
Long-term drift of output voltage	Δt = 1000 h, Noncumulative		25°C		15		ppm
Output impedance			25°C		7.5	22.5	mΩ
Short-circuit output current	Sink current, V_O = 5 V		25°C	30	55		mA
	Source current, V_O = 0			−30	−50		
Output noise voltage, rms	f = 10 Hz to 10 kHz		25°C		100		μV
Output voltage response to output current step	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		110		μs
		C_L = 100 pF			115		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0			180		
		C_L = 100 pF			180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V, V_O to 0.1%		25°C		12		μs
	V_I = 4.5 to 5.5 V, V_O to 0.01%				30		
Output voltage turn-on response	V_I = 0 to 5 V, V_O to 0.1%		25°C		125		μs
	V_I = 0 to 5 V, V_O to 0.01%				210		

†Full range is −55°C to 125°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at V_I = 5 V, I_O = 0, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage			2.48	2.5	2.52	V
Temperature coefficient of output voltage				20		ppm/°C
Bias current	I_O = 0			170	250	µA
Input regulation	V_I = 4.5 V to 5.5 V			1.5	20	µV
	V_I = 4 V to 40 V			1.5	20	µV/V
Ripple rejection	f = 120 Hz, $\Delta V_{I(PP)}$ = 1 V			80		dB
Output regulation (source current)‡	I_O = 0 to –10 mA		–160	–45	160	µV
	I_O = 0 to –20 mA		–450	–150	450	
Output regulation (sink current)‡	I_O = 0 to 10 mA		–160	15	160	µV
	I_O = 0 to 20 mA		–235	65	235	
Output impedance				7.5	22.5	mΩ
Short-circuit output current	Sink current, V_O = 5 V		30	55		mA
	Source current, V_O = 0		–30	–50		
Output noise voltage, rms	f = 10 Hz to 10 kHz			100		µV
Output voltage response to output current step	V_O to 0.1%, I_O = ± 10 mA	C_L = 0		110		µs
		C_L = 100 pF		115		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0		180		
		C_L = 100 pF		180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V, V_O to 0.1%			12		µs
	V_I = 4.5 to 5.5 V, V_O to 0.01%			30		
Output voltage turn-on response	V_I = 0 to 5 V, V_O to 0.1%			125		µs
	V_I = 0 to 5 V, V_O to 0.01%			210		

‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

table of graphs

		FIGURE
Output voltage	Distribution	1
	vs Temperature	2
Output voltage hysteresis	vs Temperature	3
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Input regulation		6
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Spot noise voltage	vs Frequency	11
Wideband noise voltage	vs Frequency	12
Output voltage change with current step	vs Time	13
Output voltage change with voltage step	vs Time	14
Output voltage power-up response	vs Time	15
Stability range	vs Load capacitance	16

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF
OUTPUT VOLTAGE

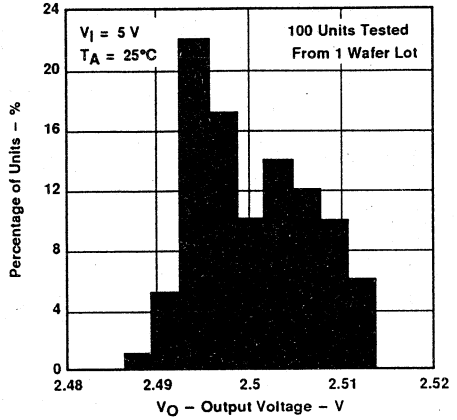


Figure 1

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

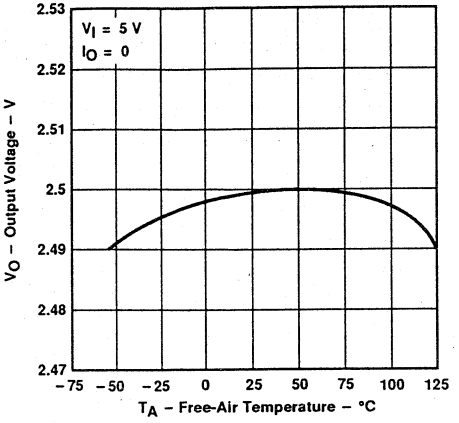


Figure 2

OUTPUT VOLTAGE HYSTERESIS
vs
FREE-AIR TEMPERATURE

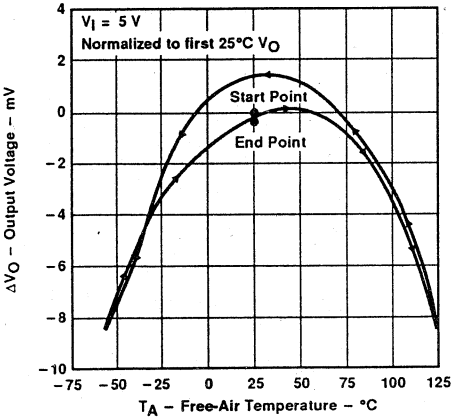


Figure 3

BIAS CURRENT
vs
INPUT VOLTAGE

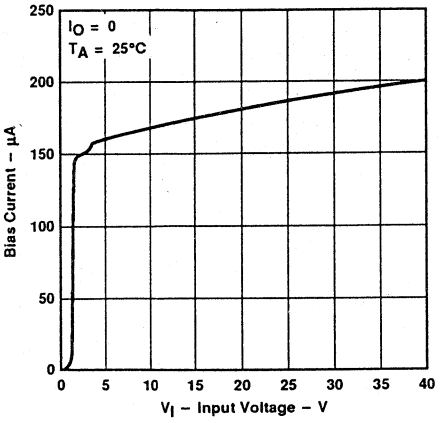


Figure 4

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

BIAS CURRENT
vs
FREE-AIR TEMPERATURE

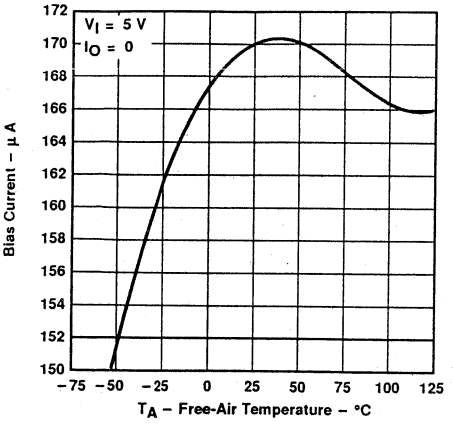


Figure 5

INPUT REGULATION

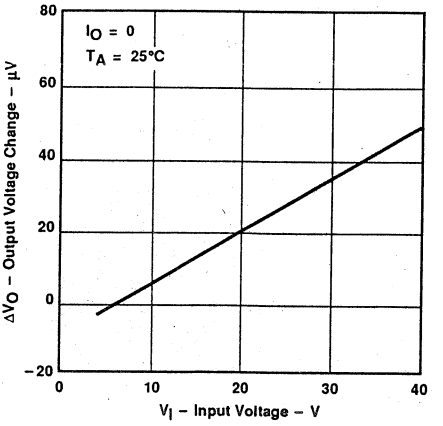


Figure 6

RIPPLE REJECTION
vs
FREQUENCY

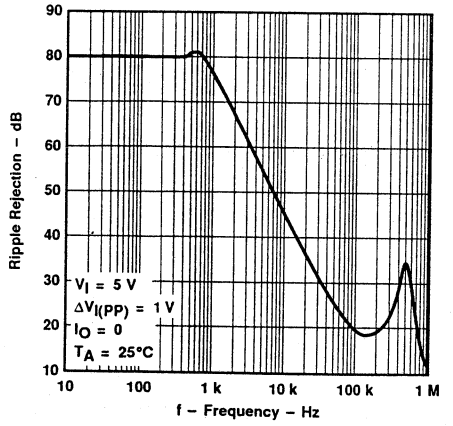


Figure 7

OUTPUT REGULATION

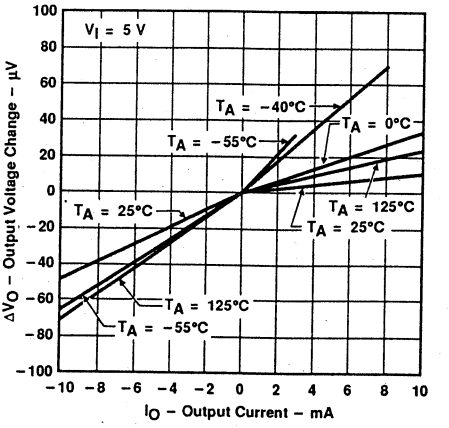


Figure 8

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OUTPUT IMPEDANCE
vs
FREQUENCY

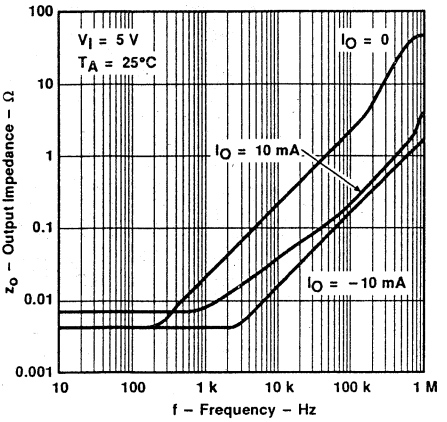


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

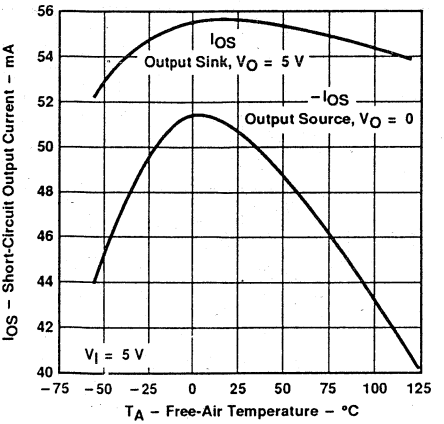


Figure 10

SPOT NOISE VOLTAGE
vs
FREQUENCY

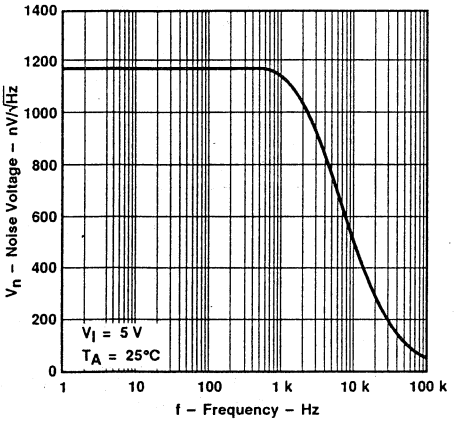


Figure 11

WIDEBAND NOISE VOLTAGE
vs
FREQUENCY

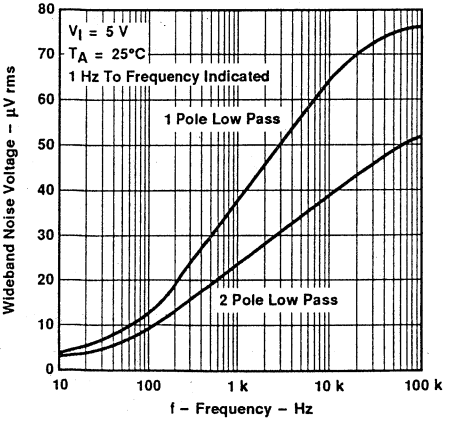


Figure 12

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE TO OUTPUT CURRENT STEP vs TIME

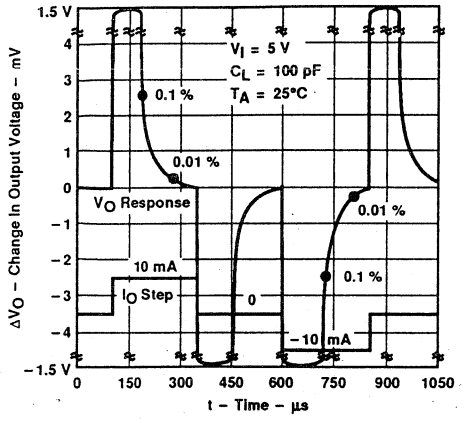


Figure 13

OUTPUT VOLTAGE RESPONSE TO INPUT VOLTAGE STEP vs TIME

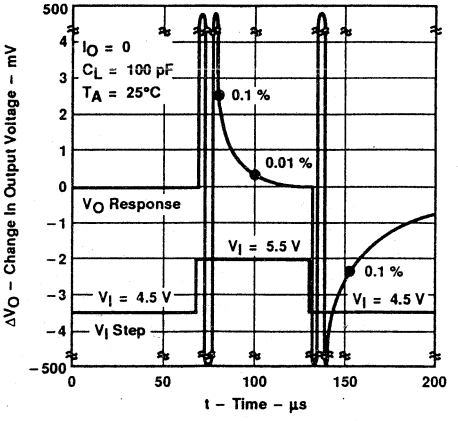


Figure 14

OUTPUT VOLTAGE POWER-UP RESPONSE vs TIME

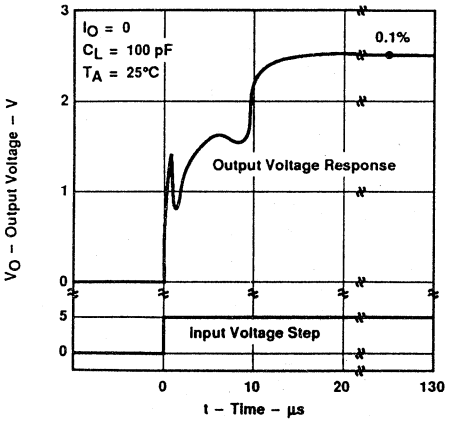


Figure 15

STABILITY RANGE vs LOAD CAPACITANCE

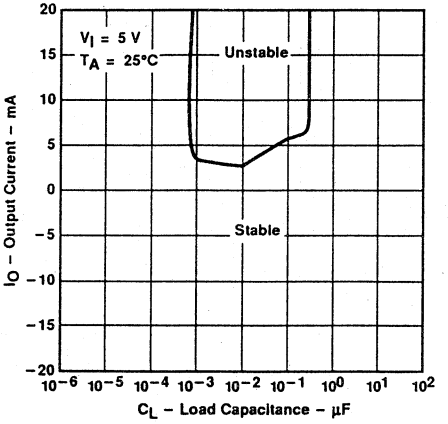


Figure 16

macromodel information

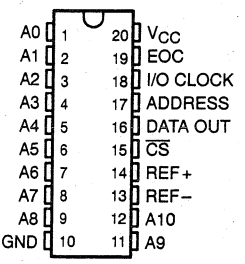
```
* TLE2425 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
* CREATED USING PARTS RELEASE 4.03 ON 08/21/90 AT 13:51
* REV (N/A)       SUPPLY VOLTAGE: 5 V
* CONNECTIONS:    INPUT
*                 | COMMON
*                 | | OUTPUT
*                 | | |
.SUBCKT TLE2425   3 4 5
*
*--------------------------------------------------------------------------------
* OPAMP SECTION
  C1       11   12   21.66E-12
  C2        6    7   30.00E-12
  C3       87    0   10.64E-9
  CPSR     85   86   15.9E-9
  DCM+     81   82   DX
  DCM-     83   81   DX
  DC        5   53   DX
  DE       54    5   DX
  DLP      90   91   DX
  DLN      92   90   DX
  DP        4    3   DX
  ECMR     84   99   (2,99) 1
  EGND     99    0   POLY(2) (3,0) (4,0) 0 .5 .5
  EPSR     85    0   POLY(1) (3,4) -16.22E-6  3.24E-6
  ENSE     89    2   POLY(1) (88,0) 120E-6  1
  FB        7   99   POLY(6) VB VC VE VLP VLN VPSR 0 74.8E6 -10E6 10E6 10E6
+ -10E6 74E6
  GA        6    0   11 12 320.4E-6
  GCM       0    6   10 99 1.013E-9
  GPSR     85   86   (85,86) 100E-6
  GRC1      4   11   (4,11) 3.204E-4
  GRC2      4   12   (4,12) 3.204E-4
  GRE1     13   10   (13,10) 1.038E-3
  GRE2     14   10   (14,10) 1.038E-3
  HLIM     90    0   VLIM 1K
  HCMR     80    1   POLY(2) VCM+ VCM- 0 1E2 1E2
  IRP       3    4   146E-6
  IEE       3   10   DC 24.05E-6
  IIO       2    0   .2E-9
  I1       88    0   1E-21
  Q1       11   89   13 QX
  Q2       12   80   14 QX
  R2        6    9   100.0E3
  RCM      84   81   1K
  REE      10   99   8.316E6
  RN1      87    0   2.55E8
  RN2      87   88   11.67E3
```

macromodel information (continued)

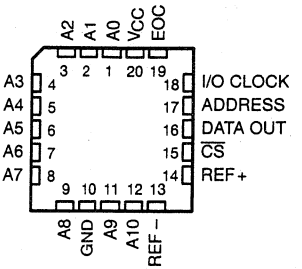
```
  RO1      8    5   63
  RO2      7   99   62
  VCM+    82   99   1.0
  VCM-    83   99   -2.3
  VB       9    0   DC 0
  VC       3   53   DC 1.400
  VE      54    4   DC 1.400
  VLIM     7    8   DC 0
  VLP     91    0   DC 30
  VLN      0   92   DC 30
  VPSR     0   86   DC 0
  RFB      5    2   1K
  RIN     30    1   1K
  RCOM    34    4   .1
*REGULATOR SECTION
  RG1     30    0   20MEG
  RG2     30   31   .2
  RG3     31   35   400K
  RG4     35   34   411K
  RG5     31   36   25MEG
  HREG    31   32   POLY(2) VPSET VNSET 0 1E2 1E2
  VREG    32   33   DC 0V
  EREG    33   34   POLY(1) (36,34) 1.23 1
  VADJ    36   34   1.27V
  HPSET   37    0   VREG 1.030E3
  VPSET   38    0   DC 20V
  HNSET   39    0   VREG 6.11E5
  VNSET   40    0   DC -20V
  DSUB     4   34   DX
  DPOS    37   38   DX
  DNNEG   40   39   DX
.MODEL DX D(IS=800.0E-18)
.MODEL QX PNP(IS=800.0E-18 BF=480)
.ENDS
```

- **Advanced LinEPIC™ Technology**
- **3.3-V Supply Operation**
- **10-Bit-Resolution A/D Converter**
- **11 Analog Input Channels**
- **Three Built-In Self-Test Modes**
- **Inherent Sample and Hold**
- **Total Unadjusted Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion (EOC) Output**
- **Pin Compatible With TLC1543**

DW, FK, J, OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLV1543C and TLV1543M are Advanced LinEPIC™ 10-bit, switched-capacitor, successive-approximation, analog-to-digital converters. These devices have three inputs and a 3-state output [chip select ($\overline{CS}$), input-output clock (I/O CLOCK), address input (ADDRESS), and data output (DATA OUT)] that provide a direct four-wire interface to the serial port of a host processor. The devices allow high-speed data transfers from the host.

In addition to a high-speed A/D converter and versatile control capability, these devices have an on-chip 14-channel multiplexer that can select any one of 11 analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of A/D conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

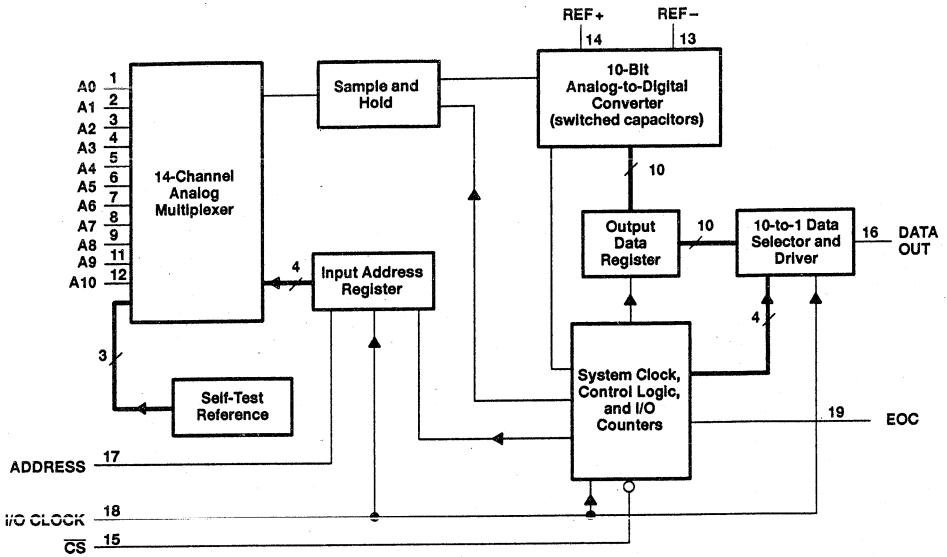
The TLV1543C is characterized for operation from 0°C to 70°C. The TLV1543M is characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGE				
	SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	PLASTIC CHIP CARRIER (FN)
0°C to 70°C	TLV1543CDW	—	—	TLV1543CN	TLV1543CFN
−55°C to 125°C	—	TLV1543MFK	TLV1543MJ	—	—

Advanced LinEPIC is a trademark of Texas Instruments Incorporated.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDRESS	17	I	Serial address. A 4-bit serial address selects the desired analog input or test voltage that is to be converted next. The address data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits have been read into the address register, ADDRESS is ignored for the remainder of the current conversion period.
A0–A10	1–9, 11, 12	I	Analog signal. The 11 analog inputs are applied to A0–A10 and are internally multiplexed. The driving source impedance should be less than or equal to 1 kΩ.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT, ADDRESS, and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables ADDRESS and I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
EOC	19	O	End of conversion. EOC goes from a high- to a low- logic level on the trailing edge of the tenth I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10	I	The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial I/O CLOCK input and performs the following four functions: 1) It clocks the four input address bits into the address register on the first four rising edges of I/O CLOCK with the multiplex address available after the fourth rising edge. 2) On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 3) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 4) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	14	I	The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to REF+ and the voltage applied to the REF– terminal.
REF–	13	I	The lower reference voltage value (nominally ground) is applied to REF–.
V_{CC}	20	I	Positive supply voltage

detailed description

With chip select ($\overline{CS}$) inactive (high), the ADDRESS and I/O CLOCK inputs are initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{CS}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and ADDRESS and the removal of DATA OUT from the high-impedance state. The host then provides the 4-bit channel address to ADDRESS and the I/O CLOCK sequence to I/O CLOCK. During this transfer, the host serial interface also receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host. The first four I/O clocks load the address register with the 4-bit address on ADDRESS selecting the desired analog channel and the next six clocks providing the control timing for sampling the analog input.

detailed description (continued)

There are six basic serial interface timing modes that can be used with the device. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{CS}$ as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, (2) a fast mode with a 10-clock transfer and $\overline{CS}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, (4) a fast mode with a 16-bit transfer and $\overline{CS}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, and (6) a slow mode with a 16-clock transfer and $\overline{CS}$ active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{CS}$ in mode 1, mode 3, and mode 5, on the rising edge of EOC in mode 2 and mode 4, and following the 16th clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the 10th clock falling edge, the EOC output goes low and returns to the high logic level when conversion is complete and the result can be read by the host. On the 10th clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of $\overline{CS}$, the number of I/O serial transfer clocks that can be used, and the timing edge on which the MSB of the previous conversion appears at the output.

Table 1. Mode Operation

MODES		$\overline{CS}$	NO. OF I/O CLOCKS	MSB AT DATA OUT†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	$\overline{CS}$ falling edge	Figure 9
	Mode 2	Low continuously	10	EOC rising edge	Figure 10
	Mode 3	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 11
	Mode 4	Low continuously	16‡	EOC rising edge	Figure 12
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 13
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 14

† These edges also initiate serial-interface communication.
‡ No more than 16 clocks should be used.

fast modes

The device is in a fast mode when the serial I/O CLOCK data transfer is completed before the conversion is completed. With a 10-clock serial transfer, the device can only run in a fast mode since a conversion does not begin until the falling edge of the 10th I/O CLOCK.

mode 1: fast mode, $\overline{CS}$ inactive (high) between conversion cycles, 10-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, $\overline{CS}$ active (low) continuously, 10-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

mode 3: fast mode, $\overline{CS}$ inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

slow modes

In a slow mode, the conversion is completed before the serial I/O CLOCK data transfer is completed. A slow mode requires a minimum 11-clock transfer into I/O CLOCK, and the rising edge of the 11th clock must occur before the conversion period is complete; otherwise, the device loses synchronization with the host serial interface, and $\overline{CS}$ has to be toggled to initialize the system. The 11th rising edge of the I/O CLOCK must occur within 9.5 µs after the 10th I/O clock falling edge.

mode 5: slow mode, $\overline{CS}$ inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. The falling edge of the 16th I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

address bits

The 4-bit analog channel-select address for the next conversion cycle is presented to the ADDRESS terminal (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. This address selects one of 14 inputs (11 analog inputs or 3 internal test inputs).

analog inputs and test modes

The 11 analog inputs and the 3 internal test inputs are selected by the 14-channel multiplexer according to the input address as shown in Tables 2 and 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK, and sampling continues for six I/O CLOCK periods. The sample is held on the falling edge of the 10th I/O CLOCK. The three test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs.

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO ADDRESS INPUT	
	BINARY	HEX
A0	0000	0
A1	0001	1
A2	0010	2
A3	0011	3
A4	0100	4
A5	0101	5
A6	0110	6
A7	0111	7
A8	1000	8
A9	1001	9
A10	1010	A

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED†	VALUE SHIFTED INTO ADDRESS INPUT		OUTPUT RESULT (HEX)‡
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

† V_{ref+} is the voltage applied to the REF+ input, and V_{ref-} is the voltage applied to the REF– input.

‡ The output results shown are the ideal values and vary with the reference stability and with internal offsets.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half the V_{CC} voltage), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

converter and analog input (continued)

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

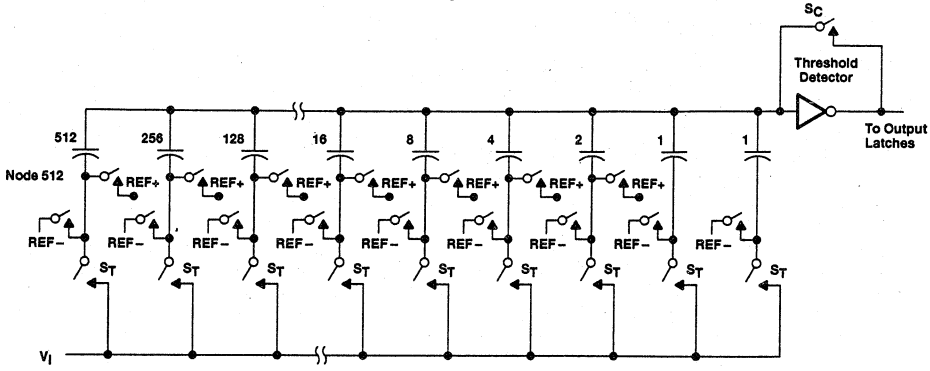


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of $\overline{CS}$ starts all modes of operation, and $\overline{CS}$ can abort a conversion sequence in any mode. A high-to-low transition on $\overline{CS}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent $\overline{CS}$ from being taken low close to completion of conversion because the output data can be corrupted.

reference voltage inputs

There are two reference inputs used with these devices: REF+ and REF–. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading, respectively. The values of REF+, REF–, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF–.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1):	TLV1543C	−0.5 V to 6.5 V
	TLV1543M	−0.5 V to 6 V
Input voltage range, V_I (any input)		−0.3 V to V_{CC} + 0.3 V
Output voltage range		−0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+}		V_{CC} + 0.1 V
Negative reference voltage, V_{ref-}		−0.1 V
Peak input current (any input)		±20 mA
Peak total input current (all inputs)		±30 mA
Operating free-air temperature range, T_A:	TLV1543C	0°C to 70°C
	TLV1543M	−55°C to 125°C
Storage temperature range		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds		260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	TLV1543C		3	3.3	5.5	V
	TLV1543M		3	3.3	3.6	V
Positive reference voltage, V_{ref+} (see Note 2)				V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)				0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)			2.5	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	V
High-level control input voltage, V_{IH}	TLV1543C	V_{CC} = 3 V to 5.5 V	2			V
	TLV1543M	V_{CC} = 3 V to 3.6 V	2			V
Low-level control input voltage, V_{IL}	TLV1543C	V_{CC} = 3 V to 5.5 V			0.6	V
	TLV1543M	V_{CC} = 3 V to 3.6 V			0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$ (see Figure 4)			100			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$ (see Figure 4)			0			ns
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			1.425			µs
Clock frequency at I/O CLOCK (see Note 4)	TLC1543C		0		1.1	MHz
	TLC1543M		0		2.1	
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$			190			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$			190			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 5)					1	µs
Transition time, ADDRESS and $\overline{CS}$, $t_{t(CS)}$					10	µs
Operating free-air temperature, T_A	TLV1543C		0		70	°C
	TLV1543M		−55		125	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.

3. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
4. For 11- to 16-bit transfers, after the 10th I/O CLOCK falling edge (≤ 2 V), at least 1 I/O clock rising edge (≥ 2 V) must occur within 9.5 µs.
5. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 3$ V to 5.5 V, I/O CLOCK frequency = 1.1 MHz for the TLV1543C, $V_{CC} = V_{ref+} = 3$ V to 3.6 V, I/O CLOCK frequency = 2.1 MHz for the TLV1543M (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	TLV1543C	V_{CC} = 3 V,	I_{OH} = −1.6 mA	2.4			V
			V_{CC} = 3 V to 5.5 V,	I_{OH} = 20 μA	V_{CC}−0.1			V
		TLV1543M	V_{CC} = 3 V,	I_{OH} = −1.6 mA	2.4			V
			V_{CC} = 3 V to 3.6 V,	I_{OH} = 20 μA	V_{CC}−0.1			V
V_{OL}	Low-level output voltage	TLV1543C	V_{CC} = 3 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 3 V to 5.5 V,	I_{OL} = 20 μA			0.1	V
		TLV1543M	V_{CC} = 3 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 3 V to 3.6 V,	I_{OL} = 20 μA			0.1	V
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	μA
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			0.8	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC},	Unselected channel at 0 V			1	μA
			Selected channel at 0 V,	Unselected channel at V_{CC}			−1	μA
	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND			10	μA
C_i	Input capacitance, Analog inputs	TLV1543C				7	55	pF
		TLV1543M				7		
	Input capacitance, Control inputs	TLV1543C				5	15	pF
		TLV1543M				5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 3 V to 5.5 V, I/O CLOCK frequency = 1.1 MHz for the TLV1543C, $V_{CC} = V_{ref+}$ = 3 V to 3.6 V, I/O CLOCK frequency = 2.1 MHz for the TLV1543M

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error (see Note 6)				±1	LSB
	Zero error (see Note 7)	See Note 2			±1	LSB
	Full-scale error (see Note 7)	See Note 2			±1	LSB
	Total unadjusted error (see Note 8)				±1	LSB
	Self-test output code (see Table 3 and Note 9)	ADDRESS = 1011		512		
		ADDRESS = 1100		0		
		ADDRESS = 1101		1023		
t_{conv}	Conversion time	See Figures 9–14			21	µs
t_c	Total cycle time (access, sample, and conversion)	See Figures 9–14 and Note 10			21 +10 I/O CLOCK periods	µs
t_{acq}	Channel acquisition time (sample)	See Figures 9–14 and Note 10			6	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 6	10			ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 6			240	ns
$t_{d(I/O-EOC)}$	Delay time, 10th I/O CLOCK↓ to EOC↓	See Figure 7		70	240	ns
$t_{d(EOC-DATA)}$	Delay time, EOC↑ to DATA OUT (MSB)	See Figure 8			100	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB driven)	See Figure 3			1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 3			150	ns
$t_{r(EOC)}$	Rise time, EOC	See Figure 8			300	ns
$t_{f(EOC)}$	Fall time, EOC	See Figure 7			300	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 6			300	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 6			300	ns
$t_{d(I/O-CS)}$	Delay time, 10th I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 11)				9	µs

† All typical values are at T_A = 25°C.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.

6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero, and full-scale errors.
9. Both the input address and the output codes are expressed in positive logic.
10. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 6).
11. Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a setup time plus two falling edges of the internal clock (1.425 µs) after the transition.

PARAMETER MEASUREMENT INFORMATION

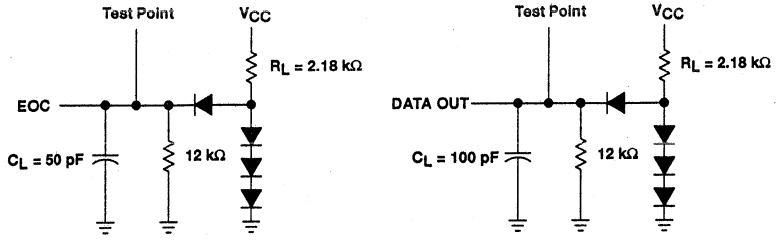


Figure 2. Load Circuits

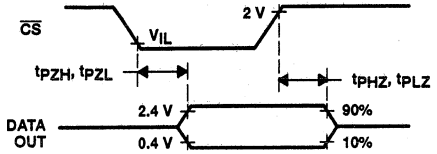


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

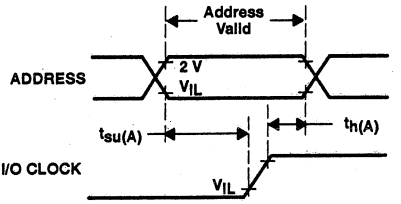


Figure 4. ADDRESS Setup Voltage Waveforms

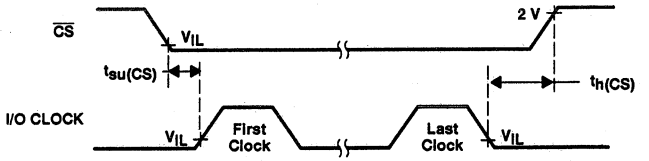


Figure 5. $\overline{CS}$ and I/O CLOCK Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

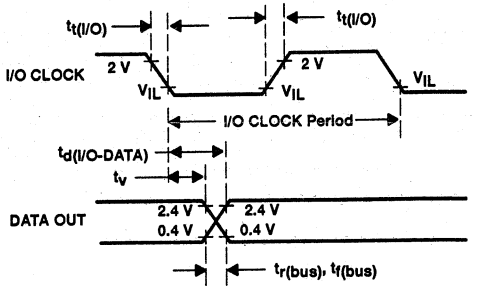


Figure 6. DATA OUT and I/O CLOCK Voltage Waveforms

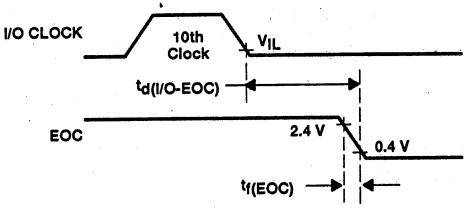


Figure 7. I/O CLOCK and EOC Voltage Waveforms

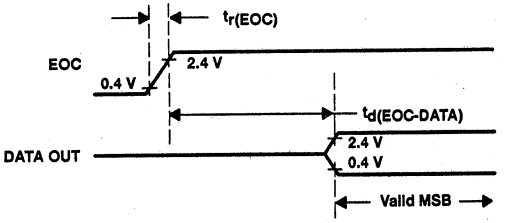


Figure 8. EOC and DATA OUT Voltage Waveforms

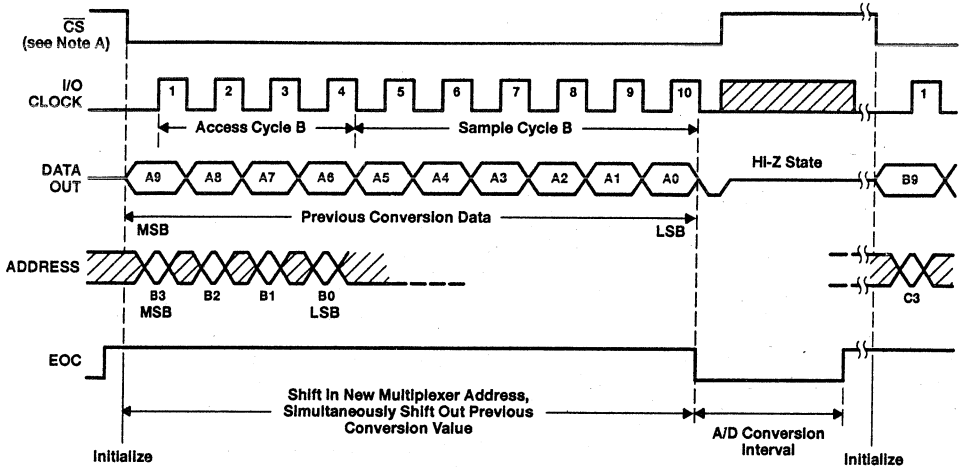


Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$

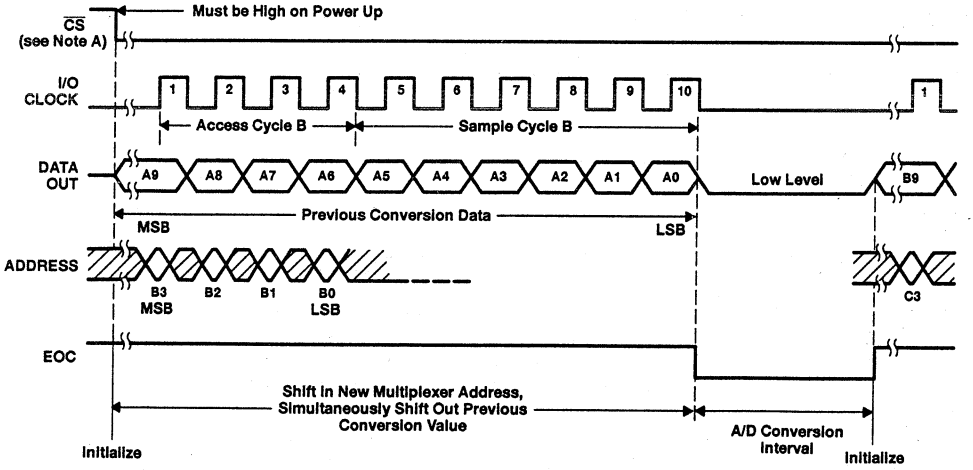


Figure 10. Timing for 10-Clock Transfer Not Using $\overline{CS}$

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

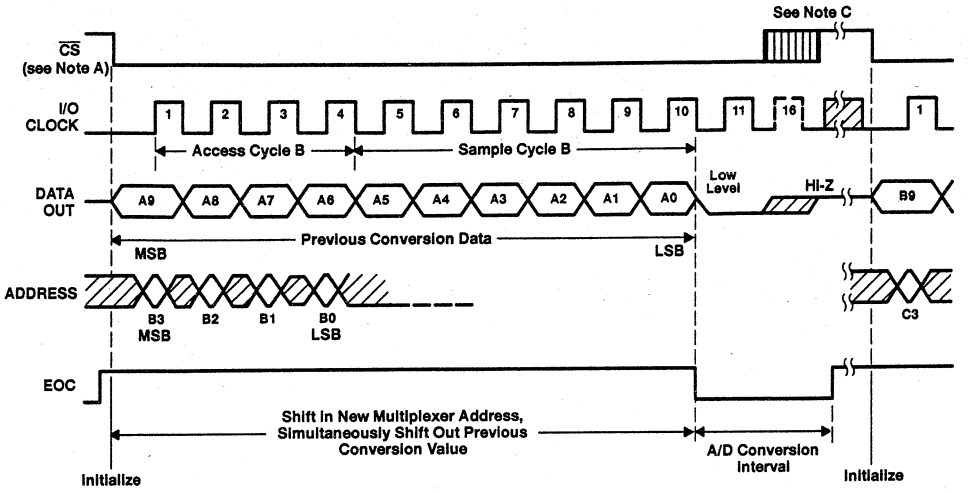


Figure 11. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

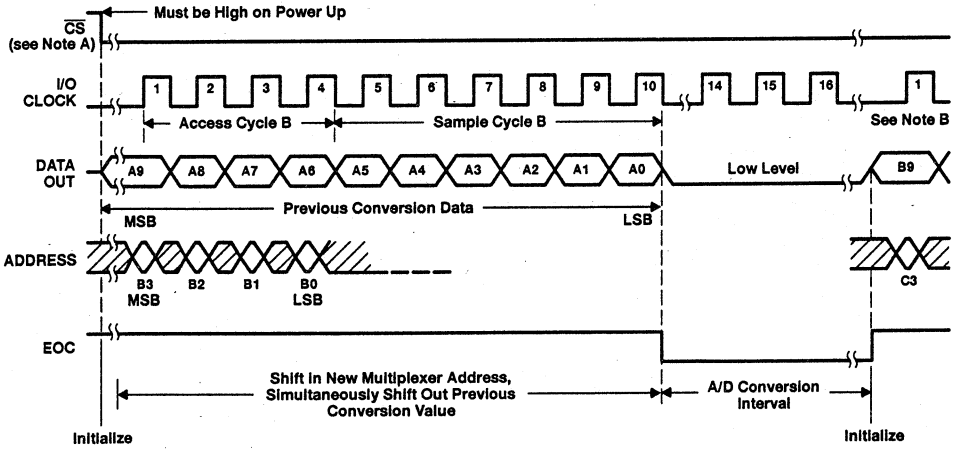


Figure 12. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The first I/O CLOCK must occur after the rising edge of EOC.

C. A low-to-high transition of $\overline{CS}$ disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

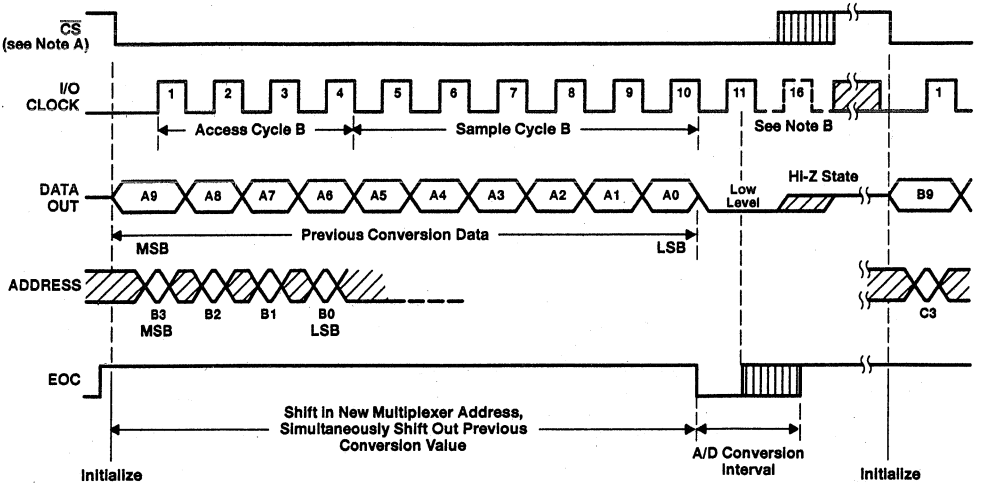


Figure 13. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

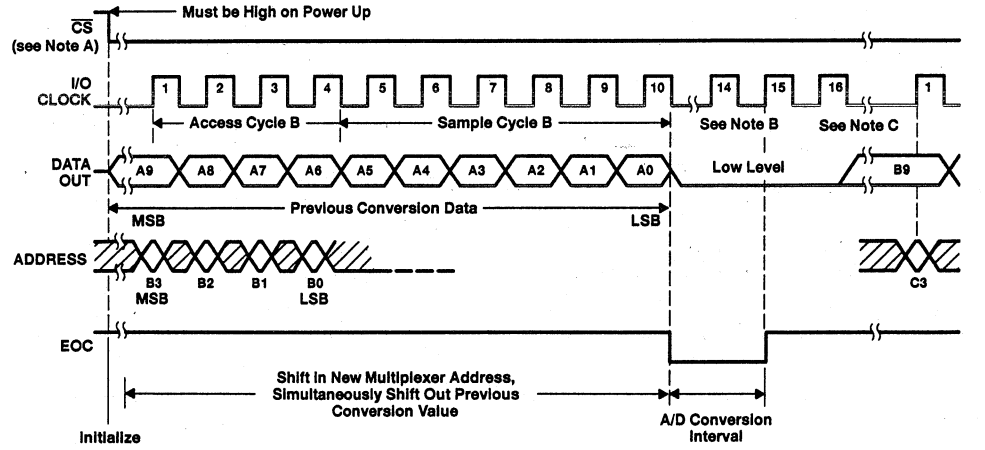


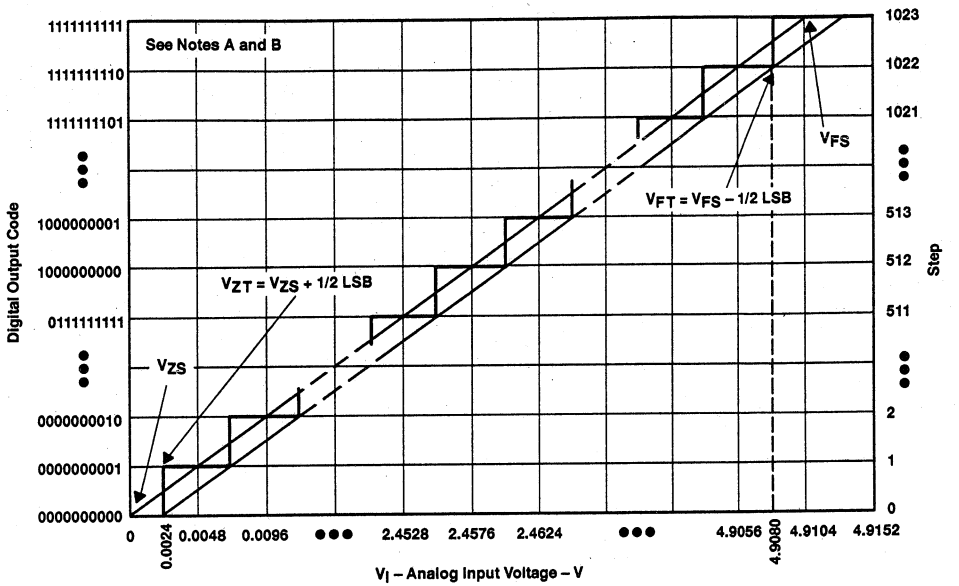
Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum chip $\overline{CS}$ setup time has elapsed.

B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

C. The I/O CLOCK sequence is exactly 16 clock pulses long.

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V and the transition to full scale (V_{FT}) is 4.908 V. 1 LSB = 4.8 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 15. Ideal Conversion Characteristics

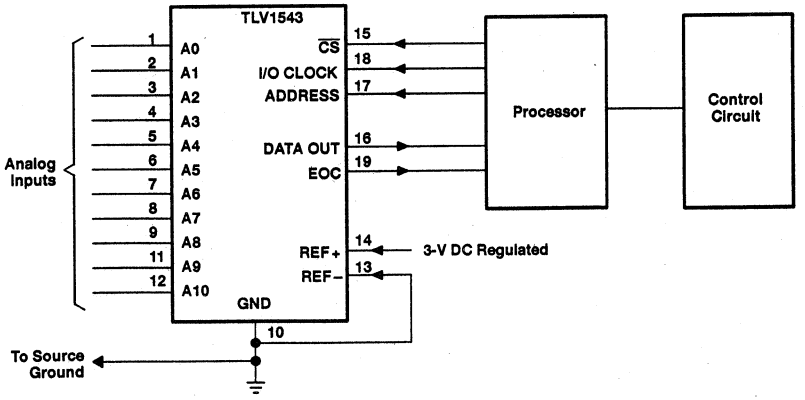
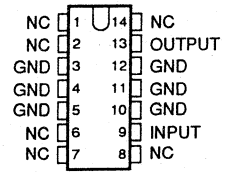


Figure 16. Serial Interface

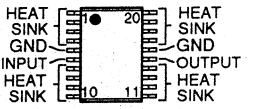
- Fixed 3.3-V Output
- ±1% Maximum Output Voltage Tolerance at T_J = 25°C
- 500-mV Maximum Dropout Voltage at 500 mA
- 500-mA Output Current
- ±2% Absolute Output Voltage Variation
- Internal Overcurrent Limiting
- Internal Thermal Overload Protection
- Internal Overvoltage Protection

N PACKAGE
(TOP VIEW)



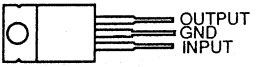
NC – No internal connection

PW PACKAGE
(TOP VIEW)



HEAT SINK – These pins have an internal resistive connection to ground and should be grounded.

KC PACKAGE
(TOP VIEW)



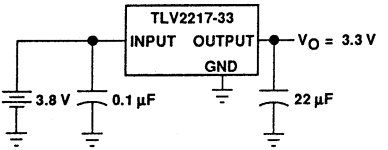
description

The TLV2217-33 is a low-dropout 3.3-V fixed voltage regulator. The regulator is capable of sourcing 500 mA of current with an input-output differential of 0.5 V or less. The TLV2217-33 provides internal overcurrent limiting, thermal overload protection, and overvoltage protection.

The 0.5-V dropout for the TLV2217-33 makes it ideal for battery applications in 3.3-V logic systems. For example, battery input voltage to the regulator may drop as low as 3.8 V, and the TLV2217-33 will continue to regulate the system. For higher voltage systems, the TLV2217-33 may be operated with a continuous input voltage of 12 V.

The TLV2217-33N and TLV2217-33KC cannot be harmed by temporary mirror image insertion. This regulator is characterized for operation from 0°C to 125°C virtual junction temperature.

typical application schematic



AVAILABLE OPTIONS

T_J	PACKAGE			CHIP FORM (Y)
	PLASTIC POWER (KC)	PLASTIC DIP (N)	SURFACE MOUNT (PW)†	
0°C to 125°C	TLV2217-33KC	TLV2217-33N	TLV2217-33PWLE	TLV2217-33Y

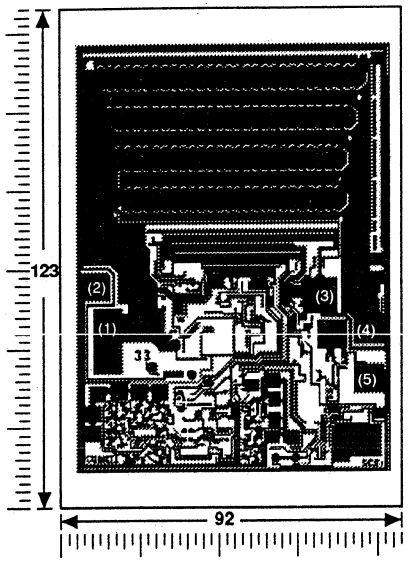
†The PW package is only available left-end taped and reeled.

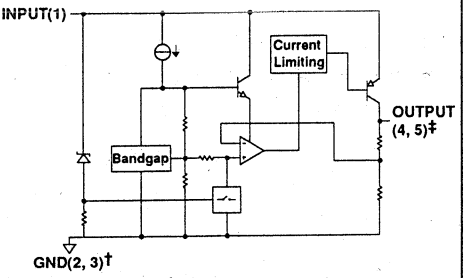
TEXAS INSTRUMENTS

TLV2217-33Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2217-33 (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
11 TYPICAL

BONDING PADS:
7 X 7 MINIMUM

T_J max = 150°C

TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

†Must connect pads 2 and 3 together
‡Must connect pads 4 and 5 together

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)

Continuous input voltage . . . . . 16 V
Continuous total dissipation (see Note 1) . . . . . See Dissipation Rating Table
Operating virtual junction temperature range . . . . . – 55°C to 150°C
Storage temperature range . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
KC	T_A	2000 mW	16.0 mW/°C	1280 mW	1040 mW	400 mW
	T_C†	20000 mW	182.0 mW/°C	14540 mW	11810 mW	4645 mW
N	T_A	2250 mW	18.0 mW/°C	1440 mW	1170 mW	450 mW
	T_C	11850 mW	94.8 mW/°C	7584 mW	6162 mW	2370 mW
PW	T_A	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
	T_C	4625 mW	37.0 mW/°C	2960 mW	2405 mW	925 mW

†Derate above 40°C

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

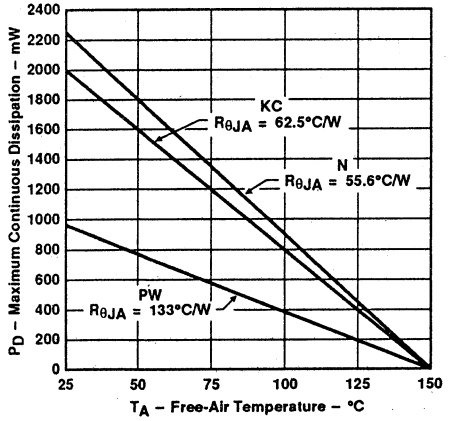


Figure 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

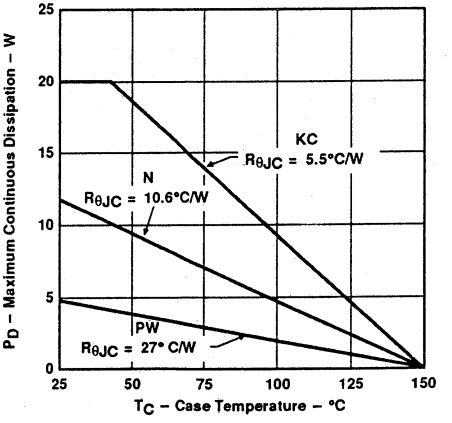


Figure 2

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	3.80	12.0	V
Output current, I_O	0	500	mA
Operating virtual junction temperature range, T_J	0	125	°C

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TLV2217-33			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.8 V to 5.5 V	T_J = 25° C	3.267	3.30	3.333	V
		T_J = 0°C to 125°C	3.234		3.366	
Input regulation	V_I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{pp}			–62		dB
Output regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 500 mA				500	
Bias current	I_O = 0			2	5	mA
	I_O = 500 mA			19	49	

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TLV2217-33Y			UNIT
		MIN	TYP	MAX	
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.8 V to 5.5 V	3.267	3.30	3.333	V
Input regulation	V_I = 3.8 V to 5.5 V		5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{pp}		–62		dB
Output regulation	I_O = 20 mA to 500 mA		5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Dropout voltage	I_O = 250 mA			400	mV
	I_O = 500 mA			500	
Bias current	I_O = 0		2	5	mA
	I_O = 500 mA		19	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

COMPENSATION CAPACITOR SELECTION INFORMATION

The TLV2217-33 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can be used to establish the capacitance value and ESR range for best regulator performance.

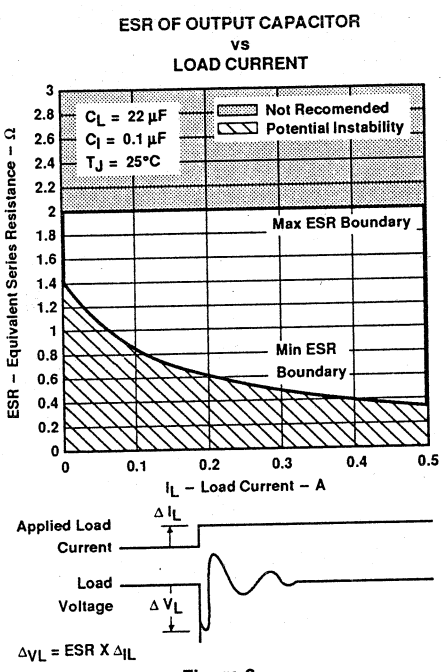


Figure 3

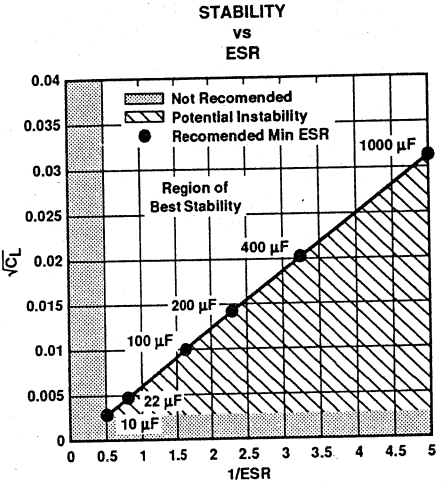
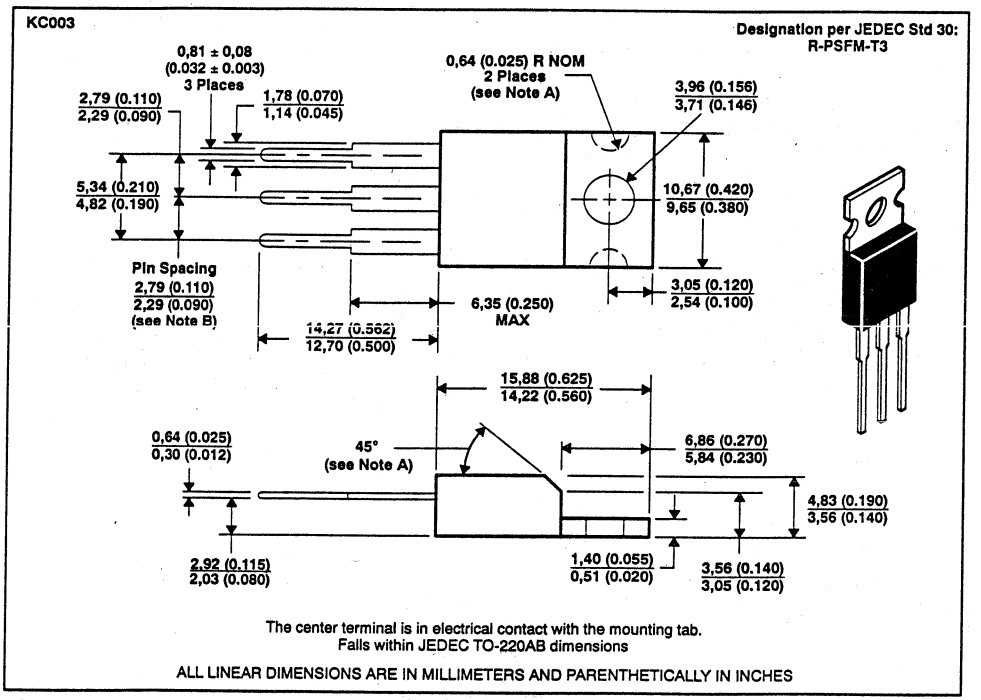


Figure 4

MECHANICAL DATA

KC003
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

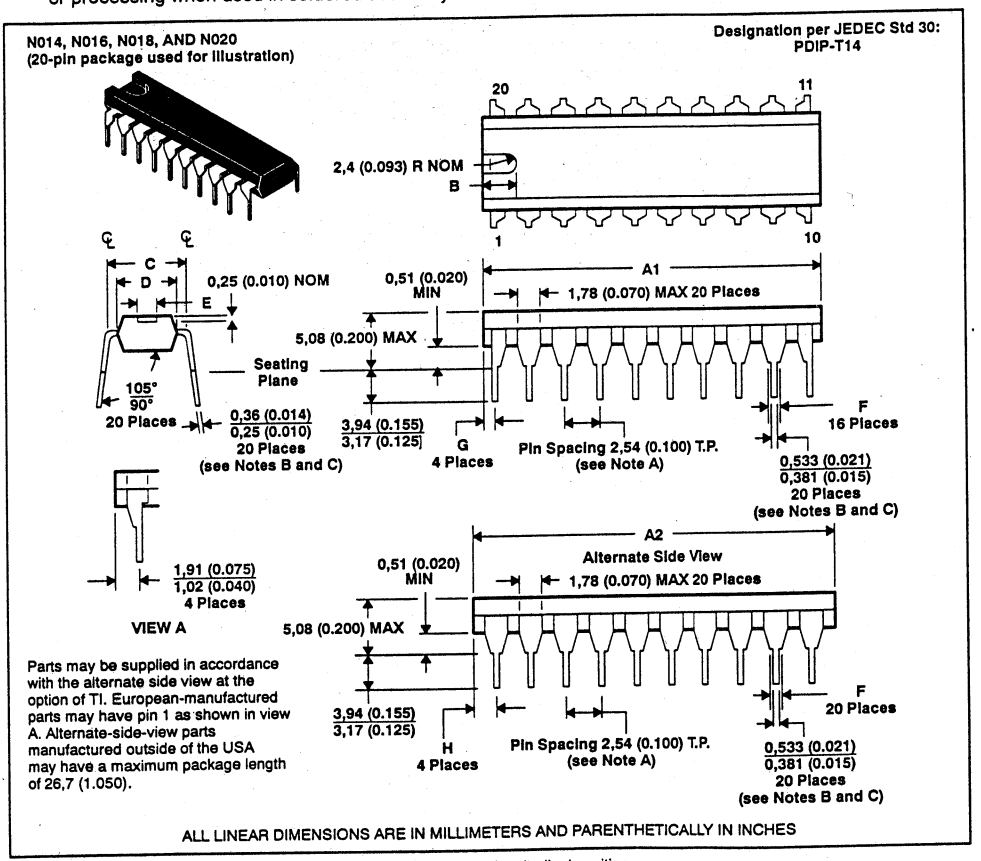


NOTES: A. Notches and/or mold chamfer may or may not be present.
B. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

MECHANICAL DATA

N014, N016, N018, and N020
300-mil plastic dual-in-line package

These dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

MECHANICAL DATA

N014, N016, N018, and N020
300-mil plastic dual-in-line package (continued)

DIM \ PIN		14	16	18	20
A	MIN	18,0 (0.710)	(see Note A)	(see Note A)	23,22 (0.914)
	MAX	19,8 (0.780)	19,8 (0.780)	23,4 (0.920)	24,77 (0.975)
B	NOM	2,8 (0.110)	2,8 (0.110)	4,06 (0.160)	2,80 (0.110)
C	MIN	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)
	MAX	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)
D	MIN	6,10 (0.240)	6,10 (0.240)	(see Note A)	6,10 (0.240)
	MAX	6,60 (0.260)	6,60 (0.260)	6,99 (0.275)	7,11 (0.280)
E	NOM	2,0 (0.080)	2,0 (0.080)	2,03 (0.080)	2,0 (0.080)
F	MIN	0,84 (0.033)	0,84 (0.033)	0,89 (0.035)	0,84 (0.033)
G	MIN	(see Note B)	0,38 (0.015)	(See Note B)	1,68 (0.066)
	MAX	(see Note B)	1,65 (0.065)	(see Note B)	0,22 (0.009)
H	MIN	2,54 (0.100)	1,02 (0.040)	0,23 (0.009)	0,38 (0.015)
	MAX	1,52 (0.060)	2,41 (0.095)	1,91 (0.075)	1,27 (0.050)

NOTES: A. This packaging characteristic is not specified.
B. The 14-pin and 18-pin plastic dual-in-line package is only offered with the external pins shaped in their entirety.

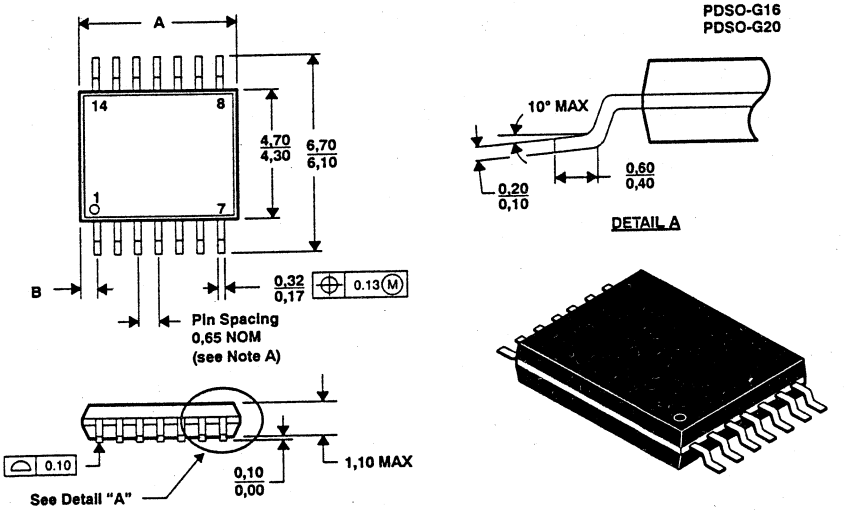
MECHANICAL DATA

PW008, PW014, PW016, PW020
shrink small-outline packages

These shrunk small-outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

PW008, PW014, PW016, PW020
(14-pin package used for illustration)

Designation per JEDEC Std 30:
PDSO-G8
PDSO-G14
PDSO-G16
PDSO-G20



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

NOTES: A. Leads are within 0,25-mm radius of true position at maximum material condition.
B. Body dimensions include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 mm.
D. Lead tips to be planar within ±0,051 mm exclusive of solder.

DIM \ PINS	8	14	16	20
A MIN	2,99	4,99	4,99	6,40
A MAX	3,03	5,30	5,30	6,80
B MAX	0,65	0,70	0,38	0,48

- Output Swing Includes Both Supply Rails
- Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Very Low Power . . . 34 μA Per Channel Typ
- Common-Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Voltage 850 μV Max at T_A = 25°C
- Wide Supply Voltage Range 2.7 V to 8 V
- Macromodel Included

description

The TLV2252 and TLV2252A are dual operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices are optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with μ-power dissipation levels, the input noise voltage performance has been dramatically improved using optimized design techniques for CMOS-type amplifiers. Another added benefit is that these amplifiers exhibit rail-to-rail output swing. Figure 1 graphically depicts the high-level output voltage for different levels of output current for a 3-V single supply. The output dynamic range can be extended using the TLV2252 with loads referenced midway between the rails. The common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ± 5 mV, allowing a minimum of 0 to 2-V common-mode input voltage range for a 3-V supply. Furthermore, at 34 μA (typical) of supply current per amplifier, the TLV2252 family can achieve input offset voltage levels as low as 850 μV, outperforming existing CMOS amplifiers. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

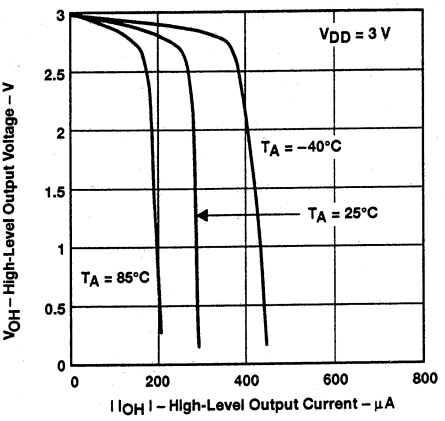


Figure 1

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	850 μV	TLV2252AID	TLV2252AIP	TLV2252AIPWLE	TLV2252Y
	1500 μV	TLV2252ID	TLV2252IP	—	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2252IDR).
The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

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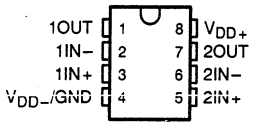
TEXAS INSTRUMENTS

description (continued)

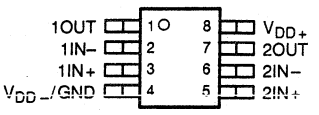
The TLV2252 and TLV2252A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to ADCs. All of these features combined with its temperature performance make the TLV2252 family ideal for remote pressure sensors, temperature control, active VR sensors, accelerometers, hand-held metering, and many other applications.

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

D OR P PACKAGE
(TOP VIEW)



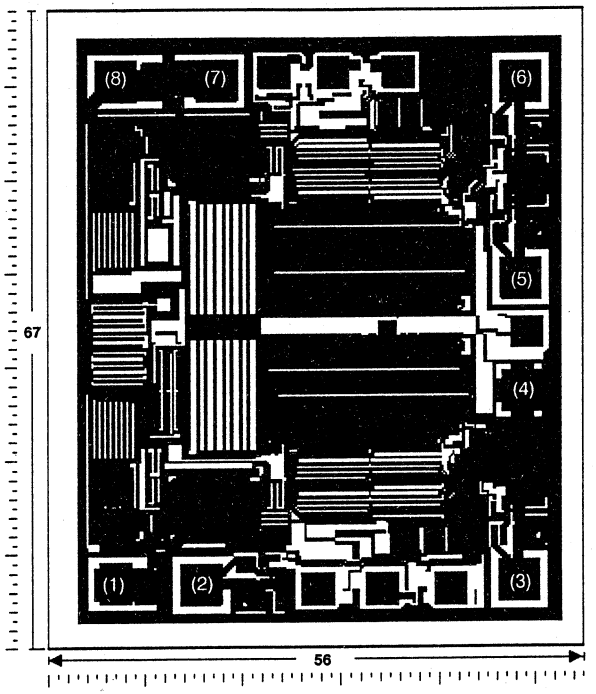
PW PACKAGE
(TOP VIEW)

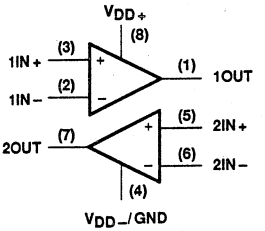


TLV2252Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2252. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

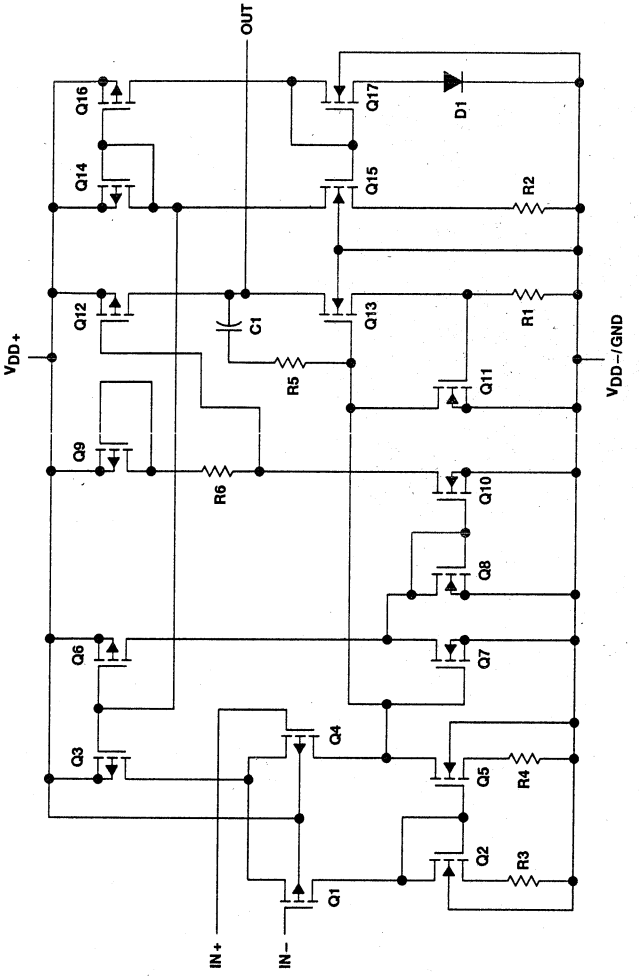
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	38
Diodes	9
Resistors	30
Capacitors	3

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) ..... −0.3 V to V_{DD}
Input current, I_I (each input) ..... ±5 mA
Output current, I_O ..... ±50 mA
Total current into V_{DD+} ..... ±50 mA
Total current out of V_{DD-} ..... ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD} (see Note 1)	2.7	8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+}-1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-1.3$	V
Operating free-air temperature, T_A	−40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2252			TLV2252A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		200	1500		200	850	μV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		2.98			2.98		V
		I_{OH} = −75 μA		25°C	2.9			2.9			
				Full range	2.8			2.8			
		I_{OH} = −150 μA		25°C	2.8			2.8			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 μA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 μA	25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 100 kΩ‡	25°C	100	250		100	250		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		800			800		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V,	R_S = 50 Ω	25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	100		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		68	125		68	125	μA
				Full range			125			125	

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS	T_A†	TLV2252			TLV2252A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, C_L = 100 pF‡ R_L = 50 kΩ‡,	25°C	0.07	0.1		0.07	0.1		V/μs
			Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		35			35		nV/√Hz
		f = 1 kHz	25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz	25°C		1.1			1.1		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡ R_L = 50 kΩ‡,	25°C		0.187			0.187		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡, A_V = 1, C_L = 100 pF‡	25°C		60			60		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		63°			63°		
	Gain margin		25°C		15			15		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2252			TLV2252A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		200	1500		200	850	μV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤5 mV,	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.98			4.98		V
		I_{OH} = −75 μA		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		I_{OH} = −150 μA		25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ‡	25°C	100	350		100	350		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		1700			1700		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		70	125		70	125	μA
				Full range			125			125	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2252			TLV2252A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2252Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω			200	1500	μV
I_{IO}	Input offset current					0.5	150	pA
I_{IB}	Input bias current					1	150	pA
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \le$5 mV,	R_S = 50 Ω		0 to 2	−0.3 to 2.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA				2.98		V
		I_{OH} = −150 μA			2.8	2.85		
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_{OL} = 50 μA			10		V
		V_{IC} = 0,	I_{OL} = 500 μA			100	125	
		V_{IC} = 0,	I_{OL} = 1 mA			200	250	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 100 kΩ†		100	225		V/mV
			R_L = 1 MΩ†			800		
r_{id}	Differential input resistance					10^{12}		Ω
r_{ic}	Common-mode input resistance					10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 0,	R_S = 50 Ω	65	77		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V,	V_{IC} = 0,	No load	80	100		dB
I_{DD}	Supply current	V_O = 0,	No load			68	125	μA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2252Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω		200	1500	μV
I_{IO}	Input offset current				0.5	150	pA
I_{IB}	Input bias current				1	150	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω	0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA			4.98		V
		I_{OH} = −75 μA		4.9	4.94		
		I_{OH} = −150 μA		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA		0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA		0.2	0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ†	100	350		V/mV
			R_L = 1 MΩ†		1700		
r_{id}	Differential input resistance				10^{12}		Ω
r_{ic}	Common-mode input resistance				10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10		200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V,	V_O = 2.5 V, R_S = 50 Ω	70	83		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, No load	V_{IC} = V_{DD}/2,	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		70	125	μA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode voltage	2, 3 4, 5
α_{VIO}	Input offset voltage temperature coefficient	Distribution	6, 7
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	8
V_I	Input voltage	vs Supply voltage vs Free-air temperature	9 10
V_{OH}	High-level output voltage	vs High-level output current	11, 14
V_{OL}	Low-level output voltage	vs Low-level output current	12, 13, 15
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	16
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	17 18
V_{ID}	Differential input voltage	vs Output voltage	19, 20
A_{VD}	Differential voltage amplification	vs Load resistance vs Frequency vs Free-air temperature	21 22, 23 24, 25
z_o	Output impedance	vs Frequency	26, 27
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	28 29
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	30, 31 32
I_{DD}	Supply current	vs Supply voltage	33
SR	Slew rate	vs Load capacitance vs Free-air temperature	34 35
V_O	Large-signal pulse response	vs Time	36, 37, 38, 39
V_O	Small-signal pulse response	vs Time	40, 41, 42, 43,
V_n	Equivalent input noise voltage	vs Frequency	44, 45
	Noise voltage (referred to input)	Over a 10-second period	46
	Integrated noise voltage	vs Frequency	47
THD + N	Total harmonic distortion plus noise	vs Frequency	48
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	49 50
ϕ_m	Phase margin	vs Frequency vs Load capacitance	22, 23 51
	Gain margin	vs Load capacitance	52
B_1	Unity-gain bandwidth	vs Load capacitance	53
	Overestimation of phase margin	vs Load capacitance	54

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2252
INPUT OFFSET VOLTAGE

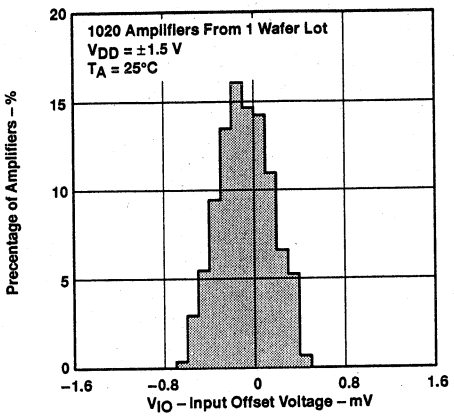


Figure 2

DISTRIBUTION OF TLV2252
INPUT OFFSET VOLTAGE

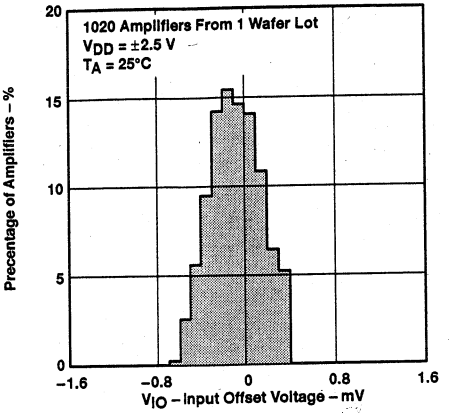


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

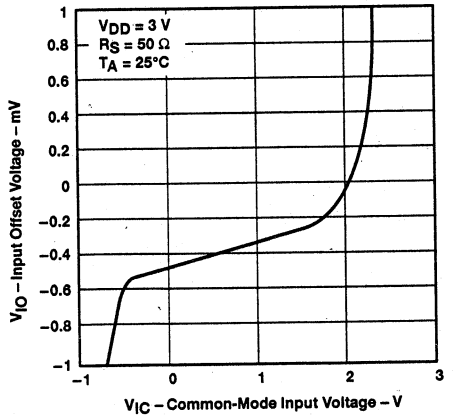


Figure 4

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

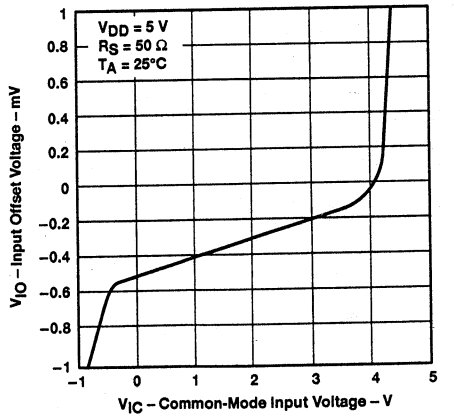


Figure 5

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2252 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

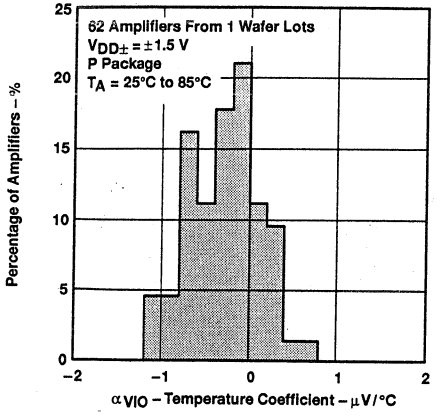


Figure 6

DISTRIBUTION OF TLV2252 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

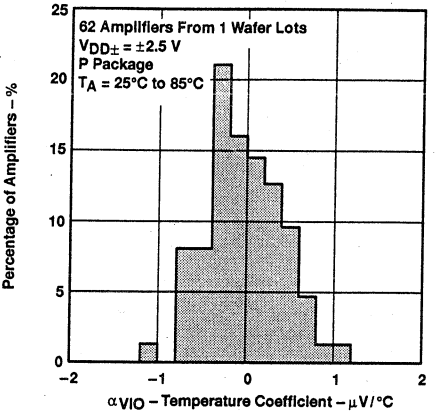


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

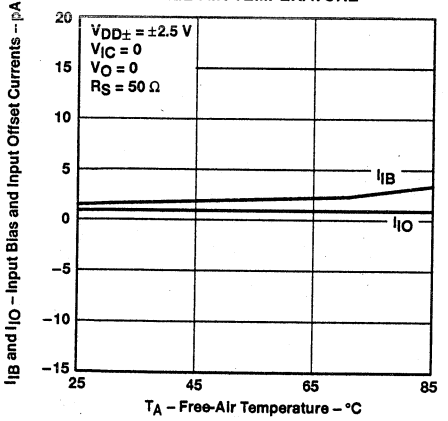


Figure 8

INPUT VOLTAGE vs SUPPLY VOLTAGE

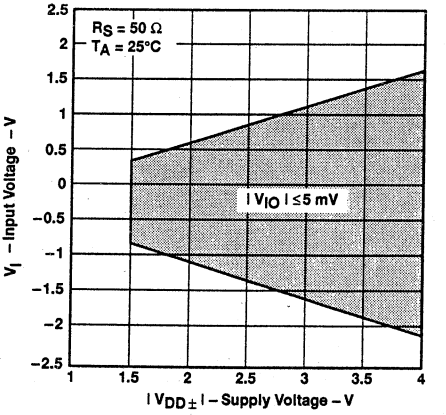


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†‡

INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

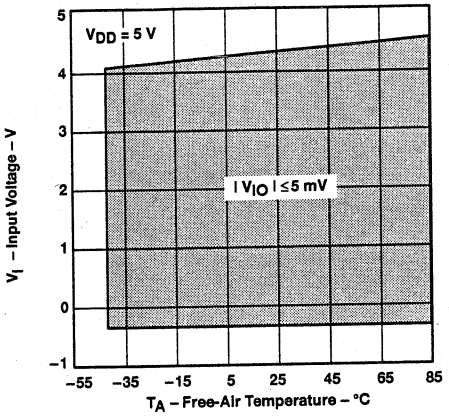


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

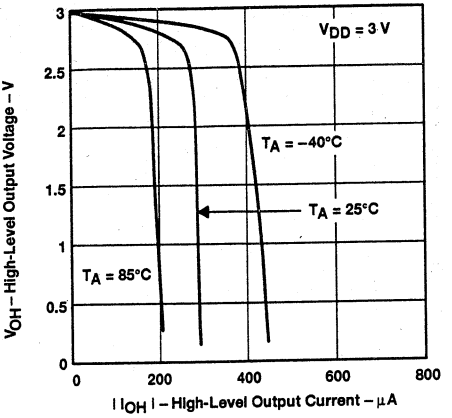


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

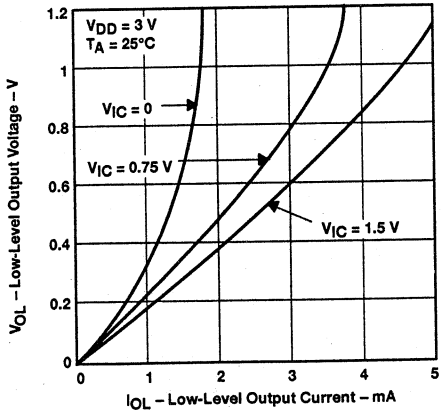


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

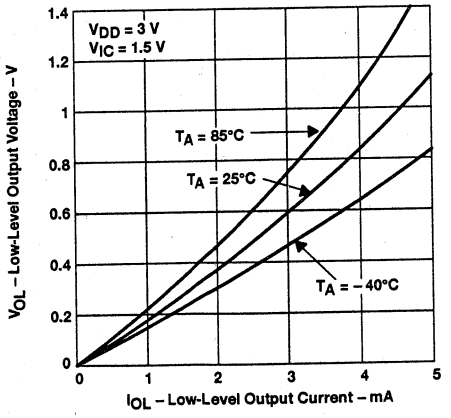


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

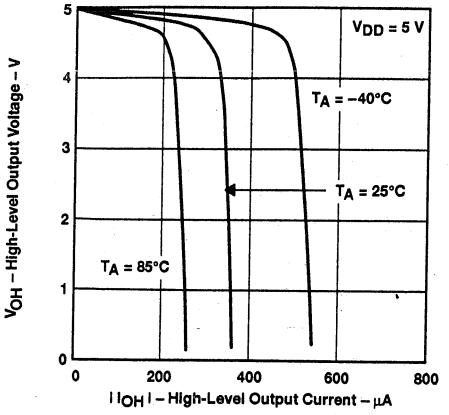


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

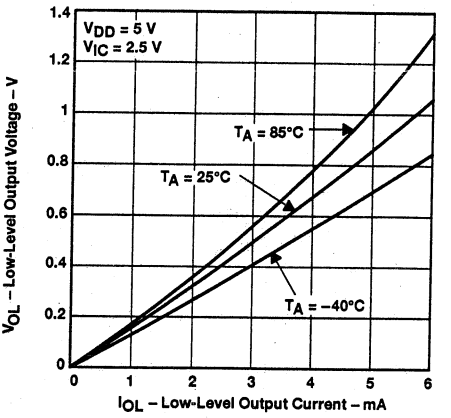


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

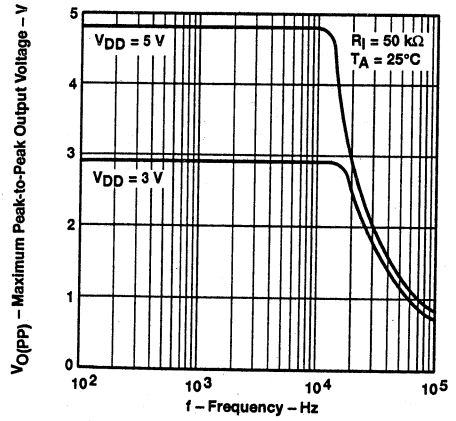


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

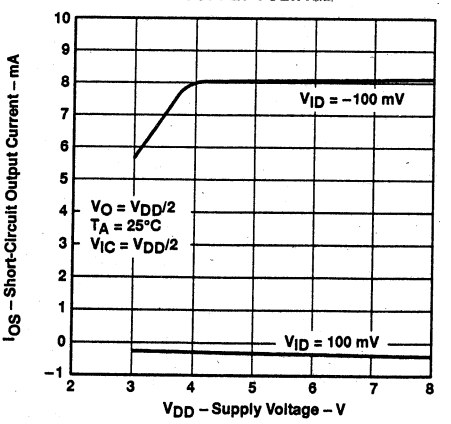


Figure 17

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

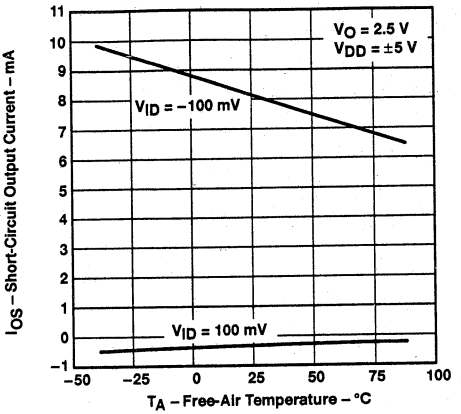


Figure 18

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

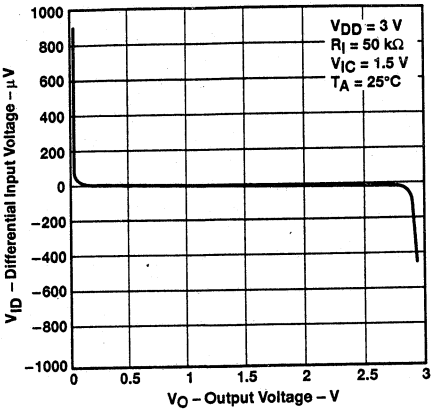


Figure 19

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

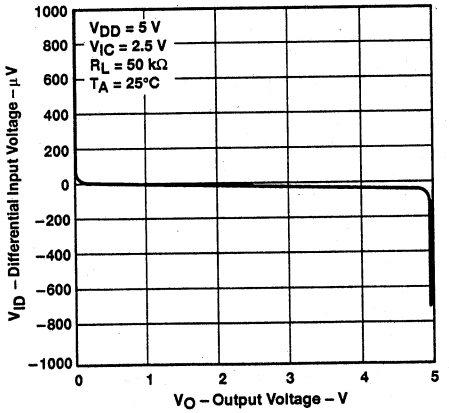


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

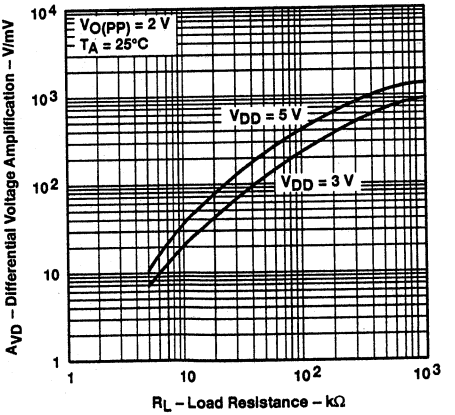


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

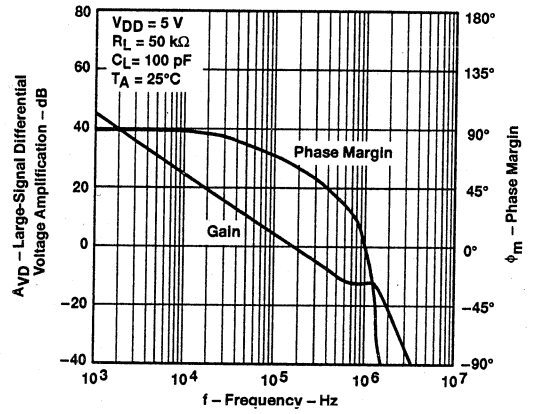


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

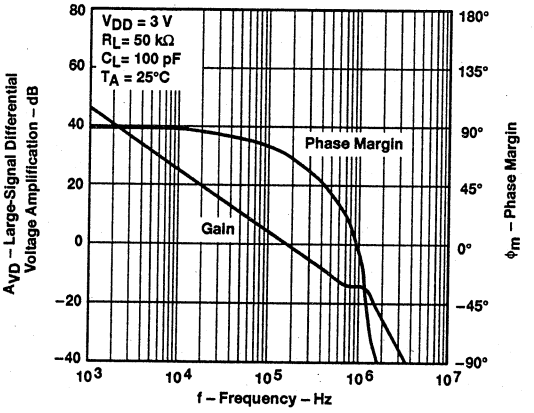


Figure 23

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

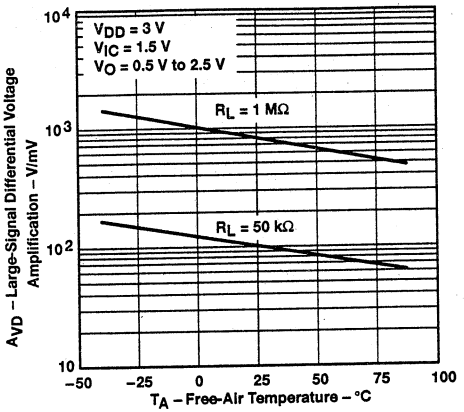


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

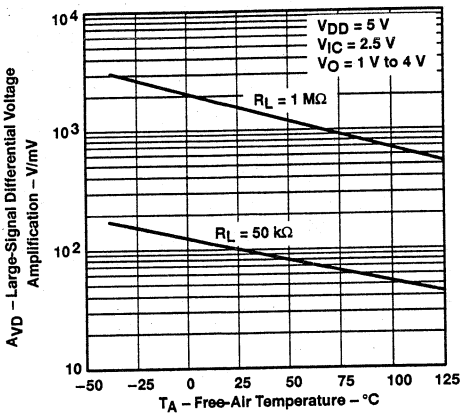


Figure 25

OUTPUT IMPEDANCE vs FREQUENCY

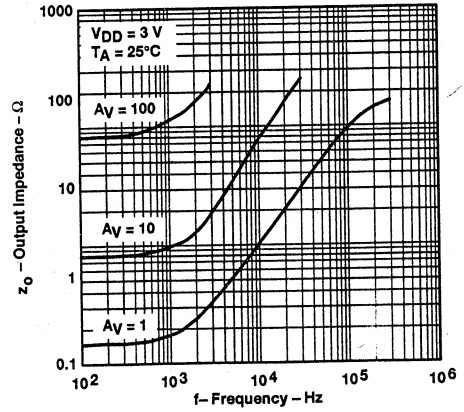


Figure 26

OUTPUT IMPEDANCE vs FREQUENCY

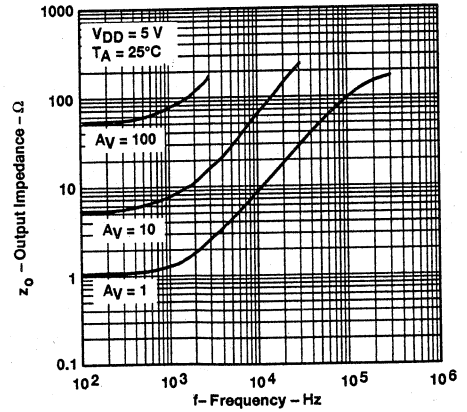


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

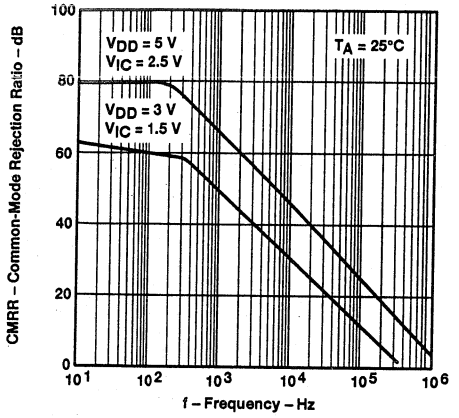


Figure 28

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

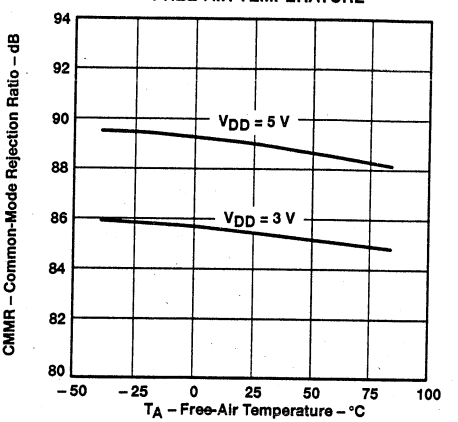


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

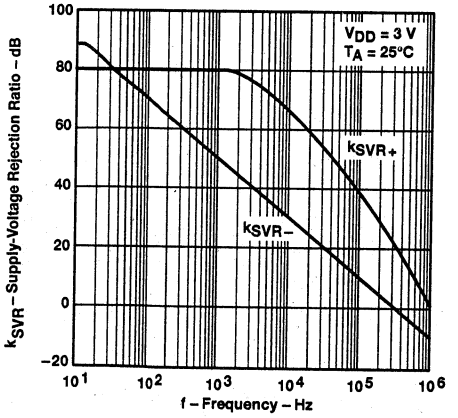


Figure 30

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

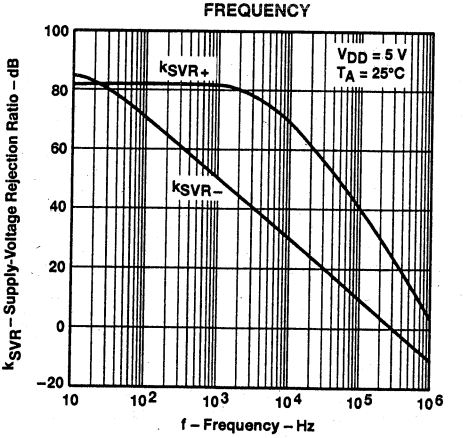


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

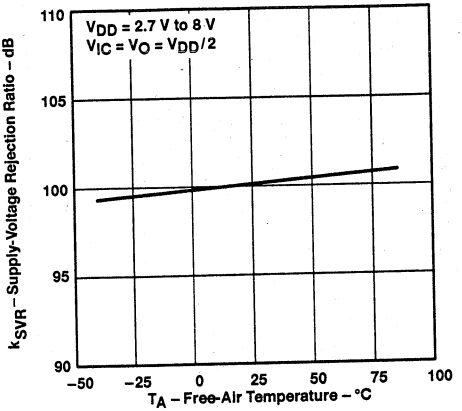


Figure 32

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

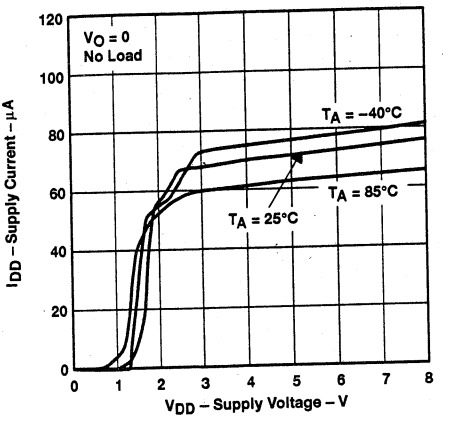


Figure 33

SLEW RATE
vs
LOAD CAPACITANCE

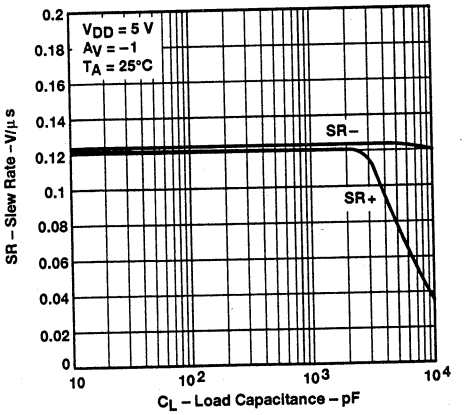


Figure 34

SLEW RATE
vs
FREE-AIR TEMPERATURE

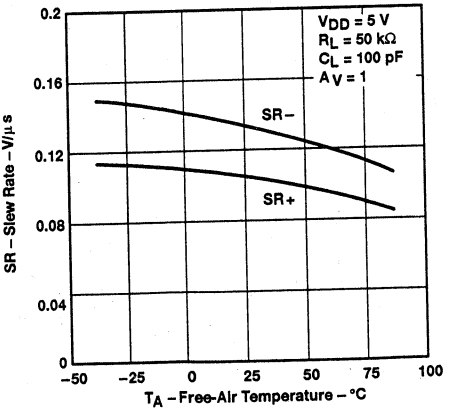


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

INVERTING LARGE-SIGNAL PULSE RESPONSE

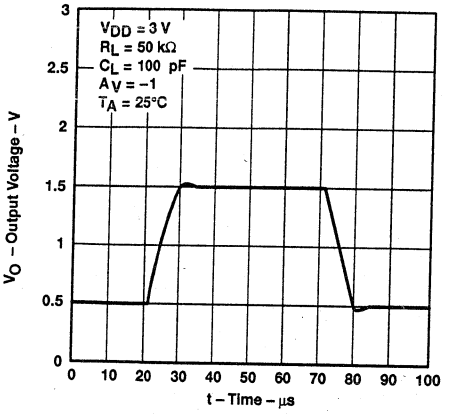


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE

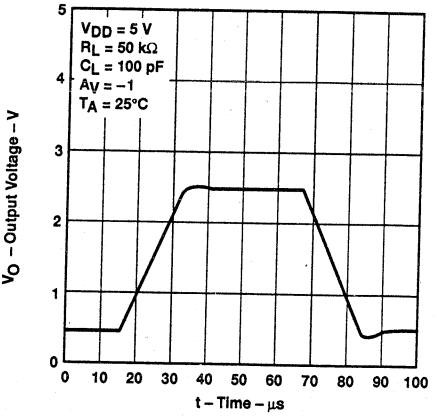


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

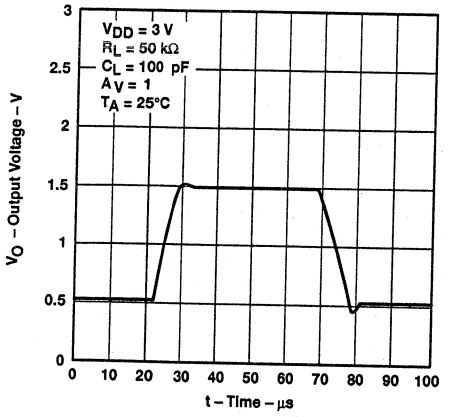


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

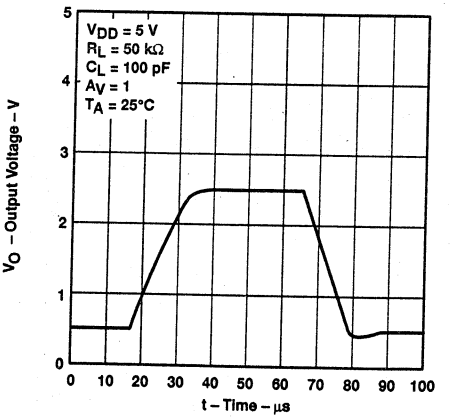


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

INVERTING SMALL-SIGNAL
PULSE RESPONSE

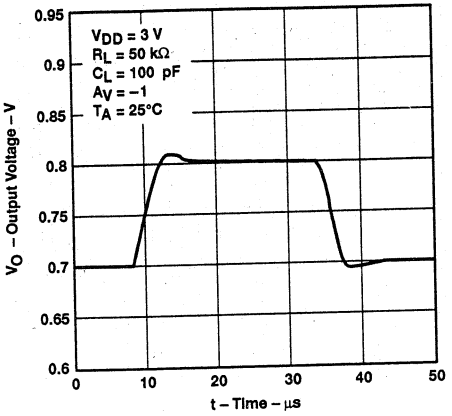


Figure 40

INVERTING SMALL-SIGNAL
PULSE RESPONSE

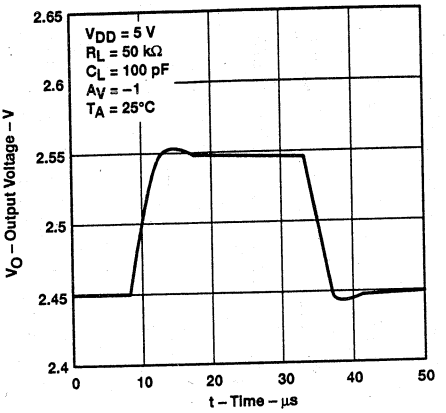


Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

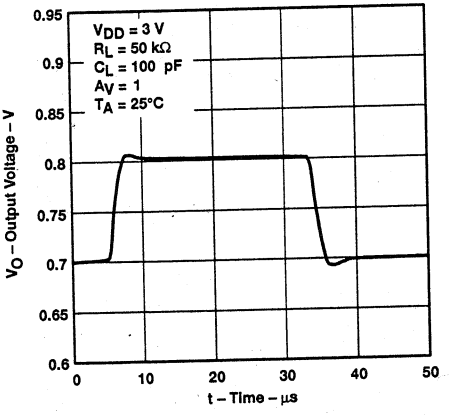


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

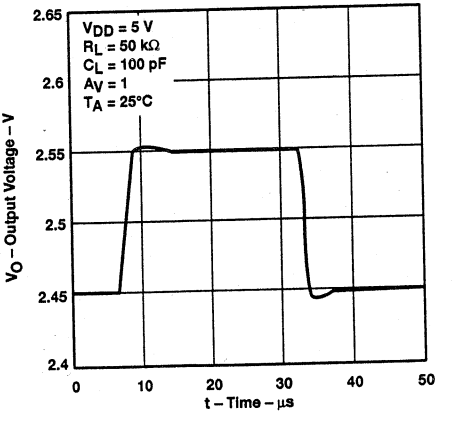


Figure 43

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

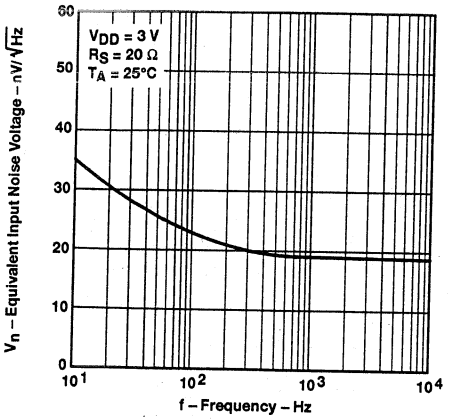


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

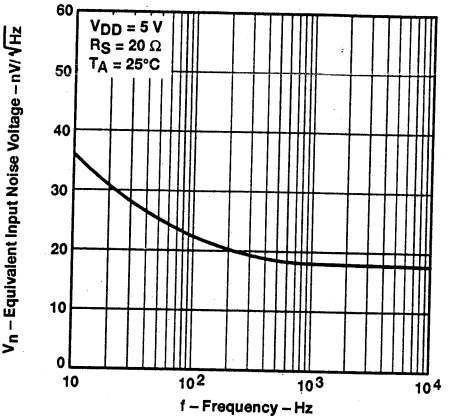


Figure 45

INPUT NOISE VOLTAGE OVER
A 10-SECOND PERIOD

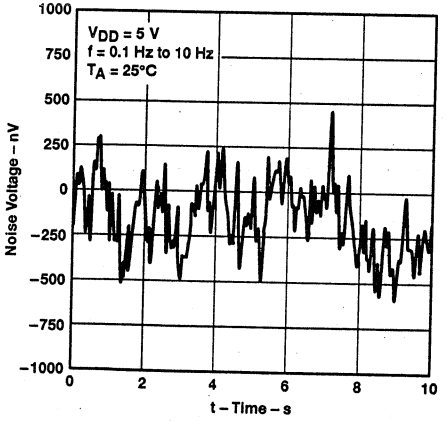


Figure 46

INTEGRATED NOISE VOLTAGE
vs
FREQUENCY

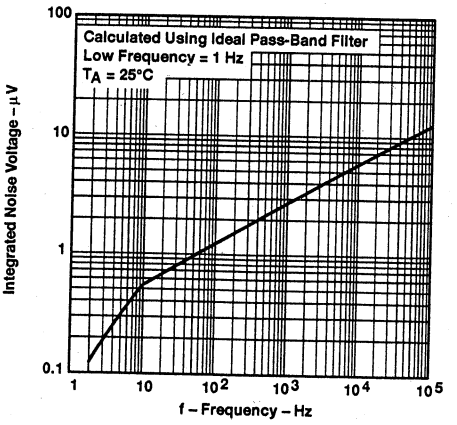


Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

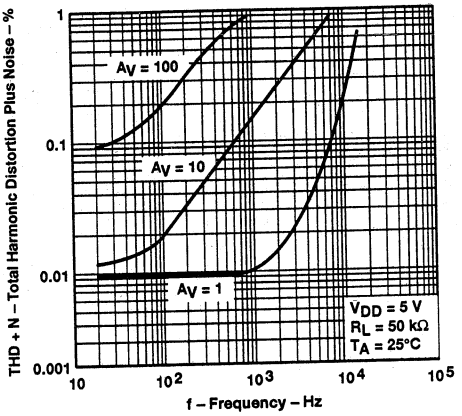


Figure 48

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

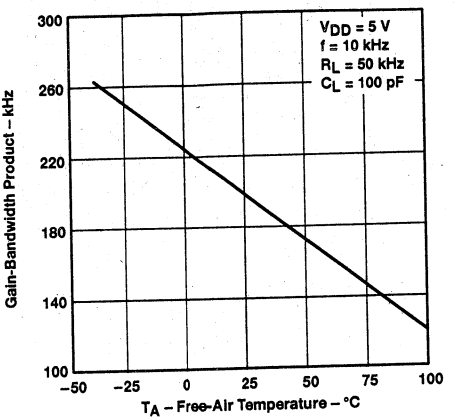


Figure 49

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

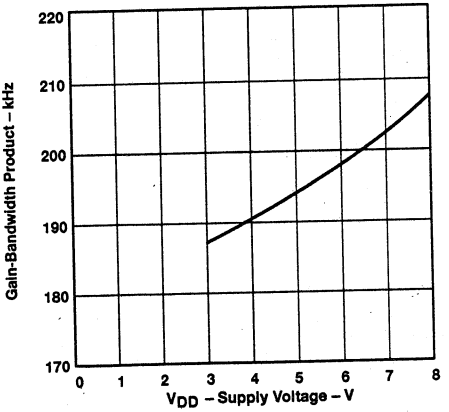


Figure 50

PHASE MARGIN
vs
LOAD CAPACITANCE

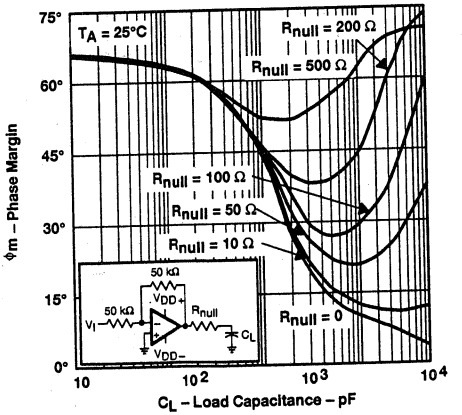


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN MARGIN
vs
LOAD CAPACITANCE

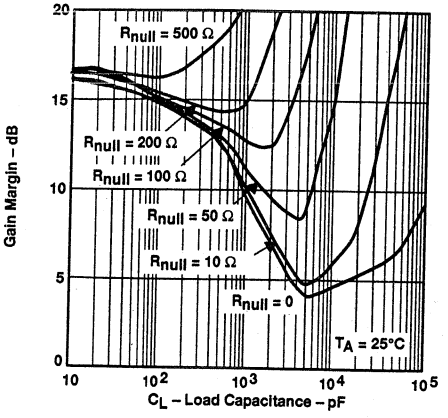


Figure 52

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

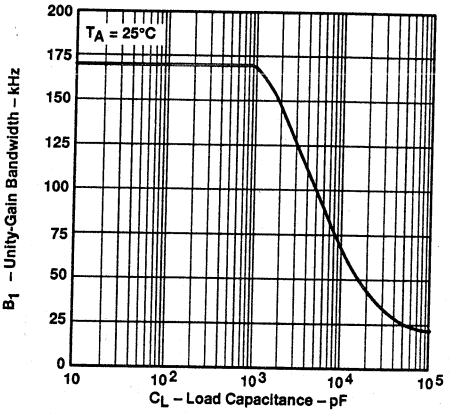
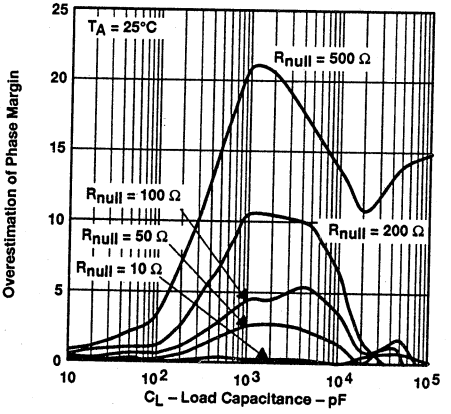


Figure 53

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE



† See application information

Figure 54

TEXAS INSTRUMENTS

APPLICATION INFORMATION

driving large capacitive loads

The TLV2252 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω, 50 Ω, 100 Ω, 200 Ω, and 500 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L\right) \quad (1)$$

where :

$\Delta\phi_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation (1), UGBW must be approximated from Figure 53.

Using equation (1) alone overestimates the improvement in phase margin as illustrated in Figure 54. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 55, with equation (1) enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

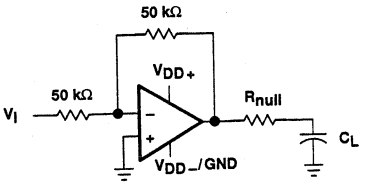


Figure 55. Series-Resistance Circuit

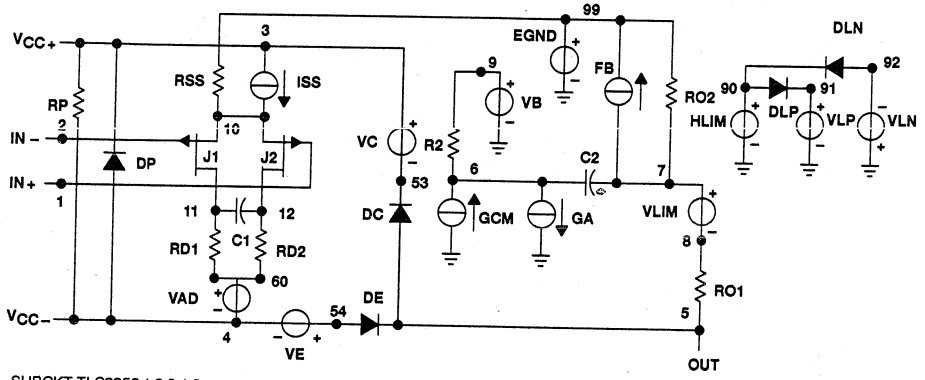
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 56 are generated using the TLV2252 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLC2252 1 2 3 4 5
C1      11    12    6.369E-12
C2      6     7     25.00E-12
DC      5     53    DX
DE      54    5     DX
DLP     90    91    DX
DLN     92    90    DX
DP      4     3     DX
EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
FB      7     99    POLY (5) VB VC VE VLP
+ VLN 0 57.62E6 –60E6 60E6 60E6 –60E6
GA      6     0     11    12 26.86E–6
GCM     0     6     10    99 2.686E–9
ISS     3     10    DC 3.1E–6
HLIM    90    0     VLIM 1K
J1      11    2     10 JX
J2      12    1     10 JX
R2      6     9     100.0E3
RD1     60    11    37.23E3
RD2     60    12    37.23E3
RO1     8     5     84
RO2     7     99    84
RP      3     4     71.43E3
RSS     10    99    64.52E6
VAD     60    4     –.5
VB      9     0     DC 0
VC      3     53    DC .605
VE      54    4     DC .605
VLIM    7     8     DC 0
VLP     91    0     DC –0.235
VLN     0     92    DC 7.5
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=139E–6
+ VTO=–.05)
.ENDS
```

Figure 56. Boyle Macromodel and Subcircuit

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TEXAS INSTRUMENTS

available features

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 500 μA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C**
- **Wide Supply Voltage Range 2.7 V to 8 V**
- **Macromodel Included**

description

The TLV2262 and TLV2262A are dual operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices are optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with μ-power dissipation levels, the input noise voltage performance has been dramatically improved using optimized design techniques for CMOS-type amplifiers. Another added benefit is that these amplifiers exhibit rail-to-rail output swing. Figure 1 graphically depicts the high-level output voltage for different levels of output current for a 3-V single supply. As can be seen, the output dynamic range can be extended using the TLV2262 with loads referenced midway between the rails. Also, the common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ± 5 mV, allowing a minimum of 0 to 2-V common-mode input voltage range for a 3-V supply. Furthermore, at 200 μA (typical) of supply current per amplifier, the TLV2262 family can achieve input offset voltage levels as low as 950 μV, outperforming existing CMOS amplifiers. The Advanced LinCMOS process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

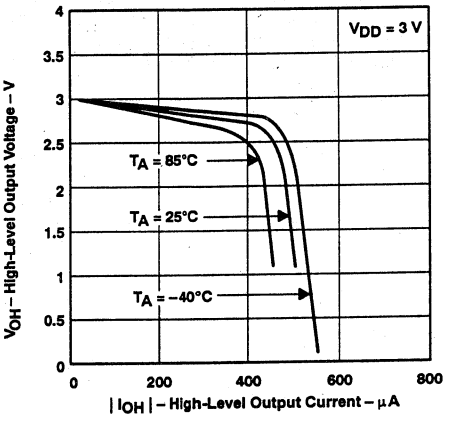

Figure 1

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES				CHIP FORM (Y)
	V_{IO} max AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
−40°C to 85°C	950 μV	TLV2262AID	TLV2262AIP	TLV2262AIPWLE	TLV2262Y
	2.5 mV	TLV2262ID	TLV2262IP	—	

The D packages are available taped and reeled. Add R suffix to device type, (e.g., TLV2262IDR).
The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

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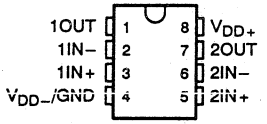
TEXAS INSTRUMENTS

description (continued)

The TLV2262 and TLV2262A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to ADCs. All of these features combined with its temperature performance make the TLV2262 family ideal for remote pressure sensors, temperature control, active VR sensors, accelerometers, hand-held metering, and many other applications.

The device inputs and outputs are designed to withstand 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, exercise care in handling these devices, as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD protection structure, inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

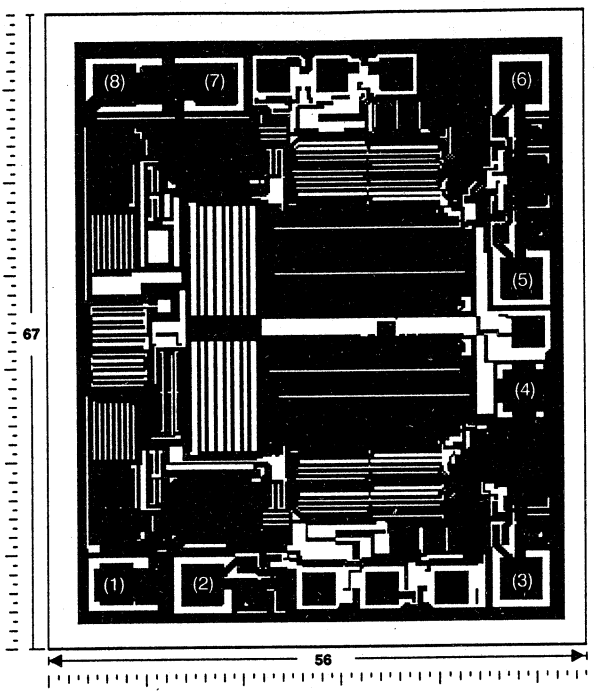
D, P, OR PW PACKAGE
(TOP VIEW)

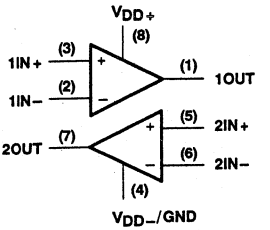


chip information

This chip, when properly assembled, displays characteristics similar to the TLV2262. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

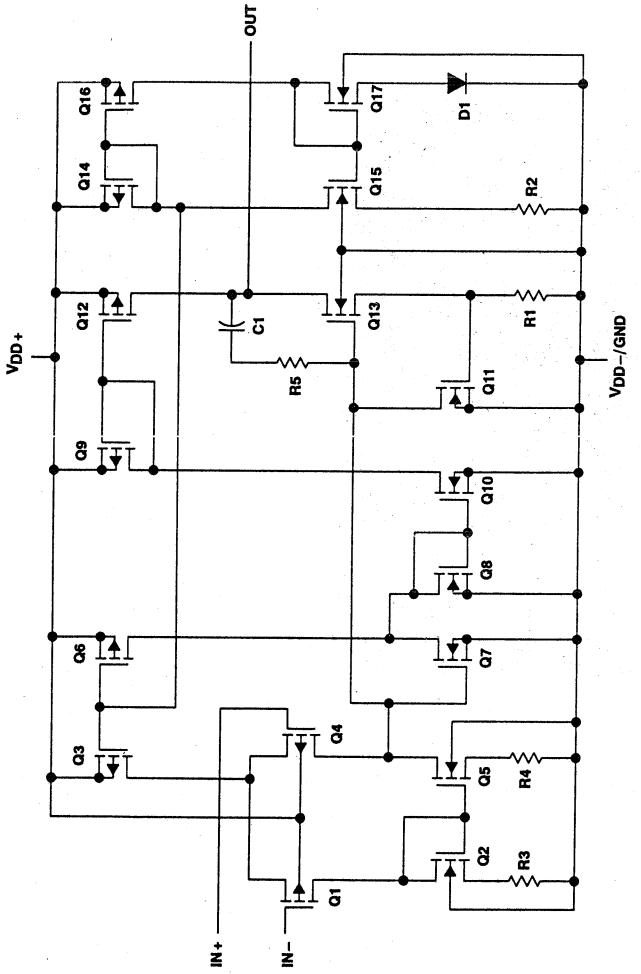
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	38
Diodes	9
Resistors	26
Capacitors	3

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD\pm}$ (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $V_{DD\pm}$
Input voltage range, V_I (any input, see Note 1) ..... −0.3 V to V_{DD}
Input current, I_I (each input) ..... ±5 mA
Output current, I_O ..... ±50 mA
Total current into V_{DD+} terminal ..... ±50 mA
Total current out of V_{DD-} terminal ..... ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$ (see Note 1)	2.7	8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	−40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			100			100	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	|V_{IO}| ≤5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		2.99			2.99		V
		I_{OH} = −100 μA		25°C	2.85			2.85			
				Full range	2.825			2.825			
		I_{OH} = −200 μA		25°C	2.7			2.7			
				Full range	2.65			2.65			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 μA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 μA	25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	30			30			
			R_L = 1 MΩ‡	25°C		100			100		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V,	R_S = 50 Ω	25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, No load,	V_{IC} = V_{DD}/2	25°C	80	95		80	100		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		400	500		400	500	μA
				Full range			500			500	

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.8			0.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		160			160		kHz
	Settling time	A_V = −1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		μs
			To 0.01%			12.5			12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		48°			48°		
	Gain margin			25°C		10			10		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			100			100	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			100			100	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤5 mV	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −200 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.6			4.6			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		80	170		V/mV
				Full range	55			55			
			R_L = 1 MΩ‡	25°C		150			550		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 4.4 V to 8 V, No load,	V_{IC} = V_{DD}/2	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		400	500		400	500	μA
				Full range			500			500	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.82			0.82		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		205			205		kHz
	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		49°			49°		
	Gain margin			25°C		11			11		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,			300	2500	μV
I_{IO}	Input offset current					0.5	100	pA
I_{IB}	Input bias current					1	100	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \leq 5$ mV,	R_S = 50 Ω		0 to 2	−0.3 to 2.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA				2.99		V
		I_{OH} = −200 μA			2.7	2.75		
V_{OL}	Low-level output voltage	V_{IC} = 0 V,	I_{OL} = 50 μA			10		V
		V_{IC} = 0 V,	I_{OL} = 500 μA			100	125	
		V_{IC} = 0 V,	I_{OL} = 1 mA			200	250	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 50 kΩ†		60	100		V/mV
			R_L = 1 MΩ†			100		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 0,	R_S = 50 Ω	65	77		dB
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 2.7 V to 8 V,	No load,	V_{IC} = 0	80	100		dB
I_{DD}	Supply current	V_O = 0,	No load			400	500	μA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω			300	2500	μV
I_{IO}	Input offset current					0.5	100	pA
I_{IB}	Input bias current					1	100	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω		0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA				4.99		V
		I_{OH} = −100 μA			4.85	4.94		
		I_{OH} = −200 μA			4.7	4.85		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA			0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA			0.2	0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ†		80	170		V/mV
			R_L = 1 MΩ†			550		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V,	V_O = 2.5 V,	R_S = 50 Ω	70	83		dB
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 8 V,	No load,	V_{IC} = V_{DD}/2	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load			400	500	μA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

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$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	16
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A_{VD}	Differential voltage amplification	vs Load resistance	21
		vs Frequency	22, 23
		vs Free-air Temperature	24, 25
z_o	Output impedance	vs Frequency	26, 27
CMRR	Common-mode rejection ratio	vs Frequency	28
		vs Free-air Temperature	29
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	30, 31
		vs Free-air Temperature	32, 33
I_{DD}	Supply current	vs Free-air Temperature	34
SR	Slew rate	vs Load capacitance	35
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V_O	Large-signal pulse response	vs Time	37, 38, 39, 40
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V_n	Equivalent input noise voltage	vs Frequency	45, 46
	Noise voltage (referred to input)	Over a 10-second period	47
	Integrated noise voltage	vs Frequency	48
THD + N	Total harmonic distortion plus noise	vs Frequency	49
	Gain-bandwidth product	vs Free-air Temperature	50
		vs Supply voltage	51
ϕ_m	Phase margin	vs Frequency	22, 23
		vs Load capacitance	52
	Gain margin	vs Load capacitance	53

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

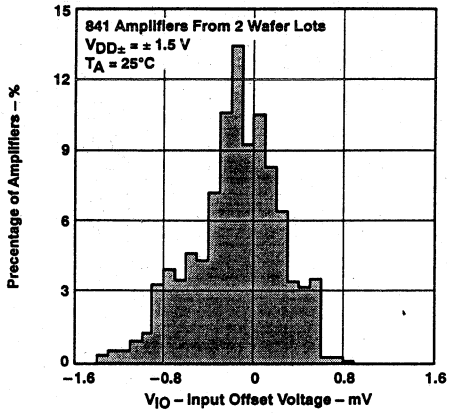


Figure 2

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

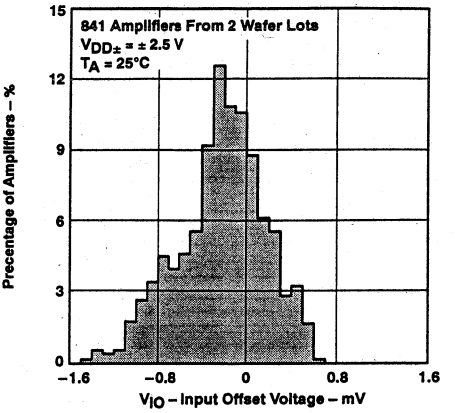


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

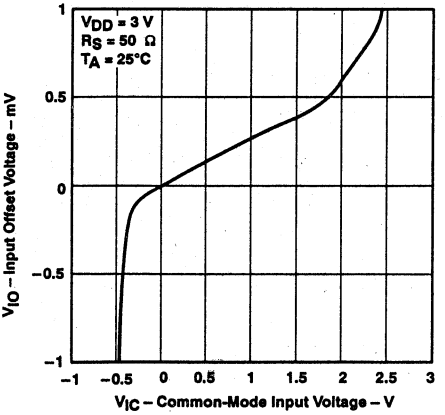


Figure 4

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

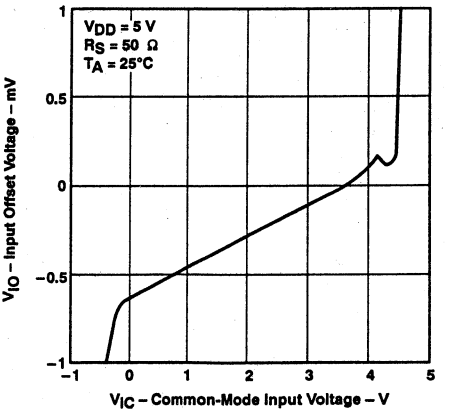


Figure 5

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

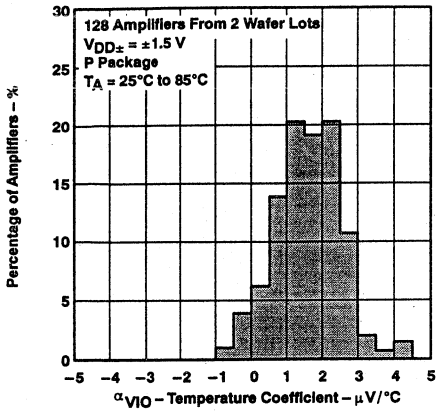


Figure 6

DISTRIBUTION OF TLV2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

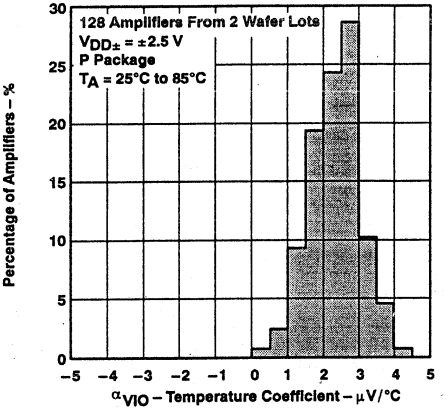


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

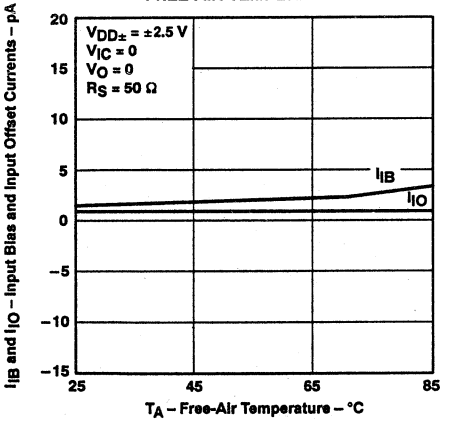


Figure 8

INPUT VOLTAGE vs SUPPLY VOLTAGE

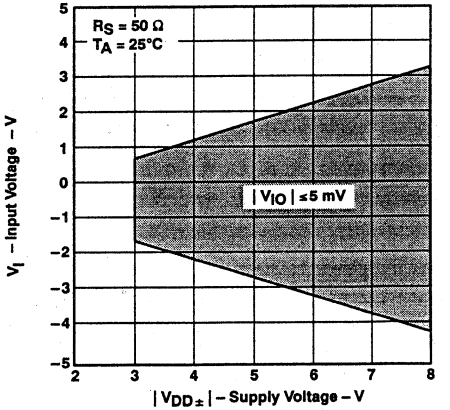


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†‡

INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

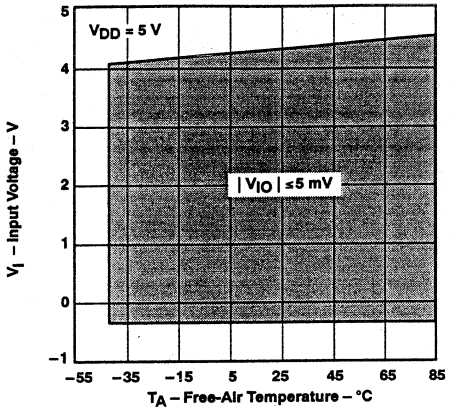


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

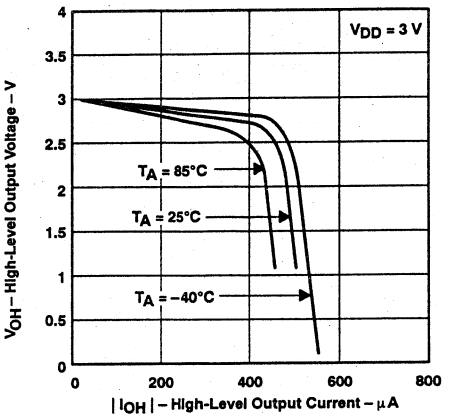


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

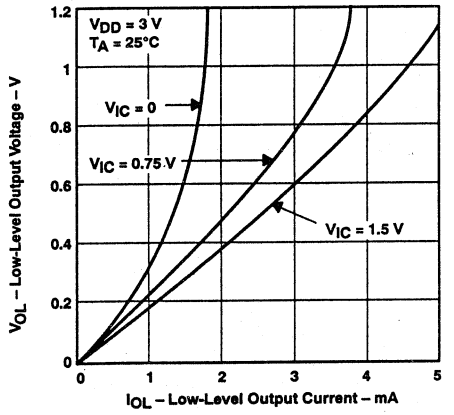


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

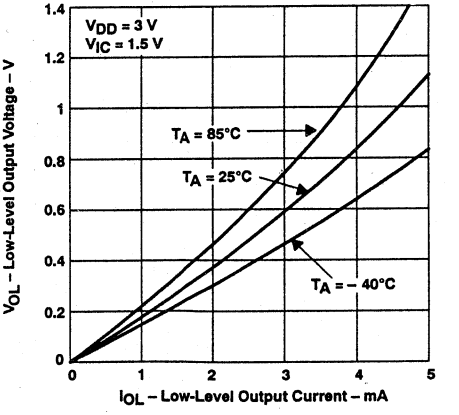


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

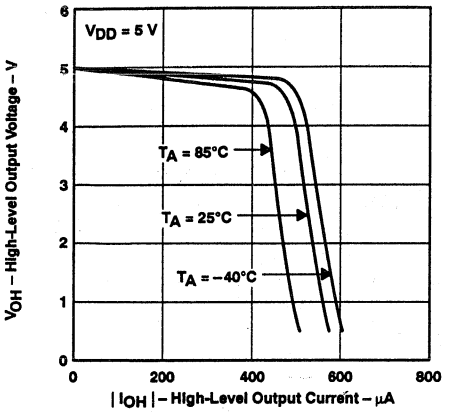


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

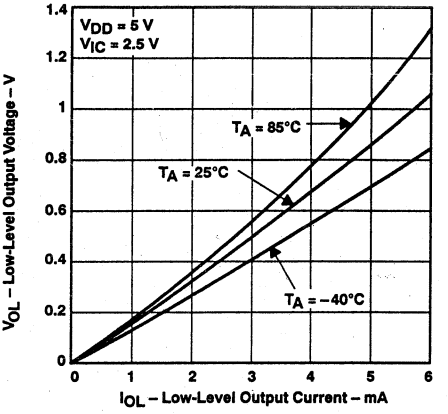


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

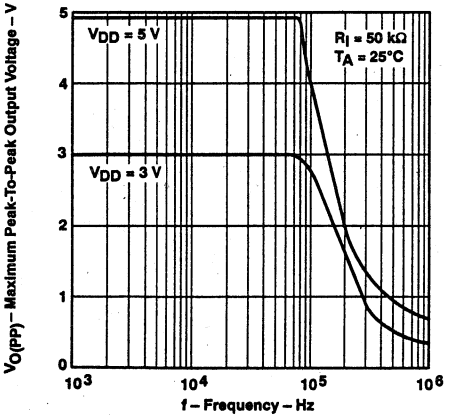


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

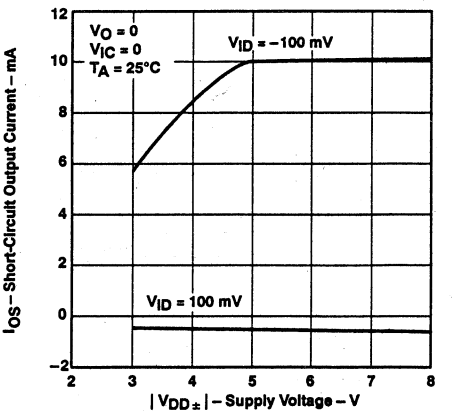


Figure 17

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

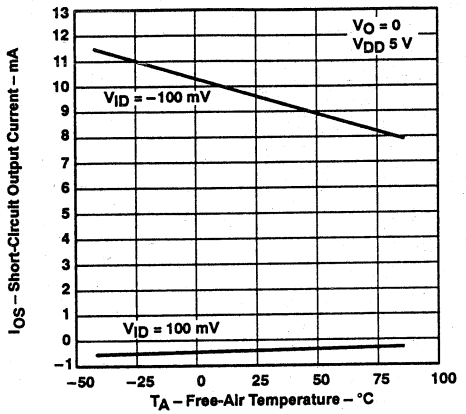


Figure 18

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

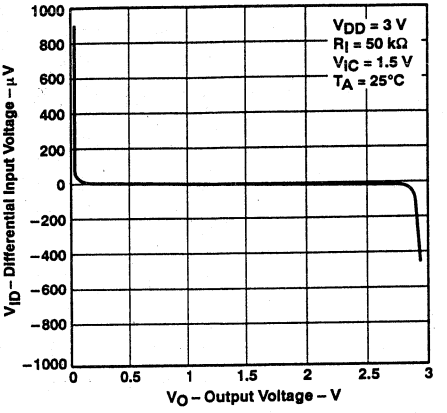


Figure 19

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

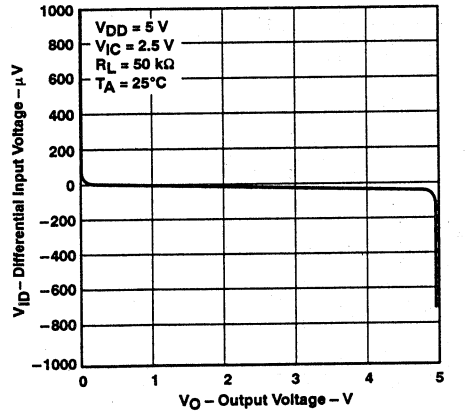


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

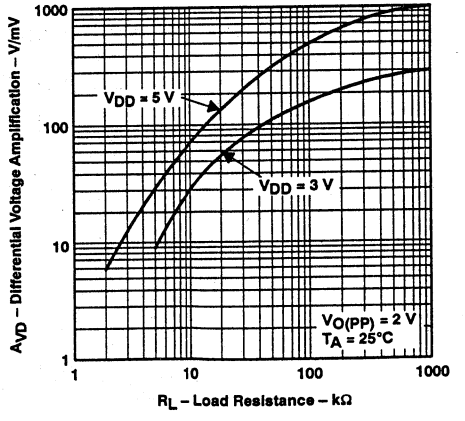


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS‡

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

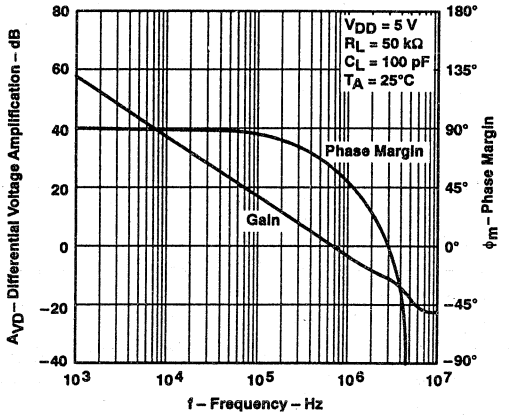


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

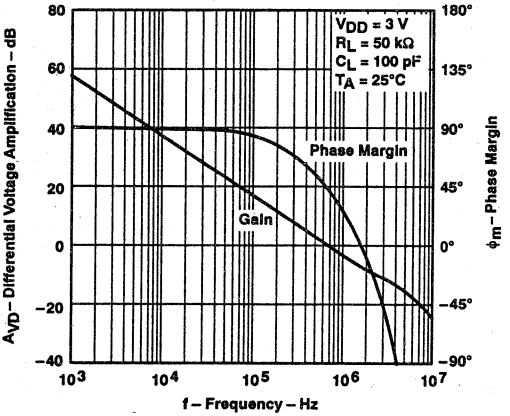


Figure 23

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

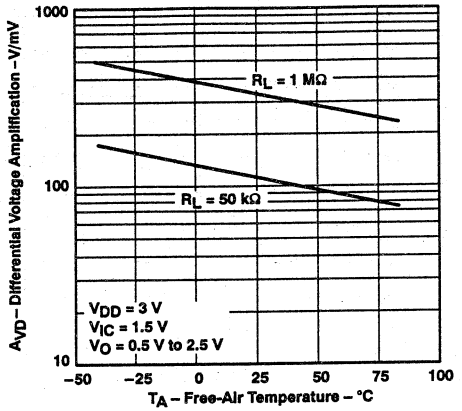


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

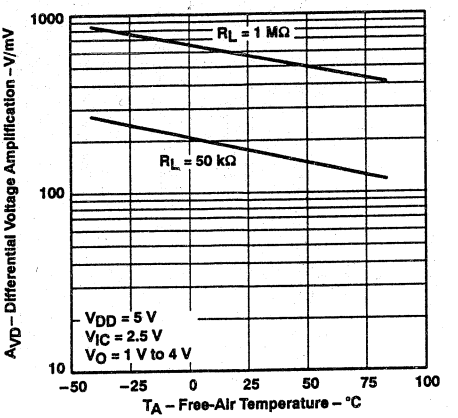


Figure 25

OUTPUT IMPEDANCE vs FREQUENCY

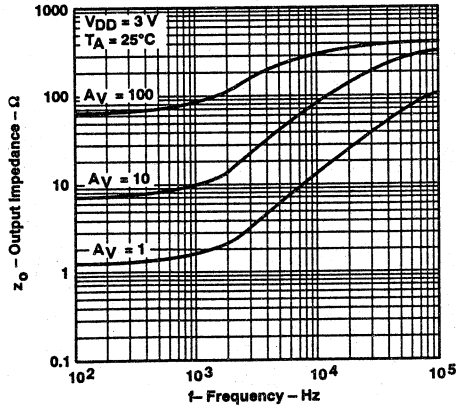


Figure 26

OUTPUT IMPEDANCE vs FREQUENCY

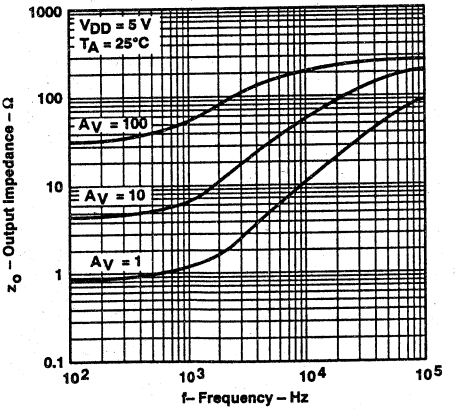


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

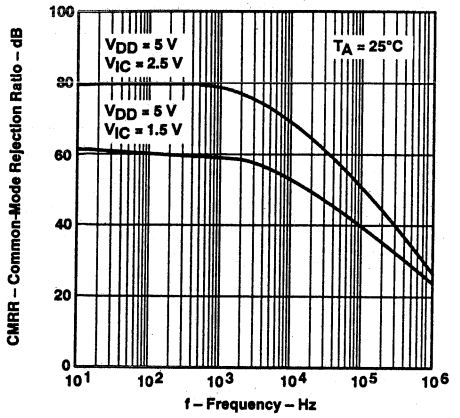


Figure 28

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

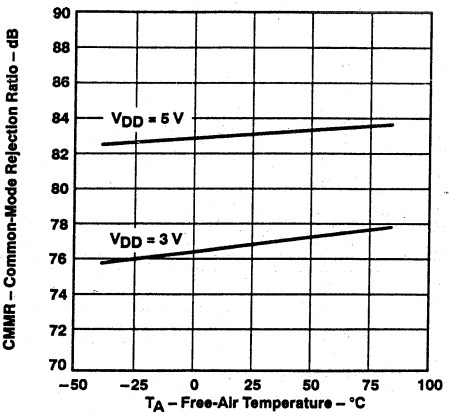


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

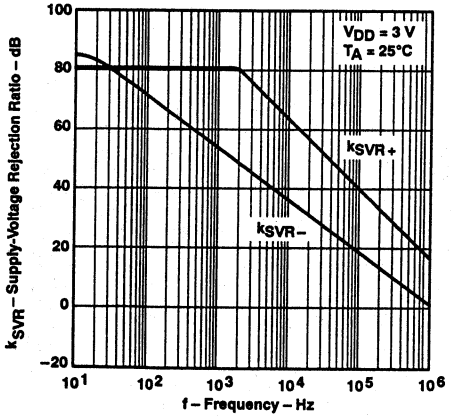


Figure 30

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

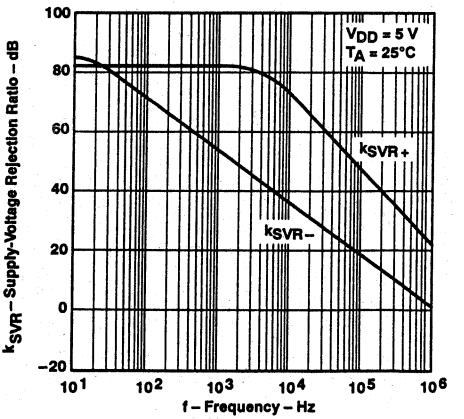


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

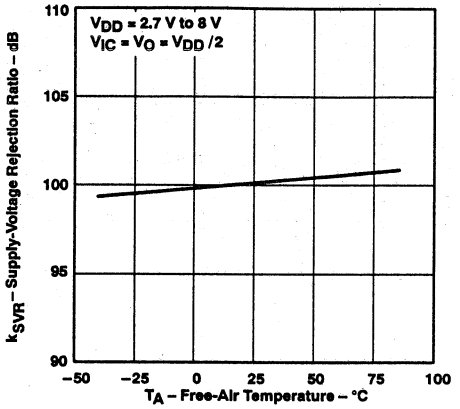


Figure 32

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

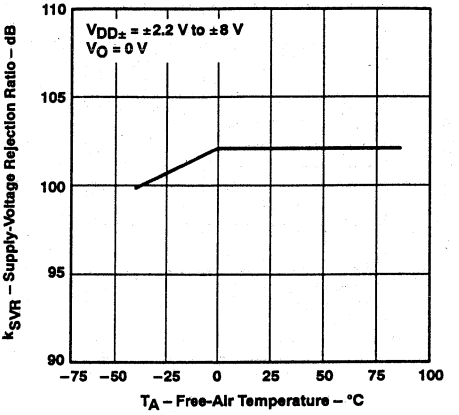


Figure 33

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

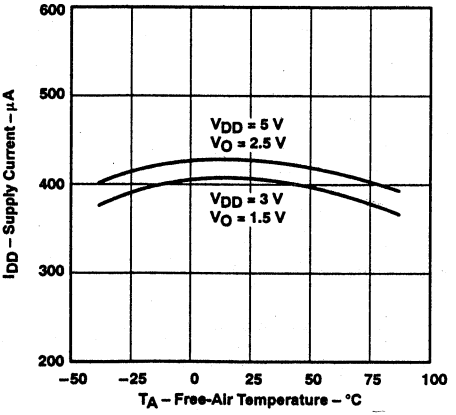


Figure 34

SLEW RATE
vs
LOAD CAPACITANCE

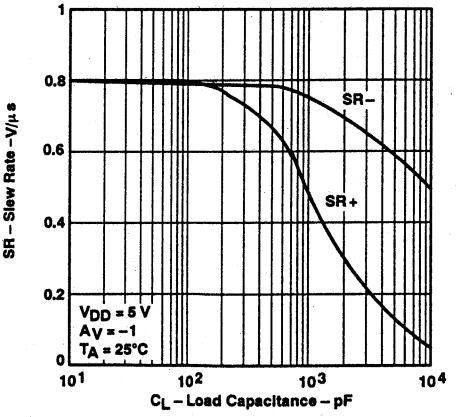


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SLEW RATE
vs
FREE-AIR TEMPERATURE

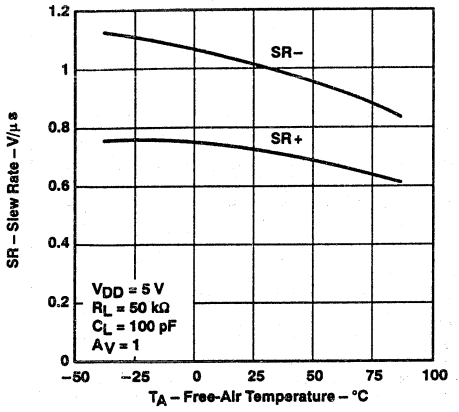


Figure 36

INVERTING LARGE-SIGNAL PULSE
RESPONSE

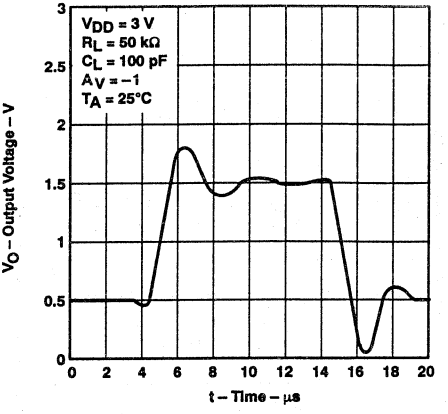


Figure 37

INVERTING LARGE-SIGNAL PULSE
RESPONSE

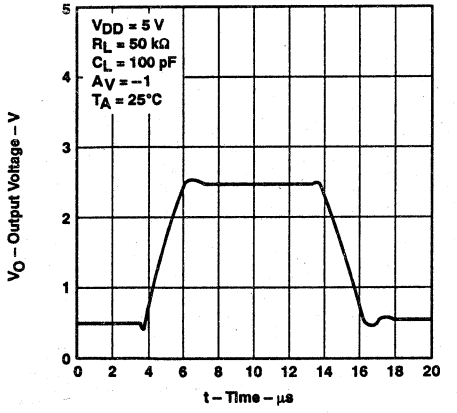


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE

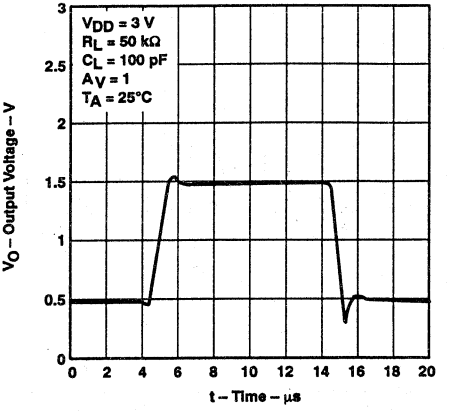


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

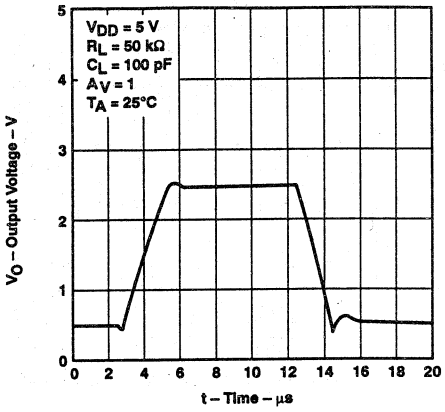


Figure 40

INVERTING SMALL-SIGNAL PULSE RESPONSE

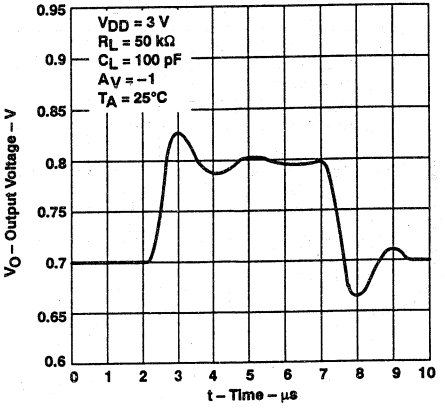


Figure 41

INVERTING SMALL-SIGNAL PULSE RESPONSE

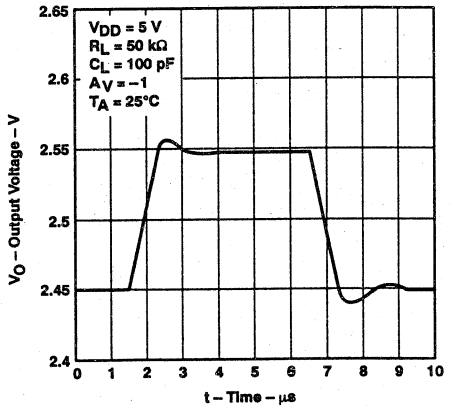


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

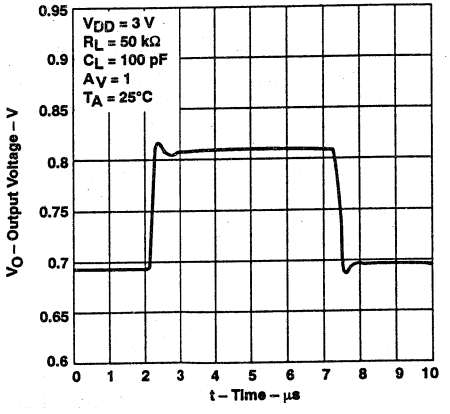


Figure 43

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

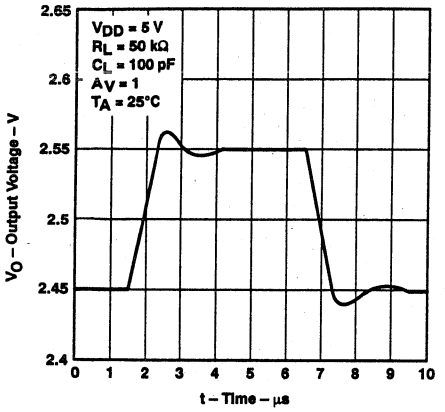


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

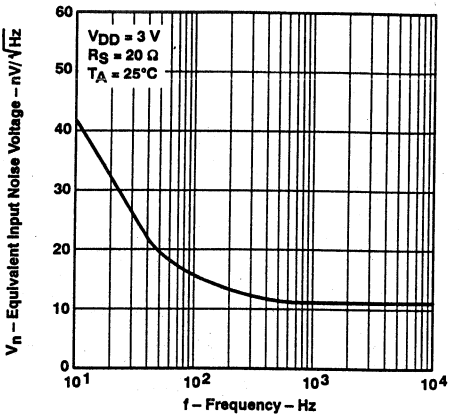


Figure 45

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

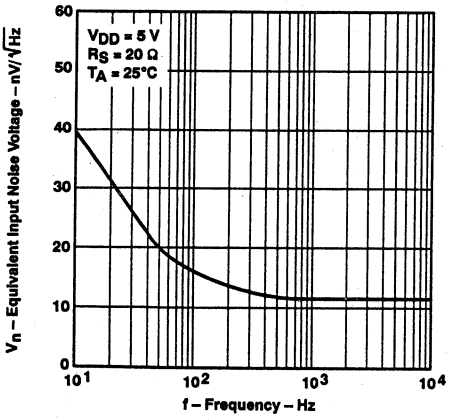


Figure 46

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

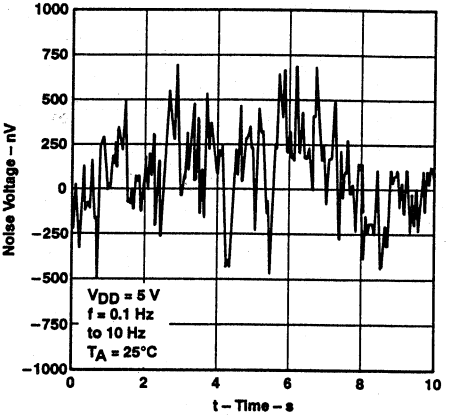


Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

INTEGRATED NOISE VOLTAGE
vs
FREQUENCY

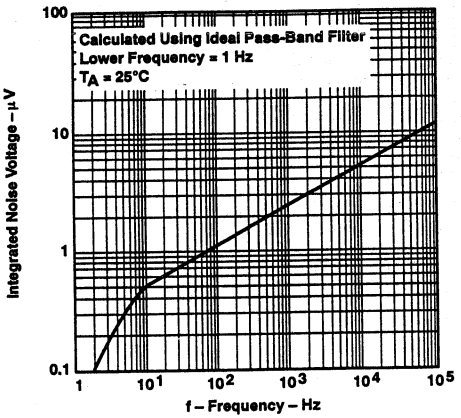


Figure 48

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

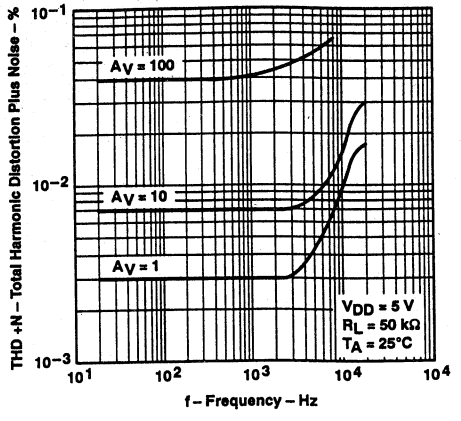


Figure 49

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

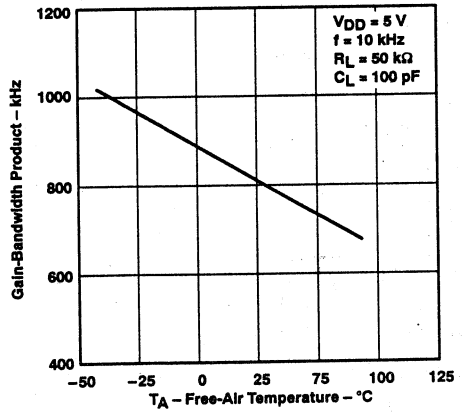


Figure 50

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

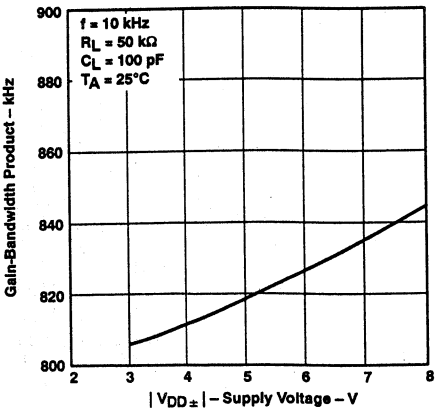


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
LOAD CAPACITANCE

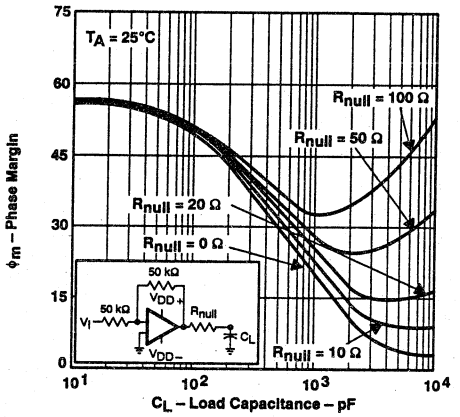


Figure 52

GAIN MARGIN
vs
LOAD CAPACITANCE

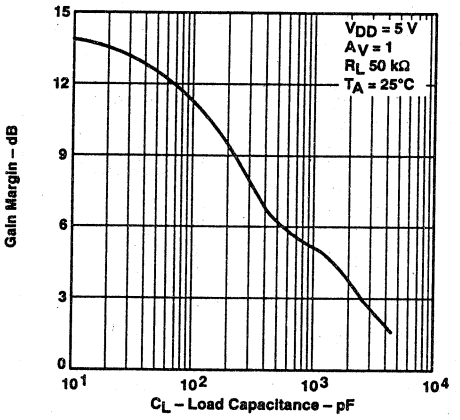


Figure 53

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

APPLICATION INFORMATION

loading considerations

The TLV2262 is a lower-power version of the TLC2272 with the appropriate design changes relative to the lower power level. The output drive performance to the negative rail for the TLV2262 is similar to the TLC2272 and is capable of driving several milliamperes.

The design topology used for the TLV2262 or the TLC2272 limits the drive to the positive rail to a value very close to the I_{DD} for the amplifier. Thus, while the TLC2272 is capable of greater than 1-mA drive from the positive rail, the TLV2262 is capable of only a few 100 microamperes in proportion to the I_{DD} of the TLV2262. When designing with lower-impedance loads (less than 50 kΩ) with the TLV2262, the lower drive capability to the positive rail needs to be taken into consideration. Although the TLV2262 topology provides lower drive to the positive rail than other high-drive-output rail-to-rail operational amplifiers, it is a more stable topology.

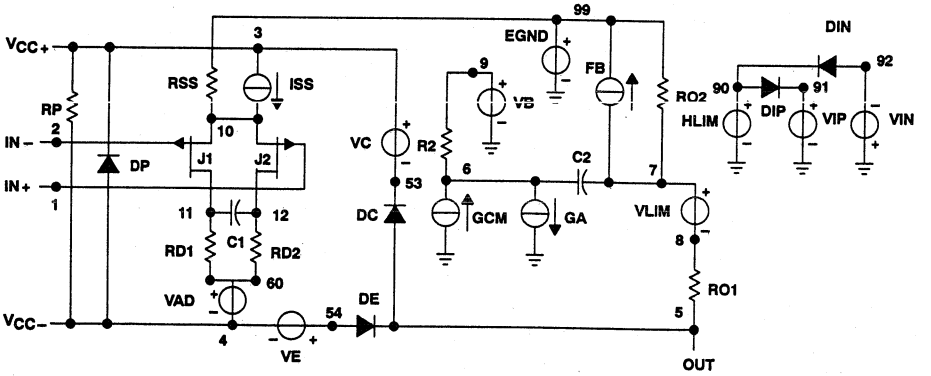
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice® Parts*™ model generation software. The Boyle macromodel and subcircuit in Figure 54 are generated using the TLV2262 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE: 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLV2262 1 2 3 4 5
C1      11    12    5.004E–12
C2      6     7     20.00E–12
DC      5     53    DX
DE      54    5     DX
DLP     90    91    DX
DLN     92    90    DX
DP      4     3     DX
EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
FB      7     99    POLY (5) VB VC VE VLP
+ VLN 0 5.89E6 –10E6 10E6 10E6 –10E6
GA      6     0     11    12 62.83E–6
GCM     0     6     10    99 22.34E–9
ISS     3     10    DC 11.00E–6
HLIM    90    0     VLIM 1K
J1      11    2     10 JX
J2      12    1     10 JX
R2      6     9     100.0E3
RD1     60    11    15.92E3
RD2     60    12    15.92E3
R01     8     5     135
R02     7     99    135
RP      3     4     15.87E3
RSS     10    99    18.18E6
VAD     60    4     –.5
VB      9     0     DC 0
VC      3     53    DC .6
VE      54    4     DC .6
VLIM    7     8     DC 0
VLP     91    0     DC 0
VLN     0     92    DC 9.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=717.8E–6
+ VTO=–.04)
.ENDS
```

Figure 54. Boyle Macromodel and Subcircuit

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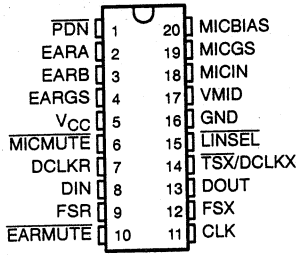
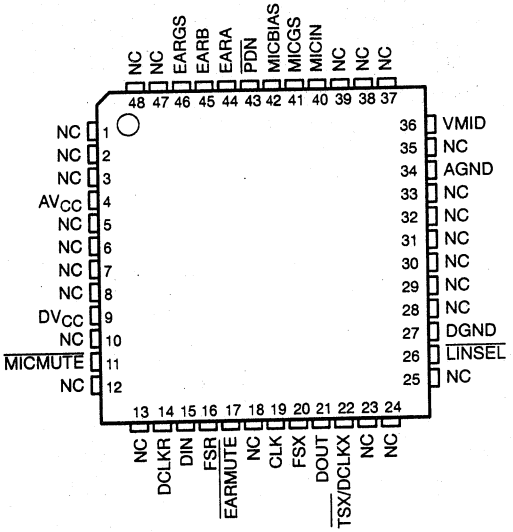
Parts is a trademark of MicroSim Corporation

- Single 3-V Operation
- Low Power Consumption:
  Operating Mode . . . 20 mW Typ
  Standby Mode . . . 5 mW Typ
  Power-Down Mode . . . 2 mW Typ
- Combined ADC, DAC, and Filters
- Electret Microphone Bias Reference Voltage Available
- Drives a Piezo Speaker Directly
- Compatible With All DSPs
- Selectable Between 8-Bit Companded and 13-Bit (Dynamic Range) Linear Conversion:
  TLV320AC36 . . . μ-Law and Linear Modes
  TLV320AC37 . . . A-Law and Linear Modes
- Programmable Volume Control in Linear Mode
- Designed for Standard 2.048-MHz Master Clock for U.S. Analog, U.S. Digital, CT2, DECT, GSM, and PCN Hand-Held Battery-Powered Telephones

DW OR N PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLV320AC36 and TLV320AC37 voice-band audio processor (VBAP™) integrated circuits are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) together with transmit and receive filtering for voice-band communications systems. Cellular telephone systems are targeted in particular; however, these integrated circuits can function in other systems including digital audio, telecommunications, and data acquisition.

These devices are pin-selectable for either of two modes, providing data in two formats: companded and linear. When the device is in the companded mode, data is transmitted and received in eight-bit words. When the linear mode is selected, 13 bits of data are sent and received, padded with zeros to provide a 16-bit word.

Caution. These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description (continued)

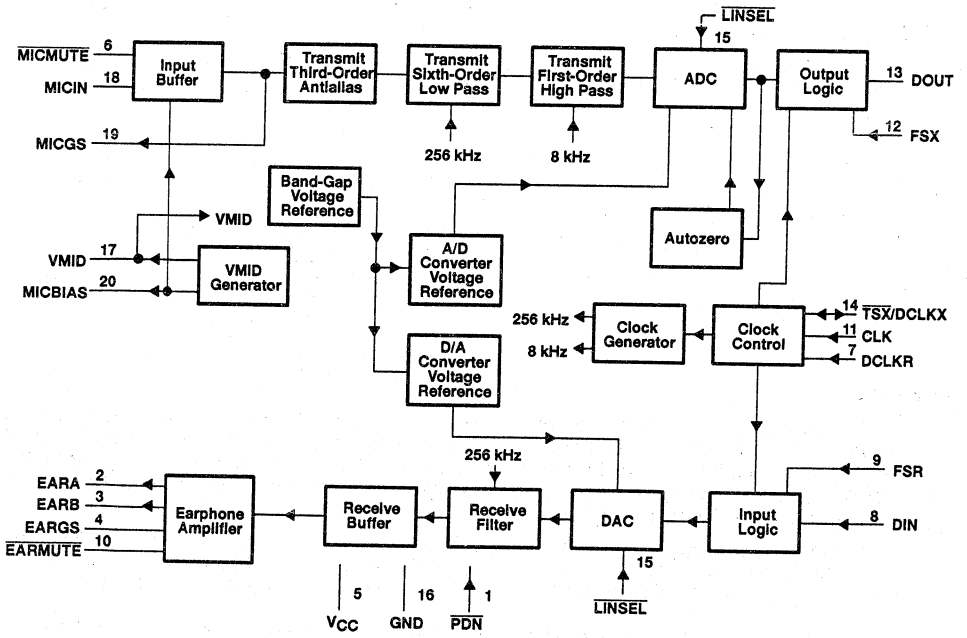
The transmit section is designed to interface directly with an electret microphone element. The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through antialiasing and band-pass filters. The filtered signal is then applied to the input of a compressing analog-to-digital converter (COADC) if companded mode is selected. Otherwise, the analog-to-digital converter performs a linear conversion.

The receive section takes a frame of serial data on DIN and converts it to analog through an expanding digital-to-analog converter (EXDAC) if the companded mode is selected; otherwise, a linear conversion is performed. The analog signal then passes through switched capacitor filters, which provide out-of-band rejection, (sin x)/x correction functions, and smoothing. The filtered signal is sent to the earphone amplifier. The earphone amplifier has a differential output with adjustable gain and is designed to minimize static power dissipation.

A single on-chip high-precision band-gap circuit generates all voltage references, eliminating the need for external reference voltages. An internal reference voltage equal to $V_{CC}/2$, VMID, is used to develop the mid-level virtual ground for all the amplifier circuits and the microphone bias circuit. Another reference voltage, MICBIAS, can be used to supply bias current for the microphone.

The TLV320AC3xC devices are characterized for operation from 0°C to 70°C. The TLV320AC3xI devices are characterized from −40°C to 85°C.

functional block diagram



Pin numbers shown are for the DW and N packages.

TEXAS INSTRUMENTS

Terminal Functions

TERMINAL NAME	TERMINAL NO. DW, N	TERMINAL NO. PT	I/O	DESCRIPTION
AGND	—	34		Ground return for all internal analog circuits
AV_{CC}	—	4		3-V supply voltage for all internal analog circuits
CLK	11	19	I	In the fixed-data-rate mode, CLK is the master clock input as well as the transmit and receive data clock input. In the variable-data-rate mode, CLK serves only as the master clock input.
DCLKR	7	14	I	Selects fixed- or variable-data-rate operation. When DCLKR is connected to V_{CC}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{CC}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock.
DGND	—	27		Ground return for all internal digital circuits
DIN	8	15	I	Receive data input. Input data is clocked in on consecutive negative transitions of the receive data clock, which is CLK for a fixed data rate and DCLKR for a variable data rate.
DOUT	13	21	O	Transmit data output. Transmit data is clocked out on consecutive positive transitions of the transmit data clock, which is CLK for a fixed data rate and DCLKX for a variable data rate.
DV_{CC}	—	9		3-V supply voltage for all internal digital circuits
EARA	2	44	O	Earphone output. EARA forms a differential drive when used with the EARB signal.
EARB	3	45	O	Earphone output. EARB forms a differential drive when used with the EARA signal.
EARGS	4	46	I	Earphone gain set input of feedback signal for the earphone output. The ratio of an external potential divider network connected across EARA and EARB adjusts the power amplifier gain. Maximum gain occurs when EARGS is connected to EARB. Minimum gain occurs when EARGS is connected to EARA. Earphone frequency response correction is performed using an RC approach.
$\overline{\text{EARMUTE}}$	10	17	I	Earphone output mute control signal. When $\overline{\text{EARMUTE}}$ is low, the output amplifier is disabled and no audio is sent to the earphone.
FSR	9	16	I	Frame-synchronization clock input for receive channel. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby state when FSR is TTL low for five frames or longer. The device enters a production test-mode condition when either FSR or FSX is held high for five frames or longer.
FSX	12	20	I	Frame-synchronization clock input for transmit channel. FSX operates independently of, but in an analogous manner to, FSR. The transmit channel enters the standby state when FSX is low for five frames or longer. The device enters a production test-mode condition when either FSX or FSR is held high for five frames or longer.
GND	16	—		Ground return for all internal circuits
$\overline{\text{LINSEL}}$	15	26	I	Linear selection input. When low, $\overline{\text{LINSEL}}$ selects linear coding/decoding. When high, $\overline{\text{LINSEL}}$ selects companded coding/decoding. Companding code on the 'AC36 is μ-law, and companding code on the 'AC37 is A-law.
MICBIAS	20	42	O	Bias voltage equal to VMID for the electret microphone
MICGS	19	41	O	Output of the internal microphone amplifier. MICGS is used as the feedback to set the microphone amplifier gain. If sidetone is required, it is accomplished by connecting a series network between MICGS and EARGS.
MICIN	18	40	I	Electret microphone input to the internal microphone amplifier
$\overline{\text{MICMUTE}}$	6	11	I	Microphone input mute control signal. When $\overline{\text{MICMUTE}}$ is active (low), zero code is transmitted.
$\overline{\text{PDN}}$	1	43	I	Power-down input. When low, the device powers down to reduce power consumption.
$\overline{\text{TSX}}$/DCLKX	14	22	I/O	Transmit time-slot strobe (active-low output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this is an open-drain output that pulls to ground and is used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock input.
V_{CC}	5	—		3-V supply voltage for all internal circuits
VMID	17	36	O	$V_{CC}/2$ bias voltage reference. An external, low-leakage, high-frequency 1-μF capacitor should be connected to VMID for filtering.

general information

system reliability features

The device should be powered up and initialized as follows:

1. Apply GND.
2. Apply V_{CC}.
3. Connect all clocks.
4. Apply TTL high to $\overline{PDN}$.
5. Apply synchronizing pluses to FSX and/or FSR.

Even though the VBAP is heavily protected against latch-up, it is still possible to cause it to latch-up under certain improper power conditions. To ensure that latch-up does not occur, a reverse-biased Schottky diode should be connected between V_{CC} (power supply) and GND.

On the transmit channel, digital outputs DOUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 µs) after power up (application of V_{CC}). After this delay, DOUT, $\overline{TSX}$, and signaling are functional and occur in the proper time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. To further enhance system integrity, DOUT and $\overline{TSX}$ are placed in a high-impedance state after an interruption of CLK.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level, and the device remains active. In the power-down mode, the average power consumption is reduced to 2 mW.

Three standby modes give the user the options of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is pulsing and FSR is held low. For receive-only operation (transmit section on standby), FSR is pulsing and FSX is held low. When the entire device is in standby mode, power consumption is reduced to 5 mW. See Table 1 for power-down and standby procedures.

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{PDN}$ = high, FSX = pulses, FSR = pulses	20 mW	Digital outputs active but not loaded
Power down	$\overline{PDN}$ = low, FSX/FSR = X/X	2 mW	$\overline{TSX}$ and DOUT in a high-impedance state
Entire device on standby	FSX = low, FSR = low, $\overline{PDN}$ = high	5 mW	$\overline{TSX}$ and DOUT in a high-impedance state
Only transmit on standby	FSX = low, FSR = pulses, $\overline{PDN}$ = high	10 mW	$\overline{TSX}$ and DOUT in a high-impedance state within 5 frames
Only receive on standby	FSR = low, FSX = pulses, $\overline{PDN}$ = high	10 mW	Digital outputs active but not loaded

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{CC} and uses the master clock (CLK), frame-synchronization clocks (FSX and FSR), and the $\overline{TSX}$ output. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR. A D/A conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter. The data word is eight bits long in the companded mode and sixteen bits long in the linear mode.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the receive data clock. In this mode, the master clock (CLK) controls the switched-capacitor filters, while data transfer into DIN and out of DOUT is controlled by DCLKR and DCLKX, respectively. This allows the data to be transferred into and out of the device at any rate up to the frequency of the master clock. DCLKR and DCLKX must be synchronous with CLK.

While the FSX input is high, data is transmitted from DOUT on consecutive positive transitions of DCLKX. Similarly, while the FSR input is high, the data word is received at DIN on consecutive negative transitions of DCLKR. The transmitted data word at DOUT is repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the data word to be transmitted more than once per frame, is available only with variable-data-rate timing.

asynchronous operations

To avoid crosstalk problems associated with special interrupt circuits, the design includes separate converters, filters, and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame.

precision voltage references

A precision band-gap reference voltage is generated internally and is used to supply all the references required for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This ensures very accurate, stable gain performance over variations in supply voltage and device temperature.

conversion laws

The TLV320AC36 provides μ-law companding operation as specified by CCITT G.711 recommendation. The TLV320AC37 provides A-law companding operation as specified by CCITT G.711 recommendation. The linear mode of operation is the same for both the TLV320AC36 and the TLV320AC37, and uses a 13-bit 2's-complement format.

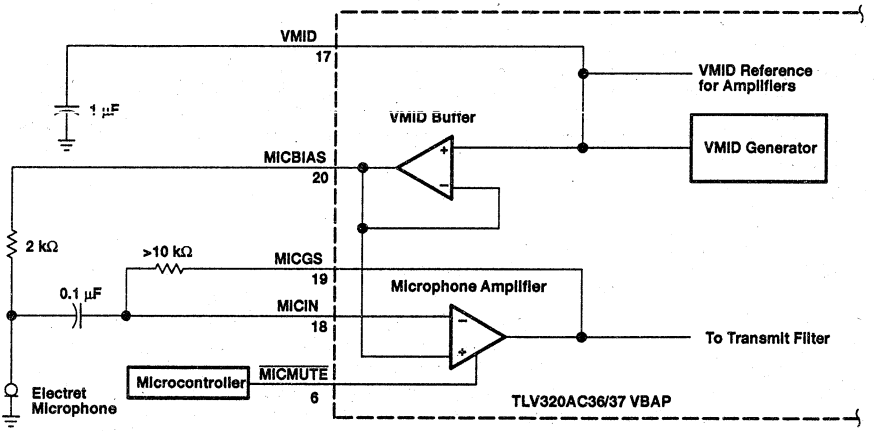
transmit operation

microphone input

The microphone input amplifier is specifically designed to interface to electret-type microphone elements as shown in Figure 1. The VMID buffer circuit provides a voltage (MICBIAS) equal to 1/2 V_{CC} as a reference for the microphone amplifier and a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network and applied to the amplifier inverting input (MICIN) to set the amplifier gain. VMID appears at a terminal to provide a place to filter the VMID voltage.

microphone mute function

The $\overline{\text{MICMUTE}}$ input causes the digital circuitry to transmit all zero code of DOUT.



Pin numbers shown are for the DW and N packages.

Figure 1. Typical Microphone Interface

transmit filter

A low-pass antialiasing filter section is included on the device and achieves 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first eight or 16 data clock cycles of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder.

data word structure

The data word is eight bits long in the companded mode and all eight bits represent one audio data sample. The sign bit is the first bit transmitted.

The data word is 16 bits long in the linear mode. The first 13 bits comprise the audio data sample, and the last three bits are volume control in the receive direction (DIN) and zeros in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

In the companded mode, the serial data word is received at DIN on the first eight clock cycles in fixed-data rate and on the last eight clock cycles in variable-data rate. In the linear mode, the serial data word is received at DIN on the first 13 clock cycles. Digital-to-analog conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive buffer

The receive buffer contains the volume control.

earphone amplifier

The earphone amplifier has a balanced output to allow maximum flexibility in output configuration. The output amplifier is designed to directly drive a piezo earphone in the differential configuration without any additional external components. The output can also be used to drive a single-ended load with the output signal voltage centered around $V_{CC}/2$.

The receive channel output level can be adjusted between specified limits by connecting an external resistor network to EARGS.

receive data format

In the companded mode, eight bits of data are received. The sign bit is the first bit received (see Table 2).

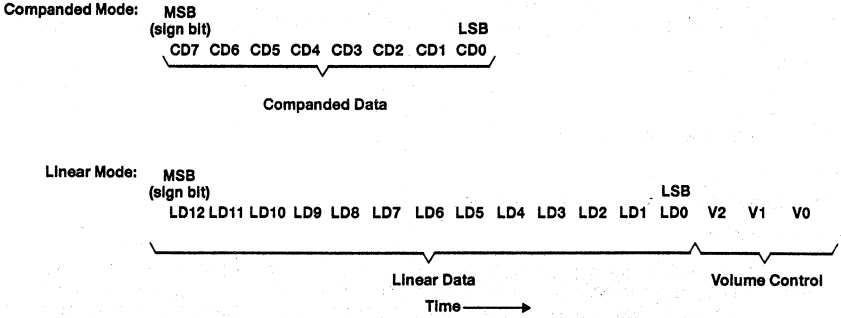
In the linear mode, 16 bits of data are received. The first 13 bits are the D/A code, and the remaining three bits form the volume control word (see Table 2). The volume control function is actually an attenuation control in which the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps giving a maximum attenuation of 21 dB when all bits are 1s. The volume control bits are not latched into the VBAP and must be present in each received data word.

Table 2. Receive Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
0	CD7	LD12
1	CD6	LD11
2	CD5	LD10
3	CD4	LD9
4	CD3	LD8
5	CD2	LD7
6	CD1	LD6
7	CD0	LD5
8	–	LD4
9	–	LD3
A	–	LD2
B	–	LD1
C	–	LD0
D	–	V2
E	–	V1
F	–	V0

relationship between data word and frame sync

Volume control and other control bits always follow the PCM data in time:



where:

CD7–CD0 = Data word when in companded mode
— = Unused bits in companded mode
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 3 dBm0
111 = minimum volume, –18 dBm0
LD12–LD0 = Data word when in linear mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 5.5 V
Output voltage range at DOUT, V_O ..... −0.3 V to 5.5 V
Input voltage range at DIN, V_I ..... −0.3 V to 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage value is with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
PT	1075 mW	7.1 mW/°C	756 mW	649 mW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)		2.7	5	V
High-level input voltage, V_{IH}		2.2		V
Low-level input voltage, V_{IL}			0.8	V
Load resistance between EARA and EARB, R_L (see Note 4)		600		Ω
Load capacitance between EARA and EARB, C_L (see Note 4)			50	nF
Operating free-air temperature, T_A	TLV320AC36C, TLV320AC37C	0	70	°C
	TLV320AC36I, TLV320AC37I	−40	85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the following sequence should be followed when applying power:
(1) Connect to GND.
(2) Connect V_{CC}.
(3) Connect the input signals.
When removing power, follow the preceding steps in reverse order.
3. Voltages at analog inputs and outputs and V_{CC} are with respect to GND.
4. R_L and C_L should not be applied simultaneously.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

supply current, f_{DCLK} = 2.048 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC} Supply current from V_{CC}	Operating	$\overline{PDN}$ is high with CLK signal present		6.2	7.5	mA
	Power down	$\overline{PDN}$ is low for 500 µs			0.75	
	Standby – both	$\overline{PDN}$ is high with FSX and FSR missing for 500 µs			2	
	Standby – one	$\overline{PDN}$ is high with FSX and FSR missing for 500 µs			4.5	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (continued)

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	I_{OH} = −3.2 mA, V_{CC} = 3 V	2.2	2.8		V
V_{OL}	Low-level output voltage		I_{OL} = 3.2 mA, V_{CC} = 3 V		0.2	0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	μA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	μA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

microphone interface‡

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset channel voltage at MICIN to DOUT		V_I = 0 to 3 V			±5	mV
I_{IB}	Input bias current at MICIN					±200	nA
B_1	Unity-gain bandwidth, open loop at MICIN§				1.5		MHz
C_i	Input capacitance at MICIN					5	pF
A_V	Large-signal voltage amplification at MICGS					10000	V/V
$I_{O(max)}$	Maximum output current	VMID				500	μA
		MICBIAS (source only)				1	mA

speaker interface‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	Peak-to-peak ac output voltage				3¶	Vp–p
	Output offset voltage at EARA, EARB (single ended)	Relative to GND			80	mVpk
I_{IL}	Input leakage current at EARGS	V_I = 0 to 4 V			±200	nA
$I_{O(max)}$	Maximum output current	R_L = 600 Ω			±2.5	mA
r_o	Output resistance at EARA, EARB			1		Ω
	Gain change	$\overline{\text{EARMUTE}}$ low, max level when muted	−64			dB

† All typical values are at V_{CC} = 3 V and T_A = 25°C.
‡ All parameters are measured between MICIN and GND (unless otherwise noted).
§ The frequency of the first pole is 100 Hz.
¶ 2.5 V_{p-p} when V_{CC} is 2.7 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (continued)

transmit gain and dynamic range, companded or linear mode, μ-law or A-law, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 5 and 6)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit reference-signal level (see Note 7)	Companded mode selected, μ-law ('AC36)		0.614	Vrms
	Companded mode selected, A-law ('AC37)		0.616	
	Linear mode selected ('AC36 and 'AC37)		0.626	
Overload-signal level (MICIN at unity gain)	Companded mode selected, μ-law ('AC36)		2.5	Vp-p
	Companded mode selected, A-law ('AC37)		2.5	
	Linear mode selected ('AC36 and 'AC37)		2.5	
Absolute gain error	0-dB input signal		±1	dB
Gain error with input level relative to gain at –10 dB	MICIN to DOUT at 3 dBm0 to –40 dBm0		±0.5	dB
	MICIN to DOUT at –41 dBm0 to –50 dBm0		±1.5	
	MICIN to DOUT at –51 dBm0 to –55 dBm0		±2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

transmit filter transfer, μ-law, A-law, or linear mode selected, over recommended ranges of supply voltage and free-air temperature, CLK = 2.048 MHz, FSX = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output signal at MICIN is 0 dB	f_{MICIN} = 50 Hz	–10	0	dB
		f_{MICIN} = 200 Hz	–2.8	0	
		f_{MICIN} = 300 Hz to 3 kHz		±0.25	
		f_{MICIN} = 3.3 kHz	–0.55	0.2	
		f_{MICIN} = 3.4 kHz	–1	–0.1	
		f_{MICIN} = 4 kHz		–14	
		f_{MICIN} ≥4.6 kHz		–32	

transmit idle channel noise and distortion, companded mode, μ-law or A-law, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, psophometrically weighted	MICIN connected to MICGS through a 10-kΩ resistor		–72	dBop
Transmit noise, C-message weighted	MICIN connected to MICGS through a 10-kΩ resistor		10	dBrnCo
Transmit signal-to-distortion ratio with sine-wave input MICIN to DOUT	MICIN to DOUT at 0 dBm0 to –30 dBm0	36		dB
	MICIN to DOUT at –31 dBm0 to –40 dBm0	30		
	MICIN to DOUT at –41 dBm0 to –45 dBm0	20		
Intermodulation distortion, 2-tone CCITT method, composite power level –13 dBm0	CCITT G.712 (7.1), R2	48		dB
	CCITT G.712 (7.2), R3	48		

NOTES: 5. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
6. The input amplifier is set for inverting unity gain.
7. The reference-signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 2 V.
8. Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level)

transmit idle channel noise and distortion, linear mode, over recommended ranges of supply voltage and operating free-air temperature (see Notes 6 and 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 10-kΩ resistor		200	μVrms
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –6 dBm0	48		dB
	MICIN to DOUT at –7 dBm0 to –12 dBm0	46		
	MICIN to DOUT at –13 dBm0 to –18 dBm0	40		
	MICIN to DOUT at –19 dBm0 to –24 dBm0	36		
	MICIN to DOUT at –25 dBm0 to –45 dBm0	24		

receive gain and dynamic range, companded or linear mode, μ-law or A-law, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive reference-signal level at analog output with unity gain (0 dB) (see Note 11)	Companded mode selected, μ-law ('AC36)		0.736	Vrms
	Companded mode selected, A-law ('AC37)		0.739	
	Linear mode selected ('AC36 and 'AC37)		0.751	
Overload-signal level, peak-to-peak	Companded mode selected, μ-law ('AC36)		3	Vp-p
	Companded mode selected, A-law ('AC37)		3	
	Linear mode selected ('AC36 and 'AC37)		3	
Absolute gain error	0-dB input signal		±1	dB
Gain error with output level relative to gain at –10 dBm0	DIN to EARA and EARB at 3 dBm0 to –40 dBm0		±0.5	dB
	DIN to EARA and EARB at –41 dBm0 to –50 dBm0		±1.5	
	DIN to EARA and EARB at –51 dBm0 to –55 dBm0		±2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature, FSR = 8 kHz (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	DIN = 0 dBm0	f_{DIN} = < 200 Hz		0.25	dB
		f_{DIN} = 200 Hz	–0.5	0.25	
		f_{DIN} = 300 Hz to 3 kHz		±0.25	
		f_{DIN} = 3.3 kHz	–0.55	0.2	
		f_{DIN} = 3.4 kHz	–1	–0.1	
		f_{DIN} = 4 kHz		–14	
		f_{DIN} = > 4.6 kHz		–30	

NOTES: 6. The input amplifier is set for inverting unity gain.
8. Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level)
9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
10. Unless otherwise noted, the digital input is a word stream generated by passing a 0-dB sine wave at 1020 Hz through an ideal encoder where 0 dB is defined as the zero reference.
11. This reference-signal level is measured at the speaker output of the receive channel with the gain of the output speaker amplifier set to unity.

receive idle channel noise and distortion, companded mode, μ-law or A-law, over recommended ranges of supply voltage and operating free-air temperature (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise, psophometrically weighted	DIN = 11010101 (A-law)		–72	dBop
Receive noise, C-message weighted	DIN = 11111111 (μ-law)		8	dBrnCo
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –30 dBm0	36		dB
	DIN to EARA and EARB at –31 dBm0 to –40 dBm0	30		
	DIN to EARA and EARB at –41 dBm0 to –45 dBm0	24		

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, linear mode, over recommended ranges of supply voltage and operating free-air temperature (see Notes 9 and 12)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise	DIN = 00000000		250	μVrms
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –5 dBm0	48		dB
	DIN to EARA and EARB at –6 dBm0 to –12 dBm0	46		
	DIN to EARA and EARB at –13 dBm0 to –18 dBm0	40		
	DIN to EARA and EARB at –19 dBm0 to –24 dBm0	36		
	DIN to EARA and EARB at –25 dBm0 to –45 dBm0	25		
Intermodulation, 2-tone CCITT distortion method, composite power level –13 dBm0	CCITT G.712 (7.1), R2	48		dB
	CCITT G.712 (7.2), R3	48		

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
12. Receive noise, linear mode: 200 μVrms is equivalent to –71 dB (referenced to device 0-dB level)

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply-voltage rejection, transmit channel	Idle channel, supply signal = 100 mVrms, f = 0 to 30 kHz (measured at DOUT)		–30		dB
Supply-voltage rejection, receive channel	Idle channel, supply signal = 100 mVrms, EARGS connected to EARB, f = 0 to 30 kHz (measured differentially between EARA and EARB)		–30		dB
Crosstalk attenuation, transmit to receive (differential)	MICIN = 0 dB, f = 1.02 kHz, unity transmit gain, EARGS connected to EARB, measured differentially between EARA and EARB	60			dB
Crosstalk attenuation, receive to transmit	DIN = 0 dBm0, f = 1.02 kHz, unity transmit gain, measured at DOUT	60			dB

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 2, 3, 4, and 5)

		MIN	NOM‡	MAX	UNIT
t_t	Transition time, CLK and DCLK			10	ns
	Duty cycle, CLK	45%	50%	55%	
	Duty cycle, DCLK	45%	50%	55%	

‡ All nominal values are at V_{CC} = 3 V, T_A = 25°C.

transmit timing requirement over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX	20	468	ns
$t_{h(FSX)}$	Hold time, FSX	20	468	ns

receive timing requirement over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 2)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR	20	468	ns
$t_{h(FSR)}$	Hold time, FSR	20	468	ns
$t_{su(DIN)}$	Setup time, DIN	20		ns
$t_{h(DIN)}$	Hold time, DIN	20		ns

transmit timing requirement over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 5)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX	40	$t_{c(DCLKX)}-40$	ns
$t_{h(FSX)}$	Hold time, FSX	35	$t_{c(DCLKX)}-35$	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR	40		ns
$t_{h(FSR)}$	Hold time, FSR	35	$t_{c(DCLKR)}-35$	ns
$t_{su(DIN)}$	Setup time, DIN	30		ns
$t_{h(DIN)}$	Hold time, DIN	30		ns

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode, C_L = 0 to 10 pF, (see Figures 2 and 3)

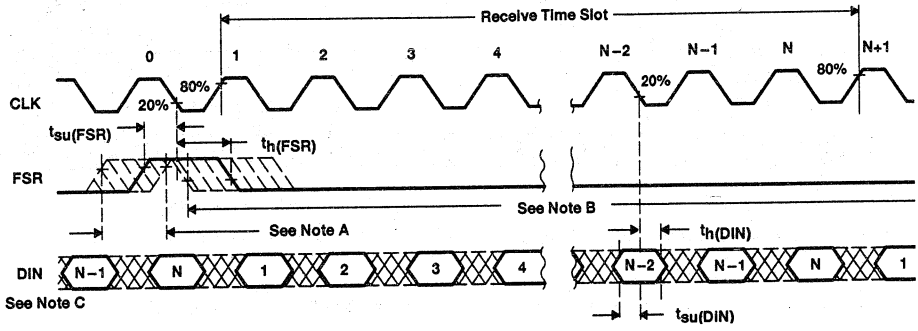
		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From CLK bit 1 high to DOUT bit 1 valid			35	ns
t_{pd2}	From CLK high to DOUT valid, bits 2 to n			35	ns
t_{pd3}	From CLK bit n low to DOUT bit n HI-Z		30		ns
t_{pd4}	From CLK bit 1 high to $\overline{TSX}$ active (low)	R_{pullup} = 1.24 kΩ		40	ns
t_{pd5}	From CLK bit n low to $\overline{TSX}$ inactive (high)	R_{pullup} = 1.24 kΩ	30		ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Figures 4 and 5)

		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	FSX high to DOUT bit 1 valid	C_L = 0 to 10 pF		30	ns
t_{pd7}	DCLKX high to DOUT valid, bits 2 to n	C_L = 0 to 10 pF		40	ns
t_{pd8}	FSX low to DOUT bit n Hi-Z		20		ns

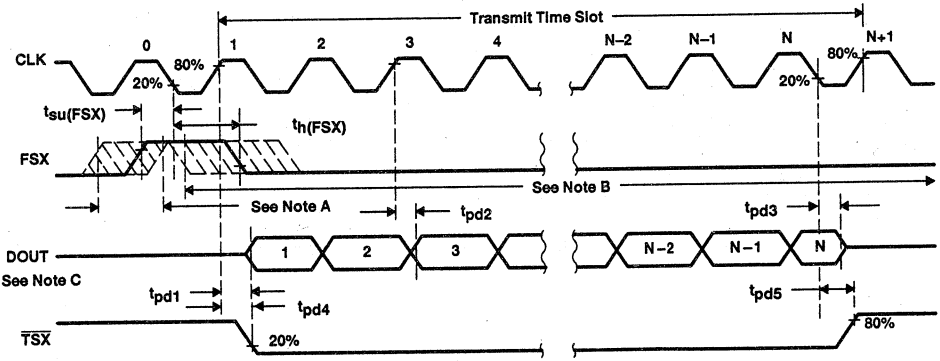
PARAMETER MEASUREMENT INFORMATION

All timing parameters are referenced to V_{IH} and V_{IL}. Bit 1 = MSB (most significant bit) and is clocked in first on DIN or clocked out first on DOUT. Bit n = LSB (least significant bit) and is clocked in last on DIN or is clocked out last on DOUT. N = 8 for the companded mode and N = 16 for the linear mode.



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

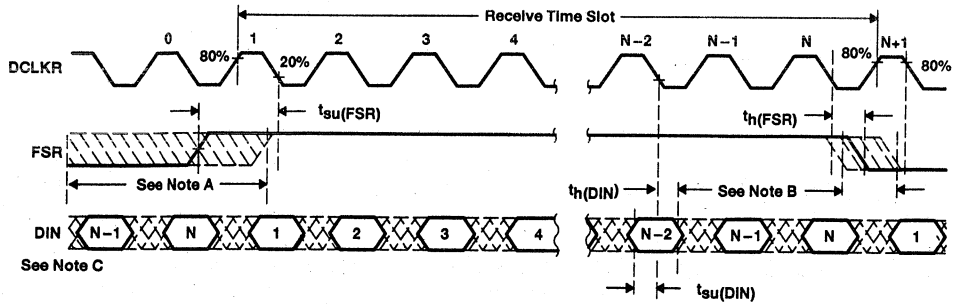
Figure 2. Fixed Data Rate, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low ($t_{h(FSX)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.

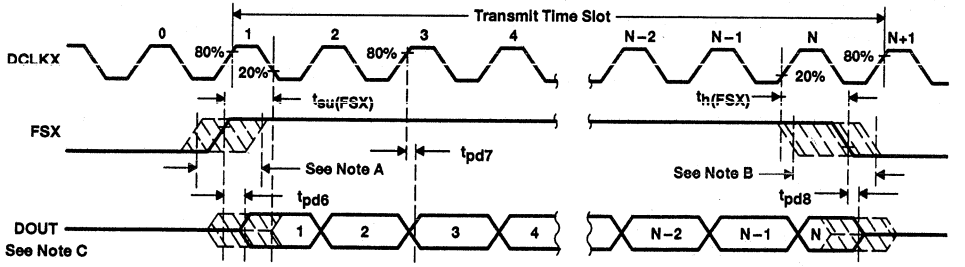
Figure 3. Fixed Data Rate, Transmit Side Timing Diagram

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for FSR high ($t_{su(FSR)}$ max determined by data collision considerations).
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 4. Variable Data Rate, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low without data repetition.
C. Transitions are measured at 50%.

Figure 5. Variable Data Rate, Transmit Side Timing Diagram

APPLICATION INFORMATION

output gain set design considerations (see Figure 6)

EARA and EARB are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at EARA
V_{O-} at EARB
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to EARGS.

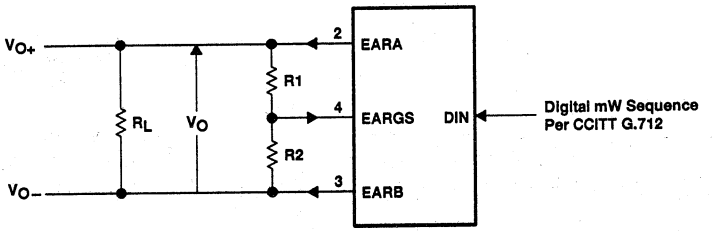
A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination R1 + R2 and R_L sets the total loading. The total capacitance at EARGS and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital mW output response (V_A = 1.001 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$



Pin numbers shown are for the DW and N package.

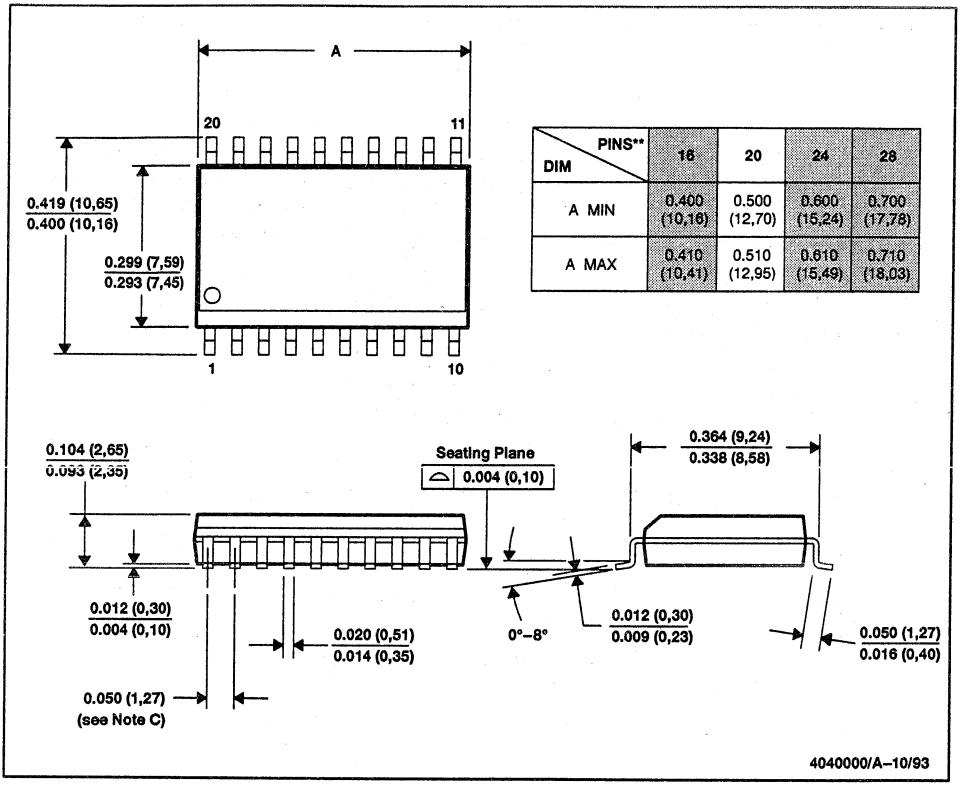
Figure 6. Gain-Setting Configuration

MECHANICAL DATA

DW/R-PDSO-G**

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

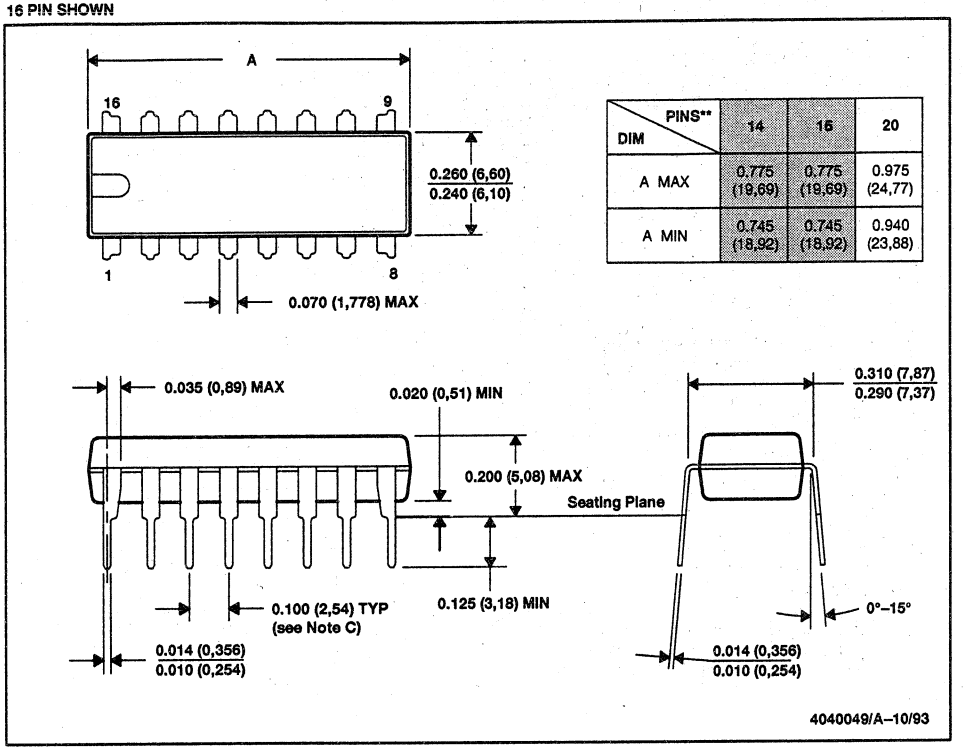
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

MECHANICAL DATA

N/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN

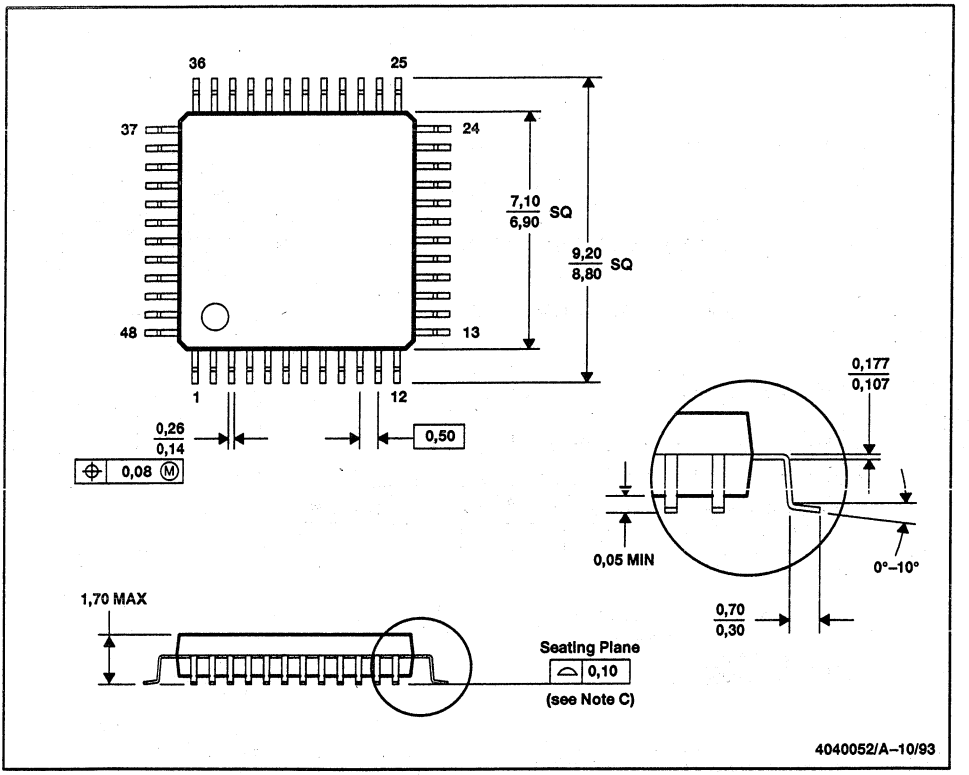


DIM \ PINS**	14	16	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.940 (23,88)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.

MECHANICAL DATA

PT/S-PQFP-G48 PLASTIC QUAD FLATPACK

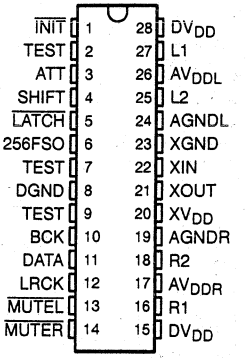


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

SLAS077B – SEPTEMBER 1993 – REVISED AUGUST 1994

- Single 5-V Power Supply
- Sample Rates (Fs) up to 48 kHz
- 18-Bit Resolution
- Pulse-Width-Modulation (PWM) Output
- Deemphasis Filter for Sample Rates of 32, 37.8, 44.1, and 48 kHz
- Mute With Zero-Data-Detect Flags
- Digital Attenuation to –60 dB
- Total Harmonic Distortion of 0.004% Maximum
- Total-Channel Dynamic Range of 96 dB Minimum
- Serial-Port Interface
- Differential Architecture
- 1-μm CMOS DLM Process
- 2s Complement Data Format

DWB PACKAGE
(TOP VIEW)



description

The TMS57014A is a stereo oversampled sigma-delta digital-to-analog converter (DAC) designed for use in systems such as compact disks, digital audio tapes, multimedia, and video cassette recorders. The device provides high-resolution signal conversion. This device consists of two identical synchronous conversion paths for left and right audio channels. Other overhead functions provide on-chip timing and control.

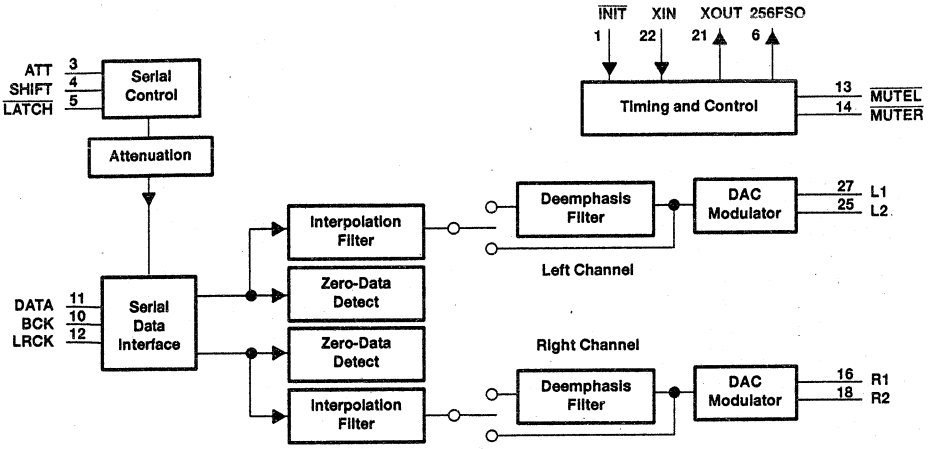
Additional features include muting, attenuation, deemphasis, and zero-data detection. These functions are implemented with 16-bit control words from a host controller or processor.

The TMS57014A is characterized for operation from 0°C to 70°C.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground.

TEXAS INSTRUMENTS

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ATT	3	I	Serial control data. ATT is a 16-bit word configured as LSB first (see Tables 2, 3, and 4).
AV_{DDL}	26	I	Analog power supply (left channel)
AV_{DDR}	17	I	Analog power supply (right channel)
AGNDL	24	I	Analog ground (left channel)
AGNDR	19	I	Analog ground (right channel)
BCK	10	I	Bit clock input. The shift clock signal is used to clock serial audio data into the device.
DATA	11	I	Audio data input. DATA can be configured as 16 or 18 bits with MSB or LSB first. DATA is 2s complement.
DV_{DD}	15, 28	I	Digital supply
DGND	8	I	Digital ground
$\overline{INIT}$	1	I	Reset. When $\overline{INIT}$ is brought low, the device is reset. The device is activated on the rising edge of $\overline{INIT}$. The LRCK signal must be applied to the device for a reset to occur.
$\overline{LATCH}$	5	I	Serial-control data latch. Control data is loaded into the internal registers when $\overline{LATCH}$ is brought low.
LRCK	12	I	Left/right clock. LRCK signifies whether the serial data is associated with the left-channel DAC (when high) or the right-channel DAC (when low).
$\overline{MUTEL}$	13	O	Left-channel mute flag active. When the left channel is muted or the data through the channel remains at zero for the system-register selected time, $\overline{MUTEL}$ is brought low.
$\overline{MUTER}$	14	O	Right-channel mute flag active. When the right channel is muted or the data through the channel remains at zero for the system-register selected time, $\overline{MUTER}$ is brought low.
L1	27	O	Left PWM output 1
L2	25	O	Left PWM output 2
R1	16	O	Right PWM output 1
R2	18	O	Right PWM output 2
SHIFT	4	I	Shift clock. SHIFT is used to clock the control data into the internal registers.
TEST	2, 7, 9	I	All TEST inputs should be tied low.
XIN	22	I	Master clock in. XIN is used to derive all the key logic signals of the device. XIN runs at 512Fs, where Fs is the sample rate.
XOUT	21	O	Master clock out
XV_{DD}	20	I	Power supply for clock section
XGND	23	I	Ground for clock section
256FSO	6	O	System clock out. 256FSO reflects the master clock input divided by 2. The rate is 256Fs, where Fs is the sample rate.

detailed description

The TMS57014A incorporates an interpolation FIR filter and oversampled modulator. The pulse-width-modulation (PWM) digital output is fed into an external low-pass filter to recover the analog audio signal.

Two control registers configure the device, the attenuation register that controls the attenuation range and the system register that controls additional functions described in Table 4.

reset/initialization

When $\overline{INIT}$ is brought low, an internal reset signal becomes active approximately 120 cycles of the sampling frequency (Fs) after the falling edge of $\overline{INIT}$. Under this condition, all internal circuits are initialized and the PWM output is held at zero data (50% duty cycle). When $\overline{INIT}$ is brought high, the internal reset signal goes inactive a maximum of five LRCK periods after the rising edge of $\overline{INIT}$. At this point, internal clocks are synchronous with LRCK and the PWM output is valid (see Figure 1). The LRCK signal must be applied for proper initialization.

reset/initialization (continued)

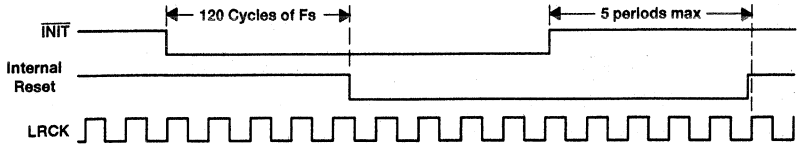


Figure 1. Reset Timing Relationships

timing and control

The timing and control circuit is used to generate and distribute necessary clocks throughout this design. XIN is the external master clock input. The sample rate of the data paths is set as LRCK = XIN/512. With a fixed oversampling ratio of 32x and each PWM output value requiring 16 XIN cycles, the effect of changing XIN is shown in Table 1.

The DAC can be operated at any conversion rate between 48 kHz and 32 kHz by choosing the appropriate master-clock frequency. Some of the functions of the converter, such as the deemphasis filter, are specified for operation only at the given frequencies in Table 1.

Table 1. Master Clock to Sample Rate Comparison

XIN (MHz)	256FSO (MHz)	LRCK (kHz)
24.5760	12.2880	48.0
22.5792	11.2896	44.1
19.3536	9.6768	37.8
16.3840	8.1920	32.0

digital audio data interface

The conversion cycle is synchronized to the rising edge of LRCK, and the data must meet the setup requirements specified in the timing requirements table. The input data is 16 or 18 bits with the MSB or LSB first as selected in the system register. The BCK frequency must be equal to or greater than 32 Fs for 16-bit data or 36 Fs for 18-bit data where Fs is the sample rate. Figure 2 illustrates the input timing.

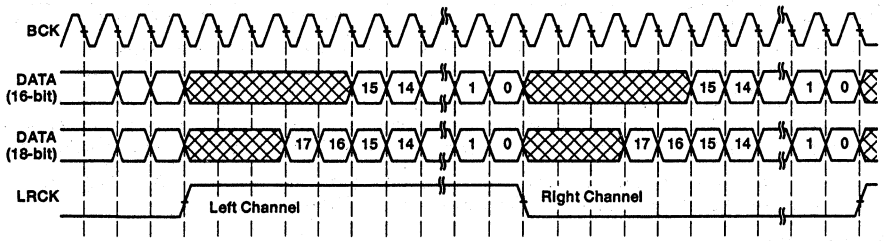


Figure 2. Audio-Data Input Timing

serial-control interface

The device uses the most-significant-bit-first format. Therefore, for a 16-bit word, D15 is the most significant bit and D0 is the least significant bit. Unless otherwise specified, all values are in 2s-complement format.

serial-control-data input

Device-control functions are implemented by the 16-bit control-data input. The TMS57014A has two registers for this data: the system register and the attenuation register. The system register contains most of the system configuration information, and the attenuation register controls audio output level, deemphasis, and mute. Figure 3 illustrates the input timing for ATT, SHIFT, and $\overline{\text{LATCH}}$. The data is loaded internally on the falling edge of $\overline{\text{LATCH}}$. The shift clock should be high for the $\overline{\text{LATCH}}$ setup time before $\overline{\text{LATCH}}$ is taken low.

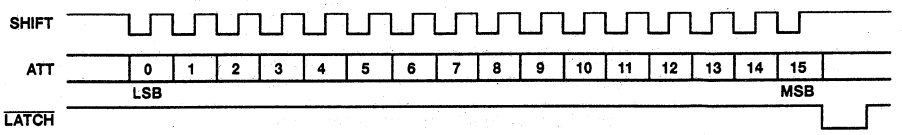


Figure 3. Control-Data-Input Timing

mute

When mute is activated, the output PWM becomes zero data (50% duty cycle). The two mute flags, $\overline{\text{MUTEL}}$ and $\overline{\text{MUTER}}$, are independently set low based on the data in the respective channel being zero. This function becomes active under the following conditions:

1. When the zero-data detector detects that the input data has been zero for 2500 cycles of Fs or 12500 cycles of Fs (as selected in the control registers), output is 50% duty cycle.
2. When the MUTE register value is set high by means of the serial-control data.
3. When $\overline{\text{INIT}}$ is active (low), output is 50% duty cycle.

zero-data detect

After the input data remains zero for 2500 or 12500 cycles of Fs as set by the system register (D4, D5), the channel-mute flag becomes active. Zero-data detection is available for both channels independently, so the two outputs ($\overline{\text{MUTER}}$ and $\overline{\text{MUTEL}}$) indicate that zero data has been detected on the respective channel. The detection period is selected by the zero-detect register value in the serial-control data. The mute flag returns high immediately when nonzero input data is received.

deemphasis filter

Four sets of deemphasis-filter coefficients have been selected to support four sampling rates (Fs): 32, 37.8, 44.1, and 48 kHz. Selection of the filter coefficients is accomplished through the internal register values. Also, the filter can be enabled or disabled through the internal register values. Figure 4 illustrates the deemphasis characteristics.

Many audio sources have been recorded with the preemphasis characteristics that are the inverse of the deemphasis characteristics shown in Figure 4. Deemphasis is provided to reconstruct the original frequency response.

deemphasis filter (continued)

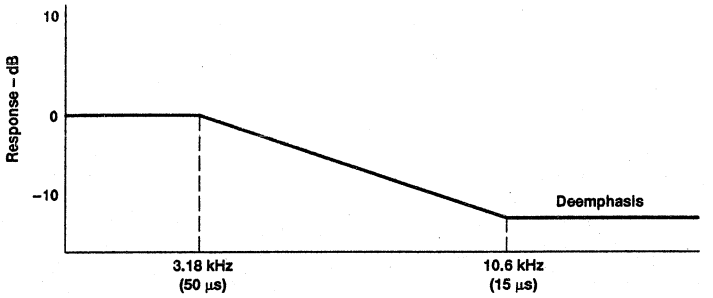


Figure 4. Deemphasis Characteristics

digital attenuation

The digital-audio-data input is attenuated by a value selected in the internal attenuation register. The attenuation value is 11 bits long with a valid range of hex values from 400h to 000h. A data value of 001h corresponds to an attenuation value of −60 dB and a data value of 400h corresponds to 0 dB. The attenuation function is nonlinear (see equation 1). Figure 5 demonstrates the attenuation function in dB. The default attenuation value is 400h.

$$\text{Attenuation} = 20 \log \left(\frac{\text{attenuation data}}{1024} \right) \quad (1)$$

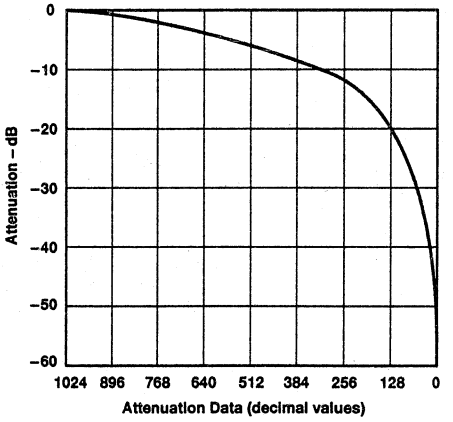


Figure 5. Digital Attenuation Characteristics

register set

Table 2 contains the register-set selection. The bit functions are listed in Tables 3 and 4.

Table 2. Register-Set Selection

BITS		DESCRIPTION
15	14	
0	0	Attenuation register
0	1	System register
1	x	Invalid condition†

† Bit 15 should always be set to 0 when writing data for proper operation.

Table 3. Attenuation-Register Bit Functions

BITS				FUNCTION
13	12	11	10–0	
0	—	—	—	Deemphasis off
1	—	—	—	Deemphasis on
—	0	—	—	Channel mute off
—	1	—	—	Channel mute on
—	—	0	—	Must be low
—	—	—	0	Digital attenuation, mute
—	—	—	1	Digital attenuation, –60.2 dB
—	—	—	2	Digital attenuation, –54.2 dB
—	—	—	3	Digital attenuation, –50.7 dB
—	—	—	. . .	
—	—	—	1FF	Digital attenuation, –6.04 dB
—	—	—	200	Digital attenuation, –6.02 dB
—	—	—	201	Digital attenuation, –6.00 dB
—	—	—	. . .	
—	—	—	3FF	Digital attenuation, –0.01 dB
—	—	—	400	Digital attenuation, 0.00 dB

Default = 0400h

NOTE: The attenuation values shown are typical values. Refer to the digital attenuation section for a description of the attenuation function.

Table 4. System-Register Bit Functions

BITS								FUNCTION
13	12	11–6	5	4	3–2	1	0	
0	—	—	—	—	—	—	—	MSB first, audio data
1	—	—	—	—	—	—	—	LSB first, audio data
—	0	—	—	—	—	—	—	16-bit, audio data
—	1	—	—	—	—	—	—	18-bit, audio data
—	—	0	—	—	—	—	—	Must be low
—	—	—	0	—	—	—	—	Zero data detect period (2500 cycles of Fs)
—	—	—	1	—	—	—	—	Zero data detect period (12500 cycles of Fs)
—	—	—	—	0	—	—	—	Must be low
—	—	—	—	—	0	—	—	Deemphasis – 44.1 kHz
—	—	—	—	—	1	—	—	Deemphasis – 48.0 kHz
—	—	—	—	—	2	—	—	Deemphasis – 37.8 kHz
—	—	—	—	—	3	—	—	Deemphasis – 32.0 kHz
—	—	—	—	—	—	0	—	LRCK and PWM not synchronized
—	—	—	—	—	—	1	—	LRCK and PWM synchronized
—	—	—	—	—	—	—	0	Must be low

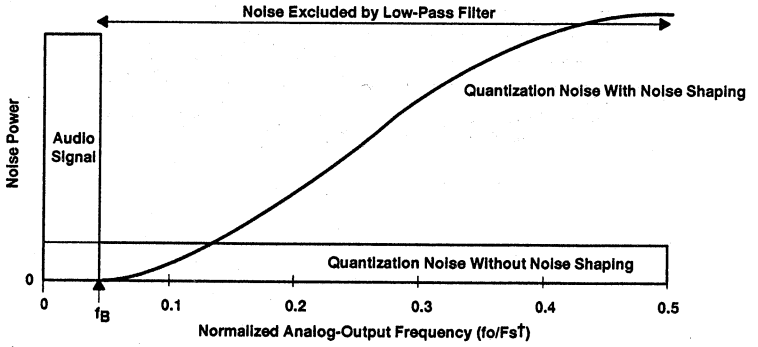
Default = 0000h

Interpolation filter

The interpolation filter used prior to the DAC increases the digital data rate from the LRCK speed to the oversampled rate by interpolating with a ratio of 1:32. The output of this filter is directed to the oversampling modulator with deemphasis as an option.

DAC modulator

The DAC is a 3rd-order modulator with 32 times oversampling. The DAC provides high-resolution, low-noise performance using a 15-value PWM output as shown in Figure 6.



† fo is the output frequency at the low-pass filter output (V_O) shown in Figure 10.

Figure 6. Oversampling Noise Power With and Without Noise Shaping

PWM output (L2–L1 and R2–R1)

The L2–L1 and the R2–R1 output pairs are pulse-width-modulated (PWM) signals with the L2–L1 differential pulse duration determining the left-channel analog voltage and the R2–R1 differential pulse duration determining the right-channel analog voltage.

Each DAC left and right output consists of 15 levels of PWM and provide a differential signal as the inputs to two external differential amplifiers configured as a low-pass filter to produce the left and right audio outputs (see Figure 9).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Analog supply voltage range, AV_{DDL}, AV_{DDR} (see Note 1) ..... −0.3 V to 7 V
Digital supply voltage range, DV_{DD} (see Note 2) ..... −0.3 V to 7 V
Clock supply voltage range, XV_{DD} (see Note 3) ..... −0.3 V to 7 V
Output voltage range: L1, L2 ..... −0.3 V to AV_{DDL} + 0.3 V
R1, R2 ..... −0.3 V to AV_{DDR} + 0.3 V
Input voltage range ..... −0.3 V to DV_{DD} + 0.3 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −55°C to 150°C
Case temperature for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values for maximum ratings are with respect to AGNDL and AGNDR, respectively.
2. Voltage values for maximum ratings are with respect to DGND.
3. Voltage values for maximum ratings are with respect to XGND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DDL}, AV_{DDR}		4.75	5	5.25	V
Digital supply voltage, DV_{DD}		4.75	5	5.25	V
Clock supply voltage, XV_{DD}		4.75	5	5.25	V
High-level input voltage, V_{IH}	XIN	0.9 V_{DD}			V
	All other digital inputs	0.76 V_{DD}			
Low-level input voltage, V_{IL}	XIN			0.1 V_{DD}	V
	All other digital inputs			0.24 V_{DD}	
Load resistance at PWM, R_L			10		kΩ
Master clock frequency at XIN		16.3		24.6	MHz
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

digital interface, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	256FSO	$I_O = -0.4$ mA	$V_{DD}-0.5$			V
		L1, L2, R1, R2	$I_O = -12$ mA	$V_{DD}-0.5$			
		XOUT	$I_O = -1.2$ mA	$V_{DD}-0.5$			
		$\overline{MUTEL}$, $\overline{MUTER}$	$I_O = -1$ mA	$V_{DD}-0.5$			
V_{OL}	Low-level output voltage	256FSO	$I_O = 0.4$ mA			0.4	V
		L1, L2, R1, R2	$I_O = 12$ mA			0.5	
		XOUT	$I_O = 1.2$ mA			0.5	
		$\overline{MUTEL}$, $\overline{MUTER}$	$I_O = 1$ mA			0.4	
I_{IH}	High-level input current, any digital input				±1	±5	µA
I_{IL}	Low-level input current, any digital input				±1	±5	µA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

supplies, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$, no load

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Analog power supply current	AV_{DDL} and AV_{DDR} are shorted together		15		mA
Digital power supply current			15		mA
Total device supply current over operating temperature range				60	mA
Power dissipation				350	mW

DAC modulator, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$, sample rate (Fs) = 44.1 kHz, full-scale input sine wave at 1 kHz, $T_A = 25°C$, bandwidth is 20 Hz to 20 kHz

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Resolution	See Note 4		18			bits
Signal-to-noise ratio	A-weighted, 20 Hz to 20 kHz, See Figure 10, Table 5, and Note 4	Deemphasis not selected	96	100		dB
Total harmonic distortion	20 Hz to 20 kHz, See Note 4			0.003%	0.004%	

filter characteristics, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$, deemphasis disabled

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Pass-band ripple	Sample rate (Fs) = 48 kHz, See Note 4	−0.002		0.002	dB
Stop-band attenuation		75			dB
Pass band (−3 dB) (DAC)	See Note 4	0		0.46 Fs	kHz
Stop band		0.54 Fs			kHz
Group delay			29/Fs		s

† All typical values are at $T_A = 25°C$.

NOTE 4: These specifications are measured at the output (V_O) of the low-pass filter shown in Figure 9.

timing requirements (see Figures 7 and 8 and Note 5)

		MIN	MAX	UNIT
t_{w1}	Pulse duration, BCK	160		ns
t_{su1}	Setup time, DATA before BCK↑	20		ns
t_{h1}	Hold time, DATA after BCK↑	20		ns
t_{su2}	Setup time, LRCK before BCK↑	50		ns
t_{h2}	Hold time, LRCK after BCK↑	50		ns
t_{w2}	Pulse duration, SHIFT	100		ns
t_{su3}	Setup time, ATT before SHIFT↑	20		ns
t_{h3}	Hold time, ATT after SHIFT↑	20		ns
t_{w3}	Pulse duration, $\overline{\text{LATCH}}$	100		ns
t_{su4}	Setup time, $\overline{\text{LATCH}}$ before SHIFT↑	100		ns
t_{h4}	Hold time, $\overline{\text{LATCH}}$ after SHIFT↑	t_{w2} + 20		ns

NOTE 5: All timing measurements were taken at the $V_{DD}/2$ voltage level.

PARAMETER MEASUREMENT INFORMATION

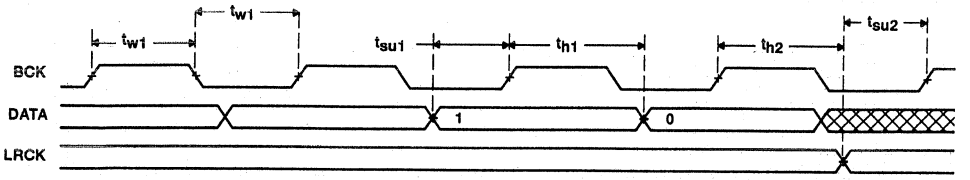


Figure 7. Audio-Data Serial Timing

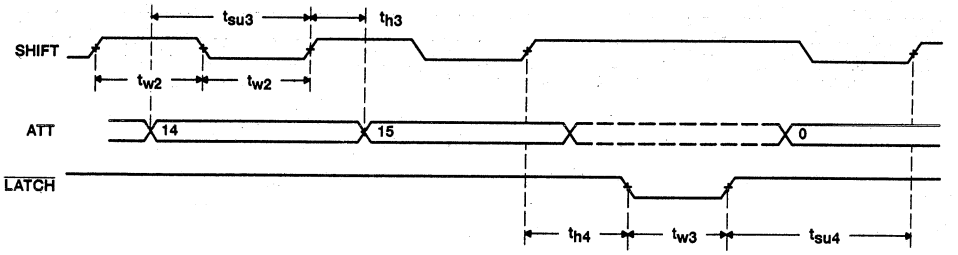


Figure 8. Control-Data Serial Timing

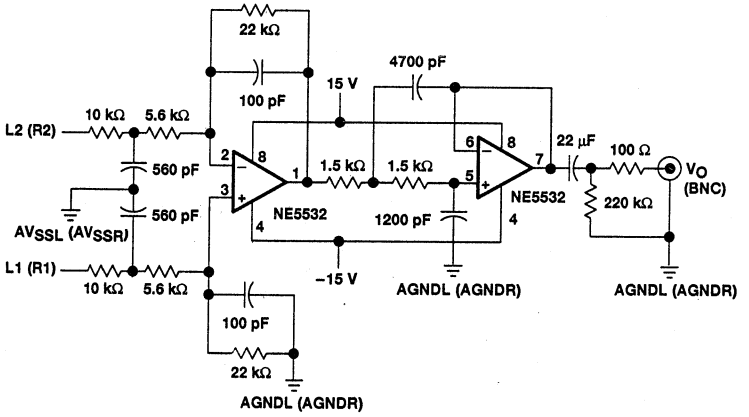


Figure 9. Analog Low-Pass Filter Recommended for Measuring the Dynamic Specifications of the TMS57014A

PARAMETER MEASUREMENT INFORMATION

Table 5. A-Weighted Data

FREQUENCY	A WEIGHTING (dB)	FREQUENCY	A WEIGHTING (dB)
25	−44.6 ±2	800	−0.1 ±1
31.5	−39.2 ±2	1000	0 ±0
40	−34.5 ±2	1250	0.6 ±1
50	−30.2 ±2	1600	1.0 ±1
63	−26.1 ±2	2000	1.2 ±1
80	−22.3 ±2	2500	1.2 ±1
100	−19.1 ±1	3150	1.2 ±1
125	−16.1 ±1	4000	1.0 ±1
160	−13.2 ±1	5000	0.5 ±1
200	−10.8 ±1	6300	−0.1 ±1
250	−8.6 ±1	8000	−1.1 ±1
315	−6.5 ±1	10000	−2.4 ±1
400	−4.8 ±1	12500	−4.2 ±2
500	−3.2 ±1	16000	−6.5 ±2
630	−1.9 ±1		

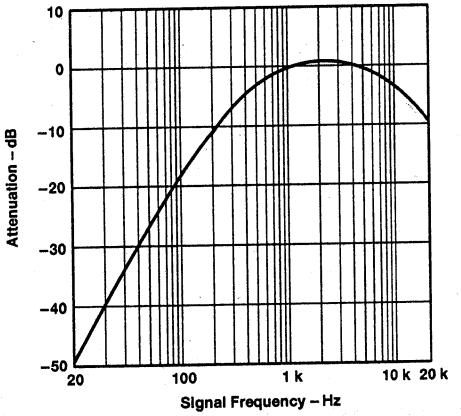


Figure 10. A-Weighted Function

APPLICATION INFORMATION

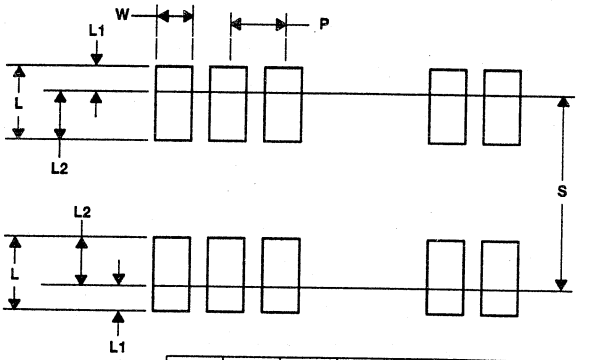
circuit and layout considerations

These guidelines should be followed for the best device performance.

- Separate digital and analog ground planes should be used. All digital device functions should be over the digital ground plane, and all analog device functions should be over the analog ground plane. The ground planes should be connected at only one point to the direct power supply only, and this is usually at the connector edge of the board.
- All digital signals should be synchronously generated from a single crystal-controlled clock.
- A 0.1-μF and a 1-μF capacitor should be used on all power supply lines. If clock noise is excessive, a toroidal inductance of 10 μH should be placed in series with XV_{DD} before connecting to DV_{DD}.
- The digital input control signals should be buffered if they are generated off the card.
- Clock jitter should be minimized, and precautions should be made to prevent clock overshoot. This minimizes any high-frequency coupling to the analog output.

PCB footprint

Figure 11 shows the printed-circuit-board land pattern for the TMS57014A small-outline package.



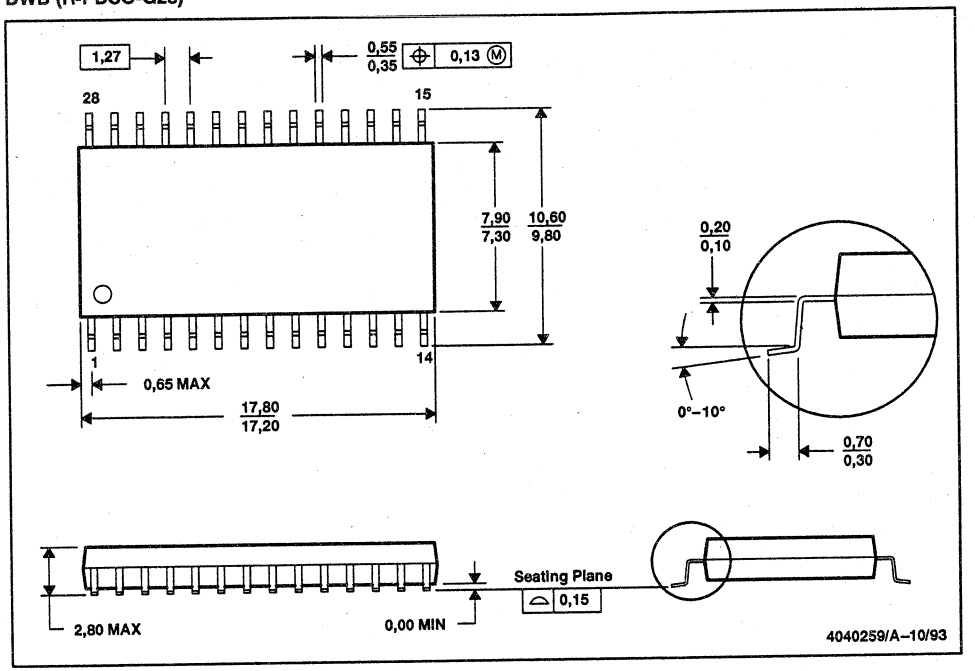
P	S	W	L	L1	L2
1.27	9.53	0.76	1.55	0.64	0.91

NOTE A: All linear dimensions are in millimeters.

Figure 11. Land Pattern for PCB Layout

MECHANICAL DATA

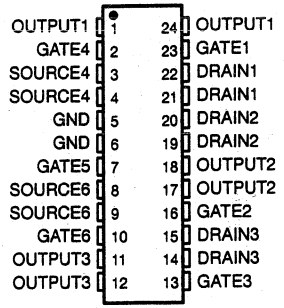
DWB (R-PDSO-G28) **PLASTIC SMALL-OUTLINE PACKAGE (SOP)**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

- Low $r_{DS(on)}$ . . . 0.23 Ω Typ
- High Voltage Output . . . 60 V
- Extended ESD Capability . . . 4000 V
- Pulsed Current . . . 11.25 A Per Channel
- Fast Commutation Speed

DW PACKAGE
(TOP VIEW)

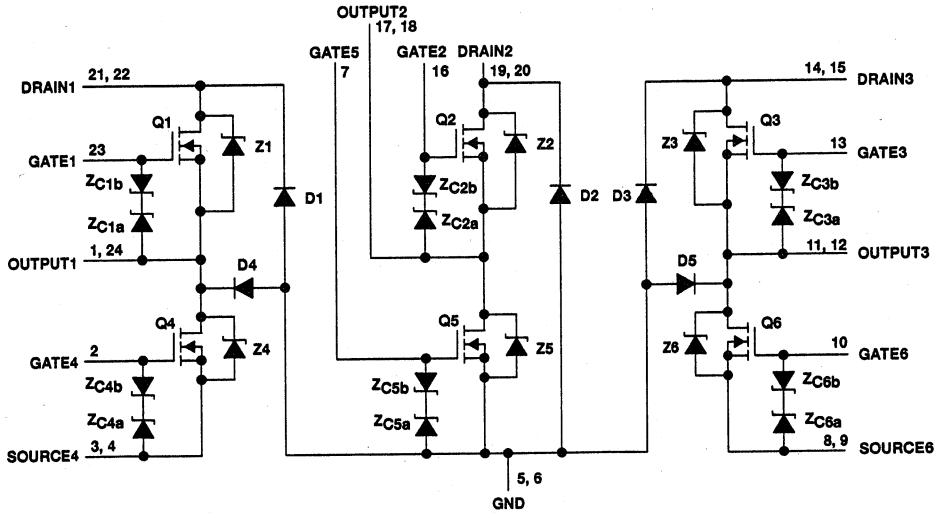


description

The TPIC1301 is a monolithic gate-protected power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors configured as three half H-bridges. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC1301 is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



NOTE: For correct operation, no terminal pin may be taken below GND.

TEXAS INSTRUMENTS

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-GND voltage, V_{DG}	100 V
Drain-to-source voltage, V_{DS}	60 V
Output-to-GND voltage	60 V
SOURCE4, SOURCE6-to-GND voltage	60 V
Gate-to-source voltage range, V_{GS}	−9 V to 18 V
Continuous drain current, each output, T_C = 25°C	2.25 A
Continuous source-to-drain diode current, T_C = 25°C	2.25 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	11.25 A
Continuous gate-to-source zener-diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pule avalanche energy, E_{AS}, T_C = 25°C (see Figures 4, 15, and 16)	17.2 mJ
Continuous total dissipation, T_C = 25°C (see Figure 15)	1.39 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	V_{DS} = V_{GS},	1.5	1.75	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1–D5)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 2.25 A, See Notes 2 and 3	V_{GS} = 10 V,		0.52	0.62	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 2.25 A, V_{GS} = 0 (Z1–Z6), See Notes 2 and 3 and Figure 12			1	1.2	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 2.25 A (D1–D5) See Notes 2 and 3			5		V
I_{DSS}	Drain current-gate shorted to source	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V,	V_{DS} = 0		20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND Gate shorted to source	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 2.25 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.23	0.275	Ω
			T_C = 125°C		0.35	0.4	
g_{fs}	Forward transconductance	V_{DS} = 15 V, See Notes 2 and 3 and Figure 9	I_D = 1.125 A,	1.6	2.21		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz,	V_{GS} = 0, See Figure 11		200	250	pF
C_{oss}	Short-circuit output capacitance, common source				175	220	
C_{rss}	Short-circuit reverse transfer capacitance, common source				40	75	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 1.125 A, V_{GS} = 0, See Figures 1 and 14	V_{DS} = 48 V, di/dt = 100 A/µs,	Z1, Z2, and Z3		50		ns
Q_{RR}	Total diode charge					65		nC

resistive-load switching characteristics, T_C = 25°C

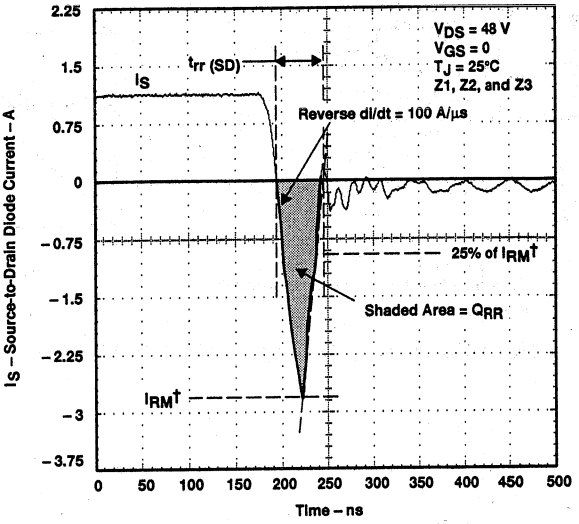
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 20 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		25	50	ns
$t_{d(off)}$	Turn-off delay time			25	50	
t_r	Rise time			15	30	
t_f	Fall time			7	15	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1.125 A, V_{GS} = 10 V, See Figure 3		6.2	7.4	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.7	0.8	
Q_{gd}	Gate-to-drain charge			2.4	2.9	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		90		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		45		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		28		°C/W

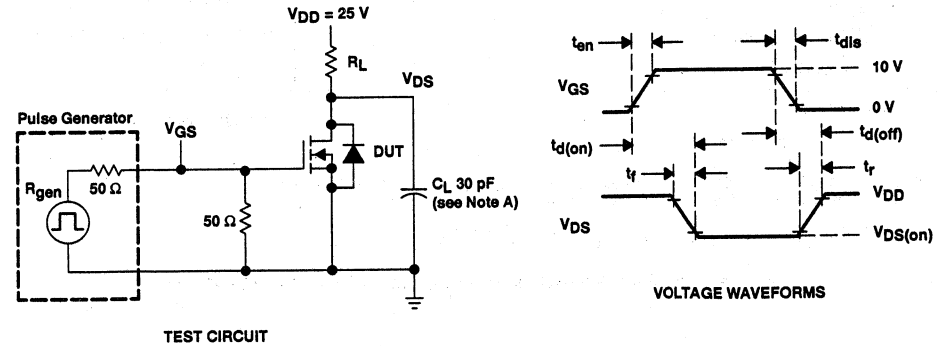
NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted on a 24 in^2, 4-layer FR4 printed-circuit board.
6. Package mounted in intimate contact with infinite heatsink.
7. All outputs with equal power

PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

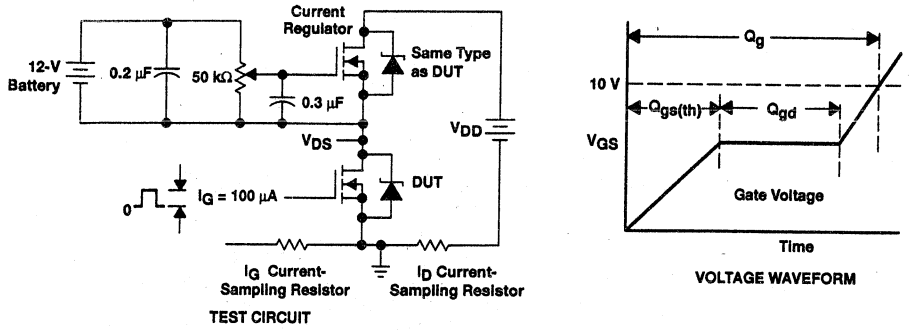
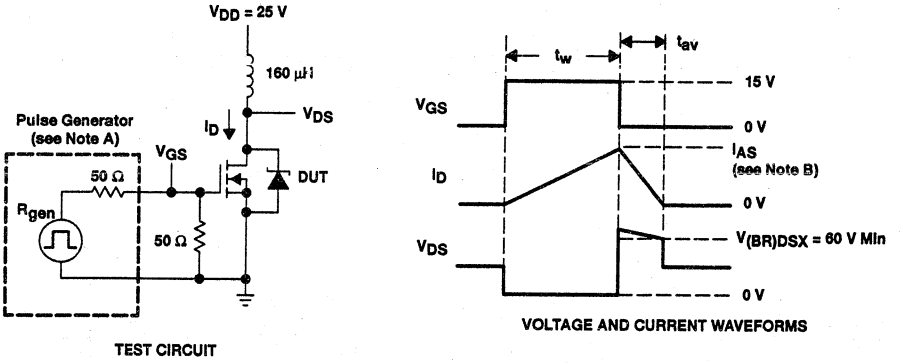


Figure 3. Gate-Charge Test Circuit and Voltage Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 11.25$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 17.2$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

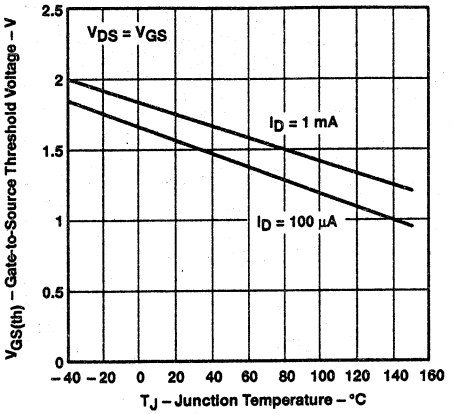


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

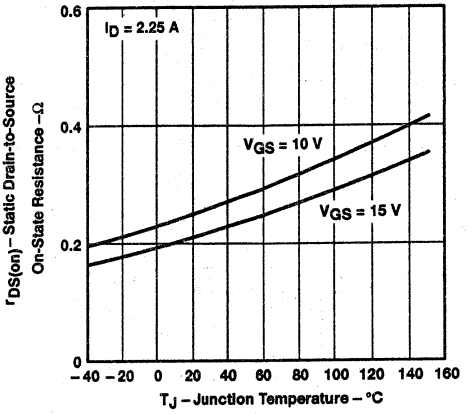


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

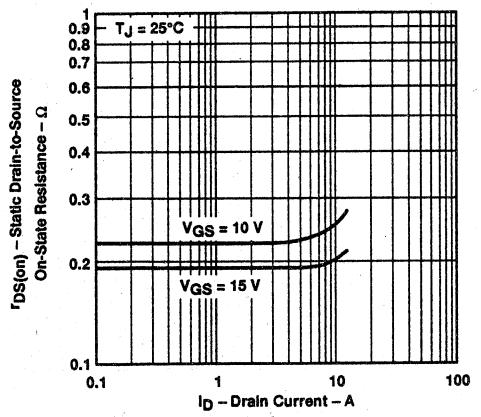


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

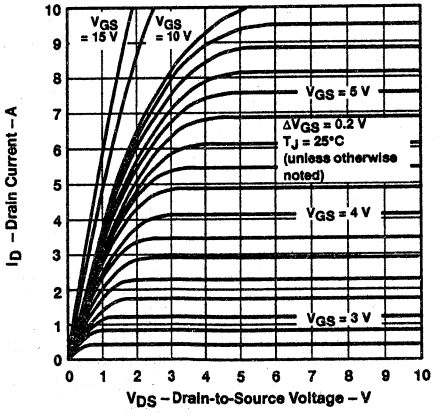


Figure 8

TYPICAL CHARACTERISTICS

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

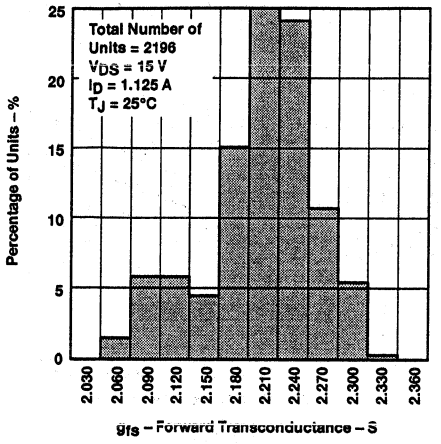


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

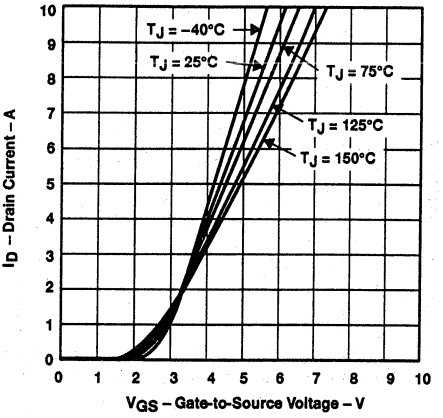


Figure 10

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

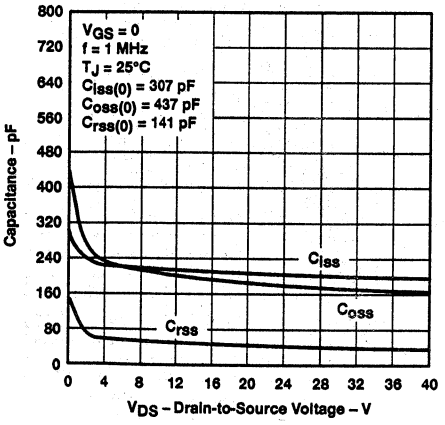


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

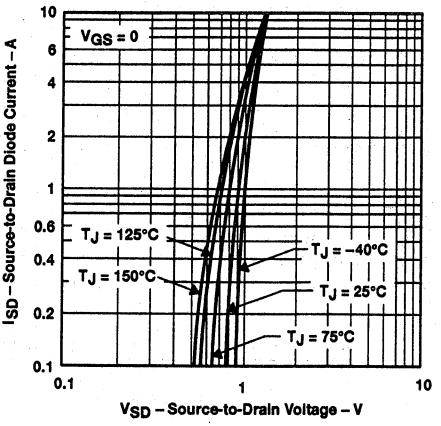


Figure 12

TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

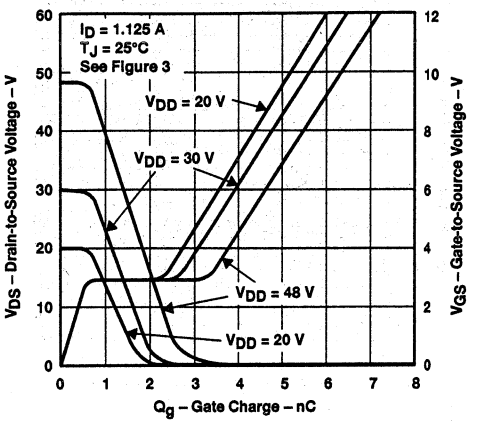


Figure 13

REVERSE RECOVERY TIME
vs
REVERSE dI/dt

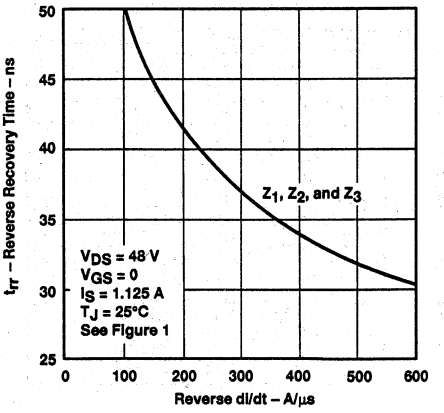
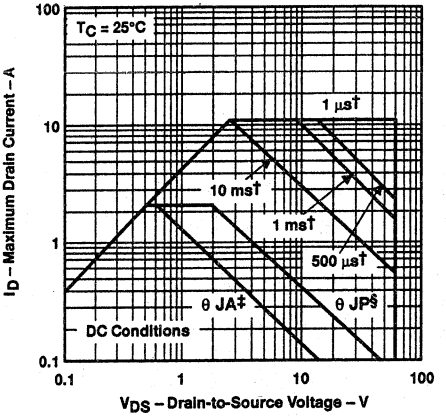


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle
‡ Device mounted on FR4 printed-circuit board with no heatsink.
§ Device mounted in intimate contact with infinite heatsink.

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

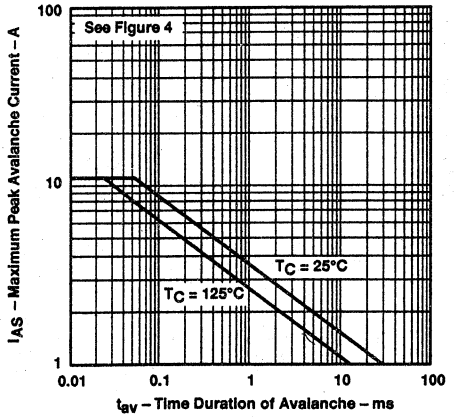
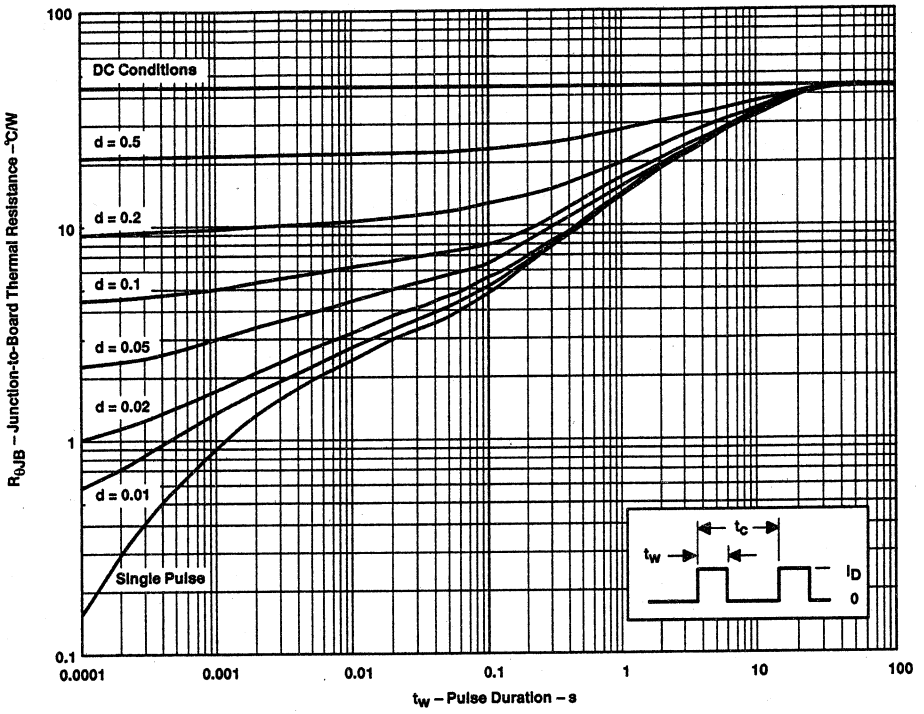


Figure 16

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink

NOTE A: $Z_{\theta B}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_c = cycle time
d = duty cycle = t_W/t_c

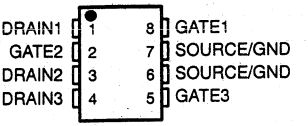
Figure 17

3-CHANNEL COMMON-SOURCE LOGIC-LEVEL POWER DMOS ARRAY

SLIS036A – JUNE 1994 – REVISED OCTOBER 1994

- Low $r_{DS(on)}$ . . . 0.6 Ω Typ
- High-Voltage Outputs . . . 60 V
- Pulsed Current . . . 2.25 A Per Channel
- Fast Commutation Speed
- Direct Logic-Level Interface

D PACKAGE
(TOP VIEW)

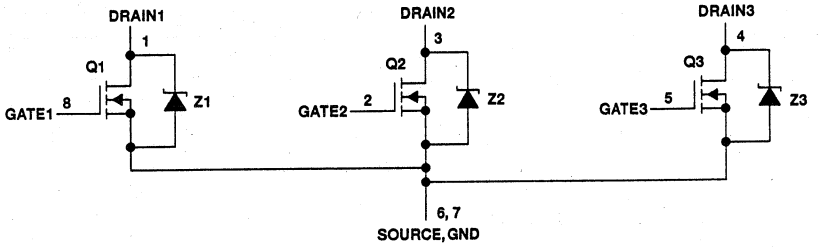


description

The TPIC2322L is a monolithic logic-level power DMOS array that consists of three electrically isolated N-channel enhancement-mode DMOS transistors configured with a common source and open drains.

The TPIC2322L is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of −40°C to 125°C.

schematic diagram



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Gate-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	0.75 A
Continuous source-to-drain diode current, T_C = 25°C	0.75 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	2.25 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	19 mJ
Continuous total power dissipation at (or below) T_C = 25°C (see Figure 15)	0.95 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

TEXAS INSTRUMENTS

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	V_{DS} = V_{GS},	1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain to GND breakdown voltage	Drain to GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 0.75 A, See Notes 2 and 3	V_{GS} = 5 V,		0.45	0.53	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 0.75 A, See Notes 2 and 3 and Figure 12	V_{GS} = 0		0.85	1	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V,	V_{DS} = 0		10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 0.75 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.6	0.7	Ω
			T_C = 125°C		0.94	1	
g_{fs}	Forward transconductance	V_{DS} = 15 V, See Notes 2 and 3 and Figure 9	I_D = 0.5 A,	0.75	0.9		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz,	V_{GS} = 0, See Figure 11		115	145	pF
C_{oss}	Short-circuit output capacitance, common source				60	75	
C_{rss}	Short-circuit reverse transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, T_C = 25°C (see schematic diagram)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_F = 0.375 A, di/dt = 100 A/µs,	V_{DS} = 48 V, See Figures 1 and 14		85		ns
Q_{RR}	Total diode charge				0.19		µC

resistive-load switching characteristics, T_C = 25°C

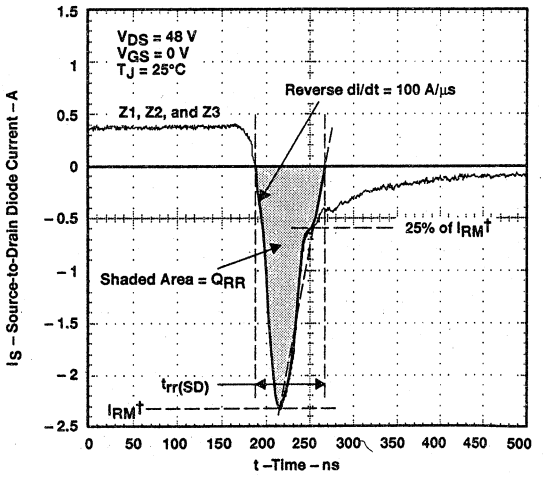
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 67 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		8	16	ns
$t_{d(off)}$	Turn-off delay time			12	24	
t_r	Rise time			14	28	
t_f	Fall time			13	26	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.375 A, V_{GS} = 5 V, See Figure 3		1.8	2.3	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.4	0.5	
Q_{gd}	Gate-to-drain charge			1.1	1.4	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, See Note 4	All outputs with equal power		130		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			44		°C/W

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink.

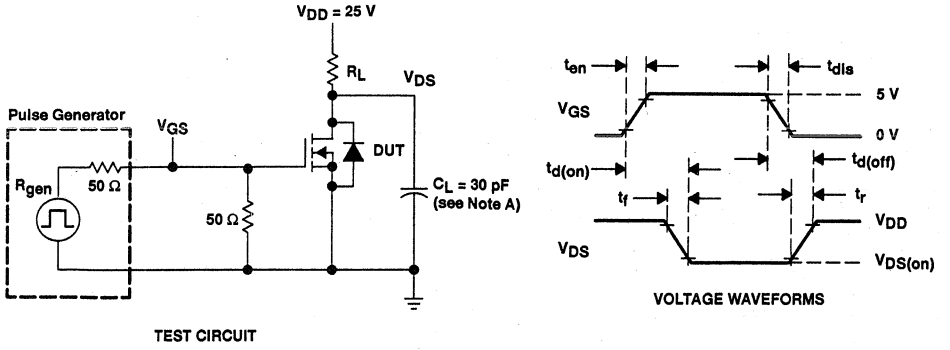
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

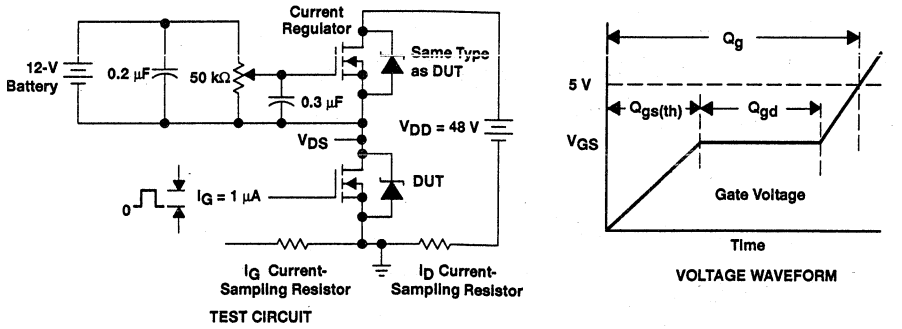
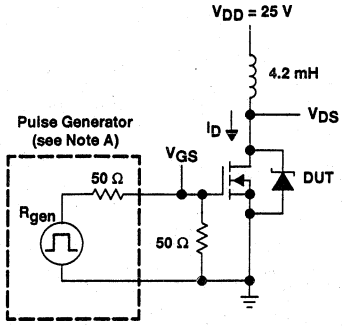
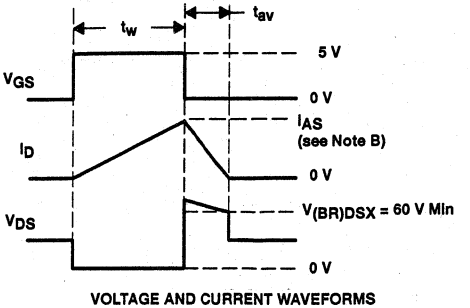


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 2.25$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 19$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

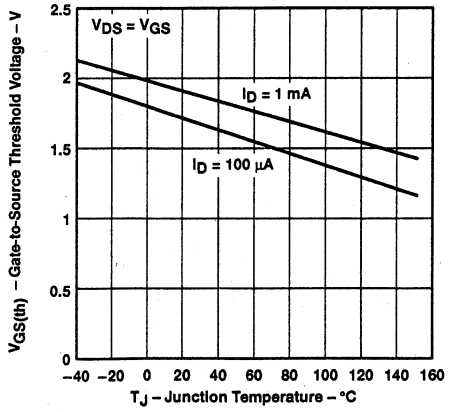


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

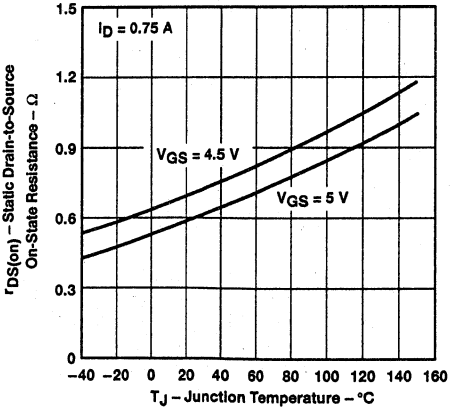


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

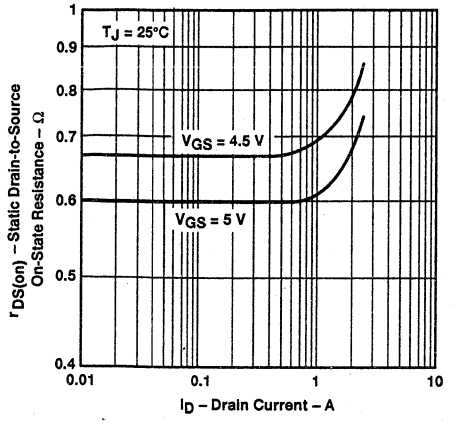


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

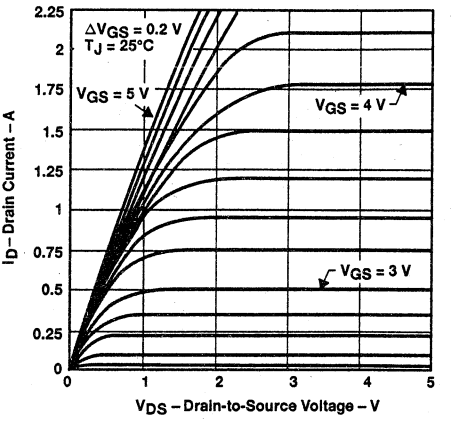


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

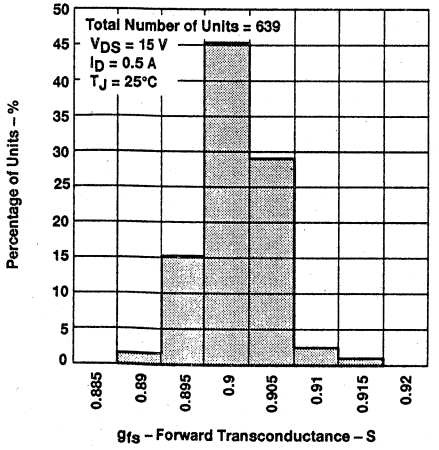


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

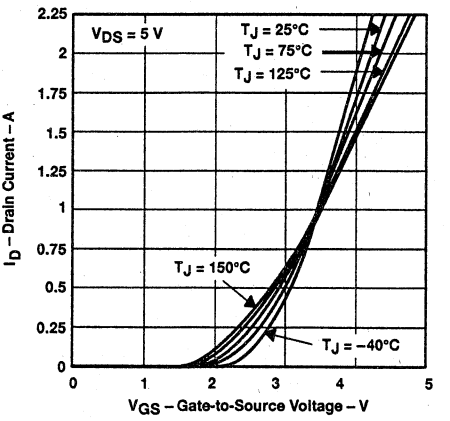


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

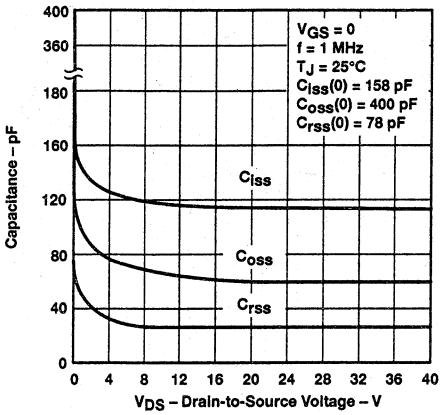


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

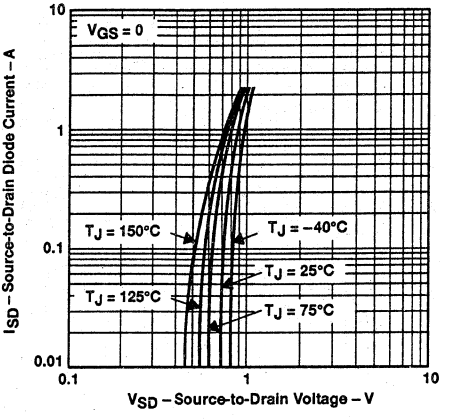


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

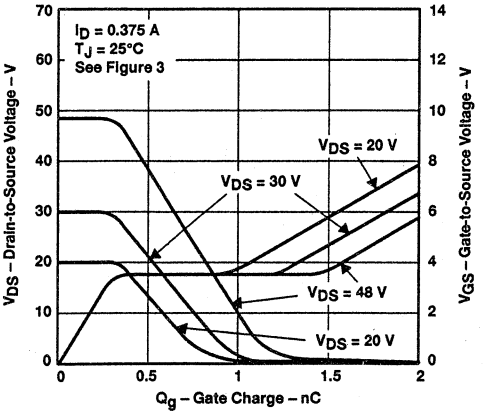


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE dI/dt

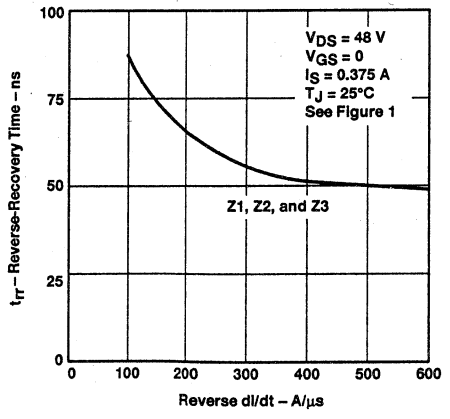
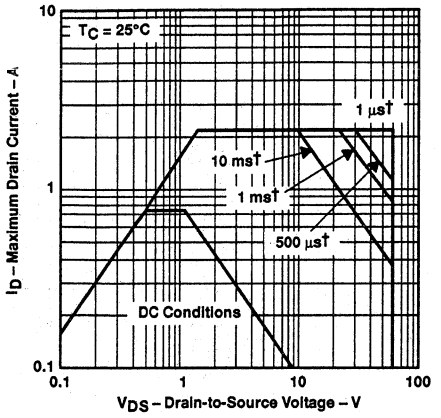


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

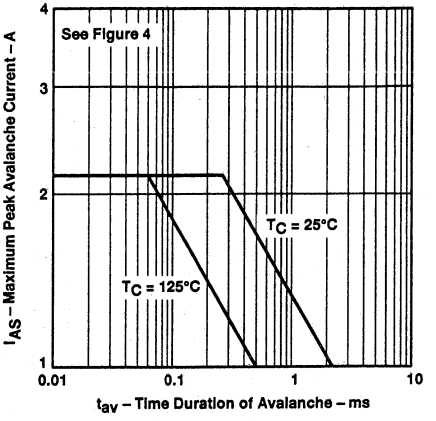
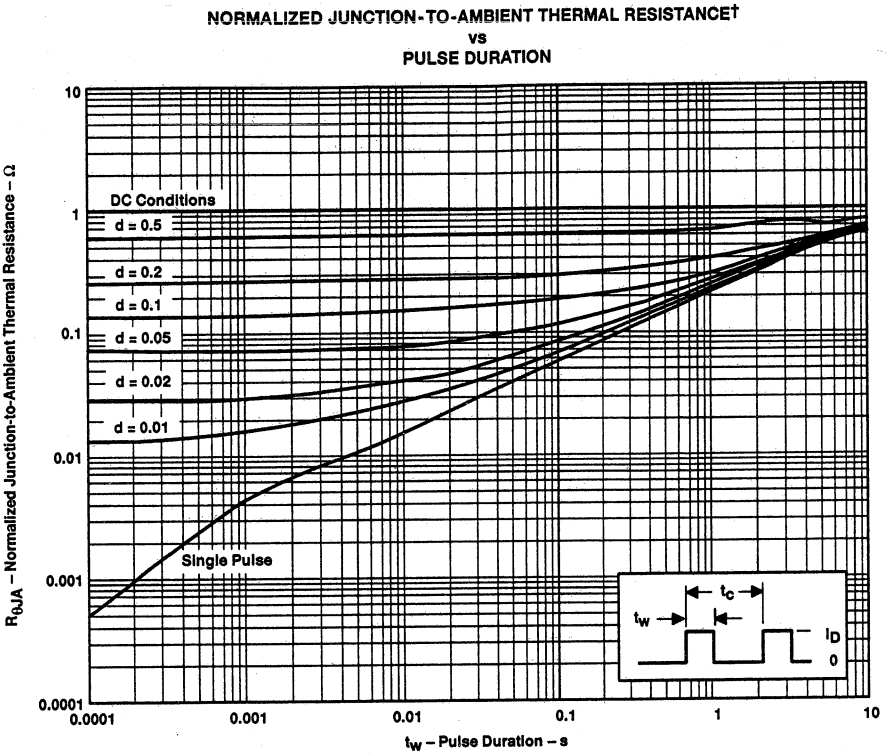


Figure 16

THERMAL INFORMATION



† Device mounted on FR4 printed-circuit board with no heat sink.

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$

t_w = pulse duration

t_c = cycle time

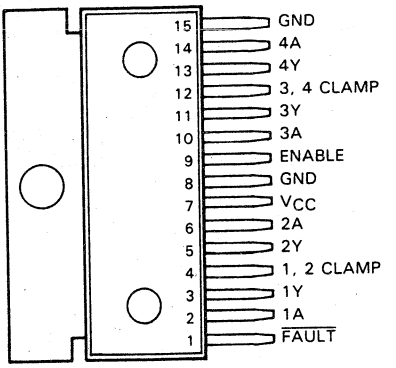
d = duty cycle = t_w/t_c

Figure 17

SLDSØ27 D3299, AUGUST 1989–REVISED JANUARY 1991

- 1-A Current Capability Per Channel
- 45-V Inductive Switching Voltage Capability
- Current Sink Inputs Compatible With TTL or CMOS Devices
- Output Clamp Diodes for Inductive Transient Protection
- Independent Thermal Shutdown Protection
- Overvoltage Shutdown Protection
- Independent Channel Current Limit
- Error Sensing
- Extended Temperature Range of −40°C to 125°C

KN SINGLE-IN-LINE PACKAGE
(TOP VIEW)



The tab is electrically connected to the GND pins.

description

The TPIC2404 is a monolithic high-voltage high-current quadruple low-side switch especially designed for driving from low-level logic to peripheral loads such as relays, solenoids, motors, lamps, and other high-voltage high-current loads. The high-efficiency power switch is optimized for applications where a very rugged power switch is required. The device will tolerate power supply transients and reverse battery conditions up to 13 V.

The TPIC2404 features four inverting open-collector outputs controlled by a common-enable input. When ENABLE is low, the outputs are disabled. An error sensing circuit monitors load and device faults. When an error is sensed, the $\overline{\text{FAULT}}$ output goes to a low state. In addition, the device features on-board V_{CC} overvoltage and thermal overload protection circuits, and the outputs are current-limit protected.

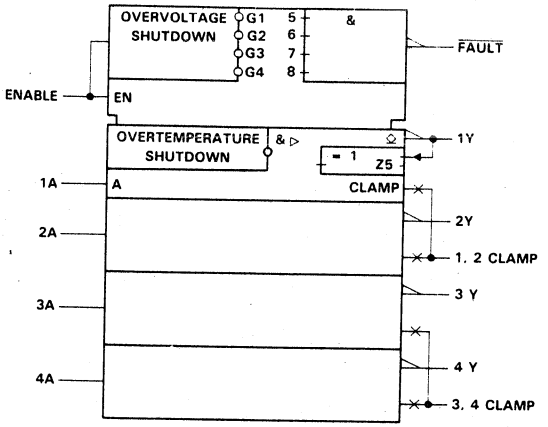
FUNCTION TABLE

	INPUTS		OUTPUTS	
	ENABLE	A	Y	$\overline{\text{FAULT}}$
Normal operation	H	H	L	H
	H	L	H	H
	L	X	H	H
Open load	H	L	L	L
	H	H	L	H
Short to GND	H	L	L	L
	H	H	L	H
Overvoltage shutdown	H	H	H	L
	H	L	H	H
Thermal shutdown	H	H	H	L
	H	L	H	H
Short to V_{CC}	H	H	H	L
	H	L	H	H

H = high level, L = low level, X = irrelevant

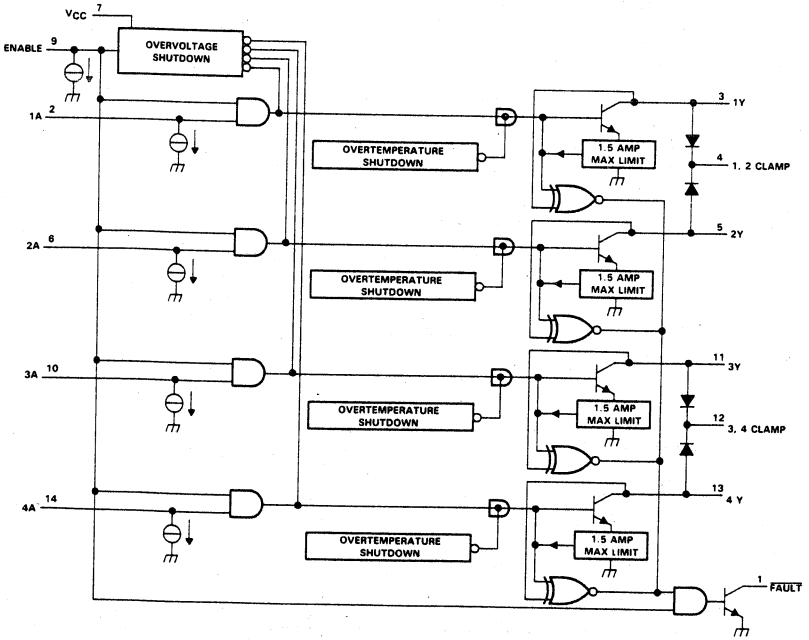
TEXAS INSTRUMENTS

logic symbol†

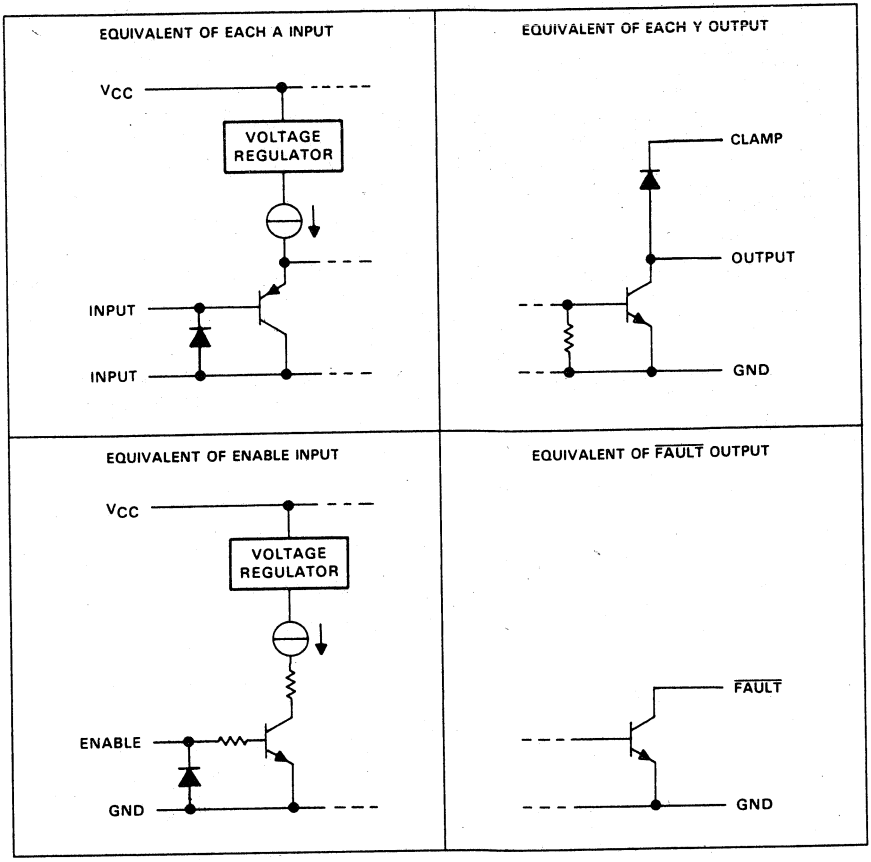


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	−13 V to 24 V
Input voltage range, V_I	−0.6 V to 7 V
Output voltage range, V_O	−0.6 V to 45 V
Output sustaining voltage, $V_{O(sust)}$	45 V
Continuous output sink current (repetitive, t_w < 8 ms), I_{OL} (see Note 2)	1.5 A
Output clamp-diode voltage, V_{OK}	45 V
Continuous total dissipation at (or below) 25°C case temperature (see Note 3)	50 W
Operating case or virtual junction temperature range	−55°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 s	260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Output sink current is limited by the overcurrent limit.
3. For operation above 25°C free-air or case temperature refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

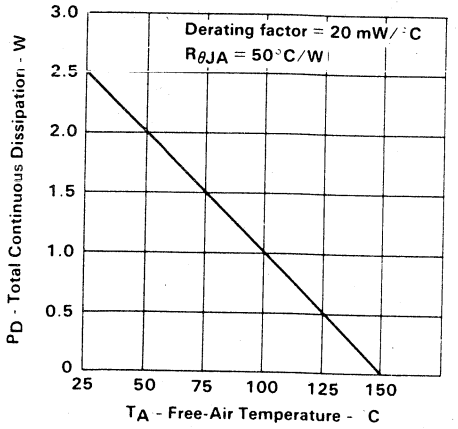


FIGURE 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

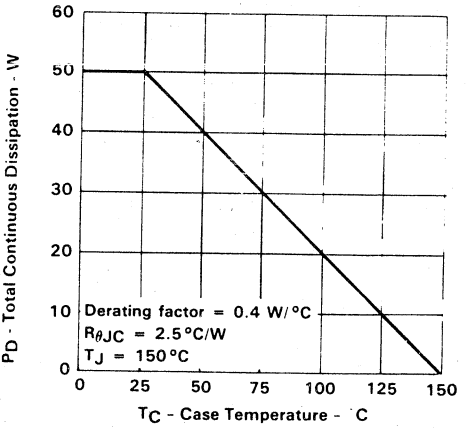


FIGURE 2

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	9	12	16	V
High-level input voltage, V_{IH}	2		5.5	V
Low-level input voltage, V_{IL}	−0.3†		0.8	V
Peak output voltage from external inductive kickback			45	V
Continuous output sink current			1	A
Fault output sink current			75	μA
Operating free-air temperature, T_A	−40		125	°C

† The algebraic convention in which the least positive (most negative) value is designated minimum is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$I_{O(off)}$	Off-state output current		V_O = 12 V, ENABLE low		15	100	μA
			V_O = 45 V, ENABLE high		0.6	2	mA
			V_O = 12 V, ENABLE high	200	400	600	μA
I_{IL}	Low-level input current		V_I = 0 to 0.8 V	−10	25	40	μA
I_{IH}	High-level input current	A inputs		10	25	60	μA
		ENABLE			0.2	1	mA
V_{OL}	Low-level output voltage		I_{OL} = 100 mA		0.1	0.15	V
			I_{OL} = 500 mA		0.3	0.55	
			I_{OL} = 1 A		0.8	1.3	
			$\overline{FAULT}$ output, I_{OL} = 30 μA		0.2	0.4	
I_{OL}	Low-level output current		$\overline{FAULT}$ output, V_{OL} = 1 V to 5.5 V	50	90	125	μA
$I_{R(K)}$	Clamp diode reverse current		V_r = 50 V, V_O = 0			100	μA
$V_{F(K)}$	Clamp diode forward voltage		I_f = 1 A			2	V
			I_f = 1.5 A			2.5	
I_{CC}	Supply current		Outputs off, ENABLE low			0.25	mA
			Outputs on, T_A = −40°C			120	
			Outputs on, T_A = 25° C to 125°C			100	

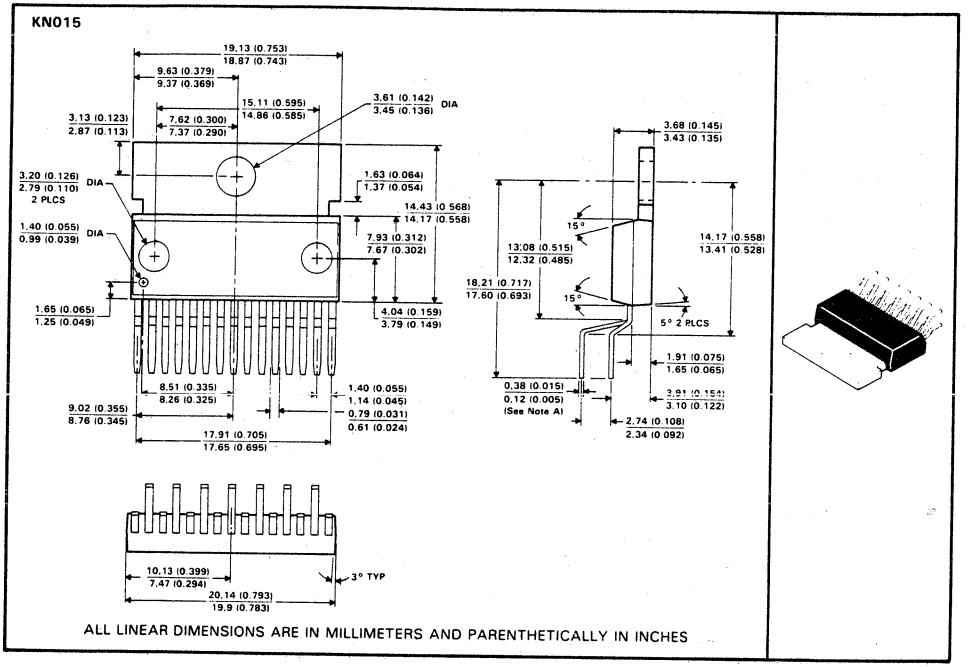
operating characteristics over recommended operating free-air temperature and supply voltages (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
High-level output sense voltage threshold				7	V
Low-level output sense voltage threshold		3			V
Overcurrent limiting	T_A = −40°C			1.85	A
	T_A = 25°C to 125°C		1.2	1.5	
V_{CC} Overvoltage shutdown		25.5		31	V
V_{hys} Overvoltages shutdown hysteresis			0.25		V
Thermal shutdown			155		°C
Thermal shutdown hysteresis			15		°C
Turn-on time			8		μs
Turn-off time			8		μs

‡ All typical values are at V_{CC} = 12 V, T_A = 25 °C.

KN015 plastic flange-mount package

This package comprises a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

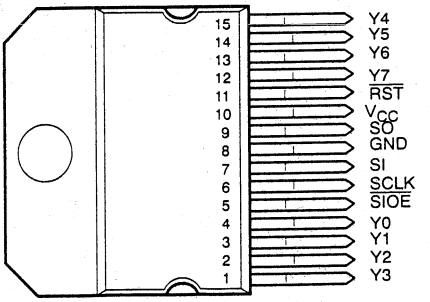


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: This dimension does not apply for solder-dipped leads.

- 8-Bit Serial-In Parallel-Out Driver
- 1-A Output Current Capability Per Channel or 8-A Total Current
- Overcurrent Limiting and Out-of-Saturation Voltage Protection on Driver Outputs
- Contains Eight Open-Collector Saturating Sink Outputs With Low On-State Voltage
- High-Impedance Inputs With Hysteresis Are Compatible With TTL or CMOS Levels
- Exceptionally Low On-State Supply Current 50 mA
- Very Low Standby Power . . . 20 mW Typical
- Status of Output Drivers May Be Monitored at Serial Output
- 3-State Serial Output Permits Serial Cascading or Wire-AND Device Connections
- 45-V Transient Clamping With Inductive Switching on Outputs, 20-mJ Rating Per Driver Output

KV PACKAGE
(TOP VIEW)



The tab is electrically connected to GND.

description

The TPIC2802 octal intelligent-power switch is a monolithic BIDFET† integrated circuit designed to sink currents up to 1 A at 45 V simultaneously at each of eight driver outputs under serial input data control. Furthermore, use of a Darlington output structure enables an 80% reduction in the on-state supply current compared with earlier designs. Status of the individual driver outputs is available in serial data format. The driver outputs have overcurrent limiting and out-of-saturation voltage protection features. Applications include driving solenoids, relays, dc motors, lamps, and other medium-current or high-voltage loads.

The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit parallel latch, which independently controls each of the eight Y-output drivers.

Data is entered into the device serially via the serial input (SI) and goes directly into the lowest bit (0) of the shift register. Using proper timing signals, the input data is passed to the corresponding output latch and output driver. A logic-high SI bit n turns the corresponding output driver (Y_n)off. A logic-low bit at SI turns the corresponding output driver on. Serial data is transferred into SI on the high-to-low transition of the serial clock (SCLK) input in 8-bit bytes with data for the Y7 output (most significant bit) first and data for Y0 output (least significant bit) last. Both SI and SCLK are active when the serial input-output enable ($\overline{SIOE}$) input is low and are disabled when $\overline{SIOE}$ is high.

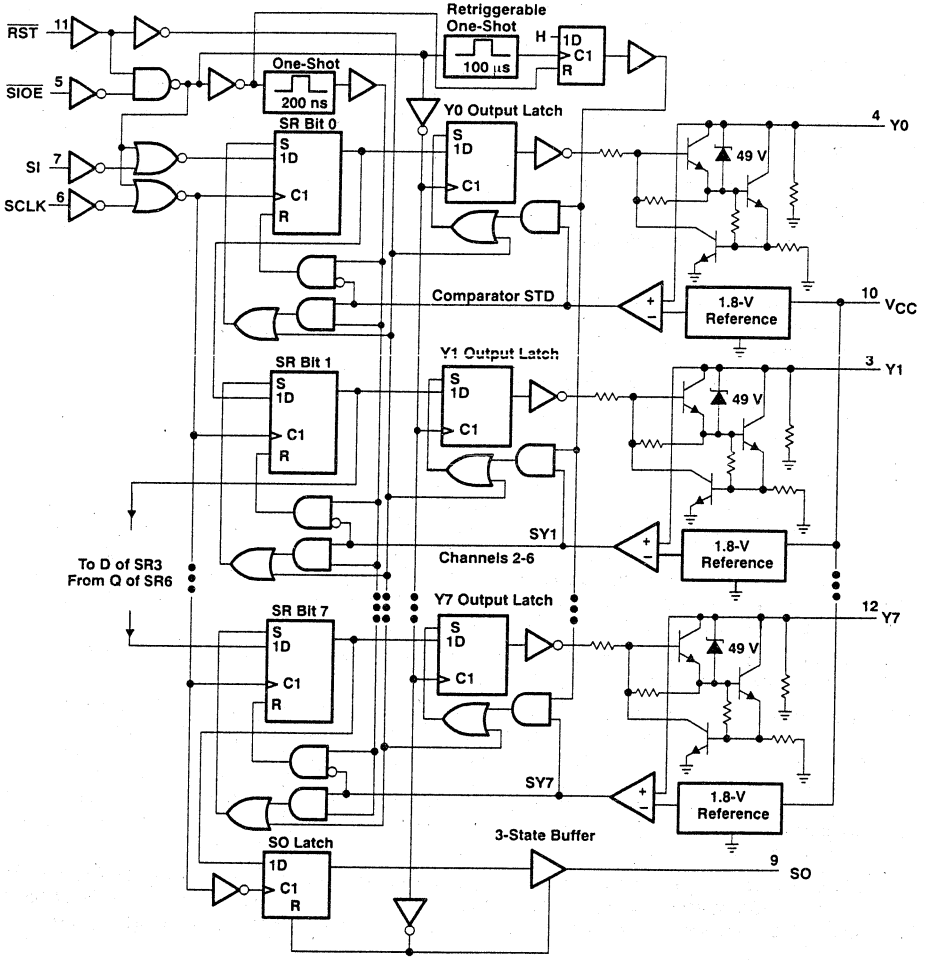
Each driver output is monitored by a voltage comparator that compares the Y-output voltage level with an internal out-of-saturation threshold voltage reference level. The logic state of the comparator output is dependent upon whether the Y output is greater or smaller than the reference voltage level. While $\overline{SIOE}$ is held high, an activated

†BIDFET – Bipolar double-diffused, N-channel and P-channel MOS transistors are on the same chip-patented process.

description (continued)

driver output will be unlatched and turned off when the output voltage exceeds the out-of-saturation threshold voltage level except when the internal unlatch enable is low and disabled. The high-to-low transition of $\overline{SIOE}$ transfers the logic state of the comparator output to the shift register.

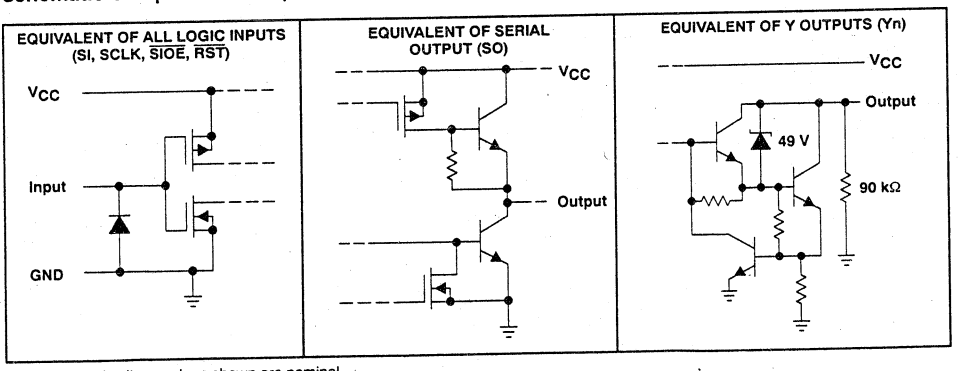
functional block diagram



Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
GND	8		Ground. Common return for entire chip. The output current from this pin is potentially as high as 8 A if all outputs are on. This ground is used for both logic and power circuits.
$\overline{RST}$	11	I	Reset. An asynchronous reset is provided for the shift register and the parallel latches. This pin is active when low and has no internal pullup. When active, it causes the power outputs to turn off. A power-on clear can be implemented using an RC network to V_{CC}.
SCLK	6	I	Serial clock. This pin clocks the shift register. The serial output (SO) changes state on the rising edge of this clock and serial input (SI) data is accepted on the falling edge.
SI	7	I	Serial Input. A high on this pin programs a particular output to be off and a low turns it on.
$\overline{SIOE}$	5	I	Serial input-output enable. Data is transferred from the shift registers to the power outputs on the rising edge of this signal. The falling edge of this signal parallel loads the output voltage sense bits from the power output stages into the shift register. The output driver SO is enabled when this pin is low, provided $\overline{RST}$ is high.
SO	9	O	Serial output. This pin is the serial 3-state output from the shift register and is in a high-impedance state when $\overline{SIOE}$ is high or $\overline{RST}$ is low. A high for a data bit on this pin indicates that the corresponding power output (Y_n) is high. This could mean that the output was programmed to be off the last time a byte was input to the device or that the output faulted and was latched off by the output voltage sense indicator. A low on this pin for a data bit indicates that the corresponding power output (Y_n) is low (an on output stage or open-circuit condition).
V_{CC}	10		5-V supply voltage
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	4 3 2 1 15 14 13 12	O	Power outputs. These outputs are provided with current limiting and voltage sense for fault indication and protection. The nominal load current for these outputs is 500 mA, and the current limiting is set to a minimum of 1 A. The active-low outputs also have voltage clamps set at about 45 V for recirculation of inductive load current. Internal 90-kΩ pulldown resistors are provided at each output. These resistors hold the output low during an open-circuit condition.

schematic of inputs and outputs



All resistor and voltage values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... –0.3 V to 7 V
Input voltage, V_I ..... 7 V
Output voltage range, SO ..... –0.3 V to 7 V
Input current, I_I ..... –15 mA
Peak output sink current at Y, I_O repetitive, t_w = 10 ms, duty cycle = 50%,
(see Notes 2 and 3) ..... Internally limited
Continuous output current at Y, I_O (see Note 3) ..... 1 A
Peak current through GND terminal: Nonrepetitive t_w = 0.2 ms ..... –8 A
Repetitive t_w = 10 ms, duty cycle = 50% ..... –6 A
Continuous current through GND terminal ..... –4.5 A
Single-pulse avalanche energy rating, E_{AS} (see Note 4) ..... 20 mJ
Avalanche current, $I_{AS(max)}$ (see Note 5) ..... 1 A
Continuous dissipation at (or below) T_A = 25°C (see Note 6) ..... 3.575 W
Continuous dissipation at (or below) T_C = 75°C (see Note 6) ..... 25 W
Operating case or virtual-junction temperature range ..... –55°C to 150°C
Storage temperature range ..... –65°C to 150°C
Lead temperature 1, 6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Each Y output is individually current limited with a typical overcurrent limit of about 1.8 A.
3. Multiple Y outputs of this device may conduct rated current simultaneously; however, power dissipation (average) over a short time interval must fall within the continuous dissipation range and the GND terminal current range.
4. V_{DD} = 20 V, starting T_J = 25°C, L = 310 mH, I_{AS} = 0.28 A.
5. V_{DD} = 10 V, starting T_J = 25°C, L = 8 mH, I_{AS} = 1 A, (see Figure 6).
6. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. To avoid exceeding the maximum virtual-junction temperature, these ratings must not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	0.75 V_{CC}		5.25	V
Low-level input voltage, V_{IL}	–0.3		0.2 V_{CC}	V
Output voltage, $V_{O(off)}$			45	V
Continuous output current, $I_{O(on)}$			1	A
Operating case temperature, T_C	–40	25	105	°C

electrical characteristics over recommended operating virtual junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current	All outputs on,	I_O = 0.5 A at all outputs			50	mA
		All outputs off,	T_J = 25°C		4	10	

electrical characteristics over recommended operating virtual junction temperature range (unless otherwise noted) (continued)

driver array outputs (Y0 to Y7)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OK}	Output clamp voltage	I_O = 0.5 A, Output programmed off and current shunted to ground		45	49		V
$V_{O(on)}$	On-state output voltage	With one output programmed on and conducting	I_{OL} = 0.175 A			1	V
			I_{OL} = 0.5 A		1	1.3	V
			I_{OL} = 0.75 A		1.2	1.5	V
			I_{OL} = 1 A, During unlatch disable		1.4	1.6	V
V_{TOS}	Out-of-saturation threshold voltage	With output programmed on and an overcurrent fault condition		1.6	1.8	2.1	V
$I_{O(off)}$	Off-state output current	V_O = 24 V with output programmed off				600	μA
$I_{O(cl)}$	Output current limit	V_O = 3 V with output programmed on		1	1.8		A
	Internal output pulldown resistor			40	90		kΩ

shift register (Inputs SI, $\overline{SCLK}$, SCLK, and $\overline{RST}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{T+}	Positive-going threshold voltage			0.75V_{CC}	V
V_{T-}	Negative-going threshold voltage		0.1 V_{CC}		V
V_{hys}	Hysteresis voltage ($V_{T+} - V_{T-}$)		0.85	2.5	V
I_I	Input current	V_I = 0 to V_{CC}		±10	μA
C_i	Input capacitance	V_I = 0 to V_{CC}		20	pF

shift register (output SO)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OL}	Low-level output voltage	I_O = 1.6 mA			0.2	0.4	V
V_{OH}	High-level output voltage	I_O = – 0.8 mA		V_{CC} –1.3			V
I_O	Output current	V_O = 0 to V_{CC},	$\overline{SIOE}$ input high			±20	μA
C_O	Output capacitance	V_O = 0 to V_{CC},	$\overline{SIOE}$ input high			20	pF

† All typical values are at V_{CC} = 5 V, T_J = 25°C.

timing requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, SCLK	See Note 7	0	1	MHz
$t_{w(SCLKH)}$	Pulse duration, SCLK high		410		ns
$t_{w(SCLKL)}$	Pulse duration, SCLK low		410		ns
$t_{w(RST)}$	Pulse duration, $\overline{RST}$ low		1200		ns
t_{su1}	Setup time, $\overline{SIOE}$↓ before SCLK↑		1		μs
t_{su2}	Setup time, SCLK↓ before $\overline{SIOE}$↑		1		μs
t_{su3}	Setup time, SI high before SCLK↓		150		ns
t_{h1}	Hold time, SI low after SCLK↓		150		ns
t_r	Rise time, SCLK, SI, $\overline{SIOE}$			90	ns
t_f	Fall time, SCLK, SI, $\overline{SIOE}$			90	ns

NOTE 7: For cascaded operation, the clock pulse durations [t_w (SCLKL) and t_w (SCLKH)] must be a minimum of 700 ns (giving a maximum clock frequency of 632 kHz).

thermal characteristics

PARAMETER		MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case temperature		3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient temperature		35	°C/W

switching characteristics

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{en}	Enable time	$\overline{SIOE}\downarrow$	SO	C_L = 20 pF, R_L = 1 kΩ, See Figure 2		1000	ns
t_{dis}	Disable time	$\overline{SIOE}\uparrow$	SO	C_L = 20 pF, R_L = 1 kΩ, See Figure 2		1000	ns
t_{d1}	Delay time, valid data	SCLK↑	SO	C_L = 200 pF, See Figure 3		550	ns
t_{d2}	Delay time, unlatch disable	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 5 Ω, See Figure 4	75	450	µs
$t_{r(so)}$	Rise time		SO	C_L = 200 pF, See Figure 3		150	ns
$t_{f(so)}$	Fall time		SO	C_L = 200 pF, See Figure 3		150	ns
$t_{d(on)}$	Delay time, turn on	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 28 Ω, I_{OL} = 500 mA, See Figure 5		10	µs
$t_{d(off)}$	Delay time, turn off	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 28 Ω, I_{OL} = 500 mA, See Figure 5		10	µs
t_v	Valid time, SO output data remains valid after SCLK high	SCLK↑	SO	C_L = 200 pF, See Figure 3	0		ns

PARAMETER MEASUREMENT INFORMATION

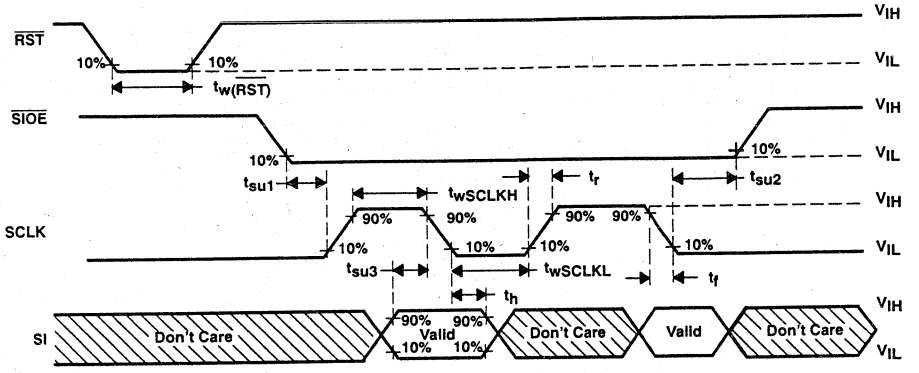
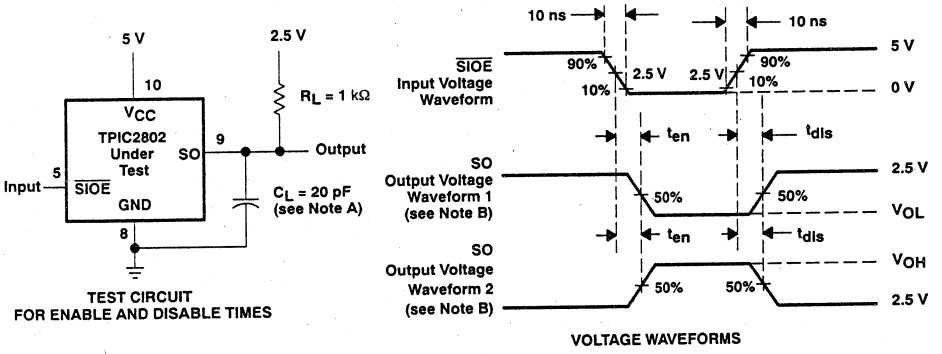


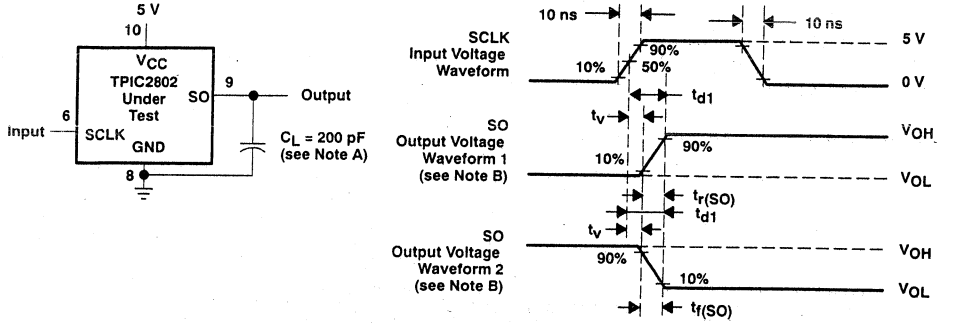
Figure 1. Input Timing Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control when $\overline{SIOE}$ is high.

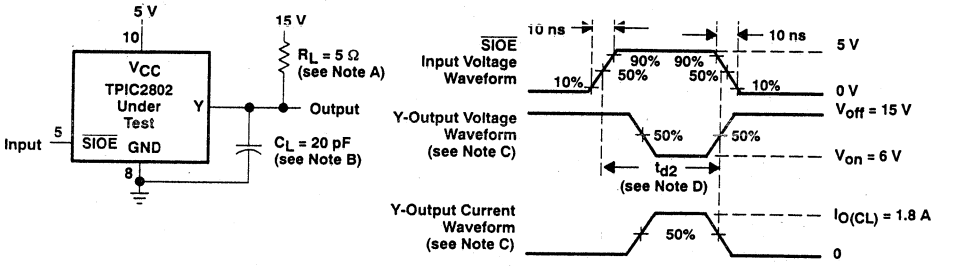
Figure 2. Voltage Waveforms for Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from high to low.

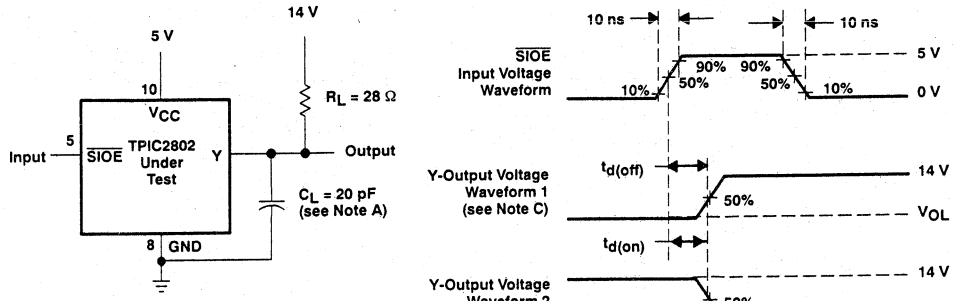
Figure 3. Voltage Waveforms for Delay Times



NOTES: A. Load voltage V_S and load resistance R_L are selected such that on-state voltage at the Y output under test, V_{on} is greater than the maximum out-of-saturation hold voltage, V_{TOS}. Thus $V_{OL} = V_{on} > V_{TOS(max)} = 2.1$ V.
B. C_L includes probe and jig capacitance.
C. Output voltage and current waveforms are for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.
D. t_{d2} = delay until Y-output current goes off under fault condition.

Figure 4. Voltage Waveforms for Unlatch Disable Delay

PARAMETER MEASUREMENT INFORMATION



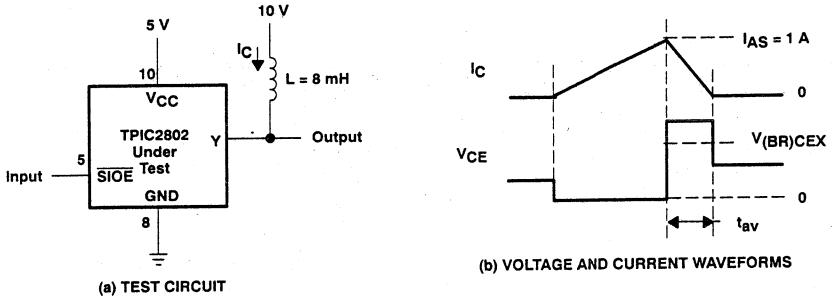
TEST CIRCUIT FOR TURN-OFF $t_{d(off)}$ AND TURN-ON $t_{d(on)}$ DELAY TIMES (see Note B)

NOTES: A. C_L includes probe and jig capacitance.

B. $t_{d(off)} = t_{PLH}, t_{d(on)} = t_{PHL}$

C. Waveform 1 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from on to off. Waveform 2 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

Figure 5. Voltage and Current Waveforms for Turn-Off and Turn-On Delay Times



(a) TEST CIRCUIT

(b) VOLTAGE AND CURRENT WAVEFORMS

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

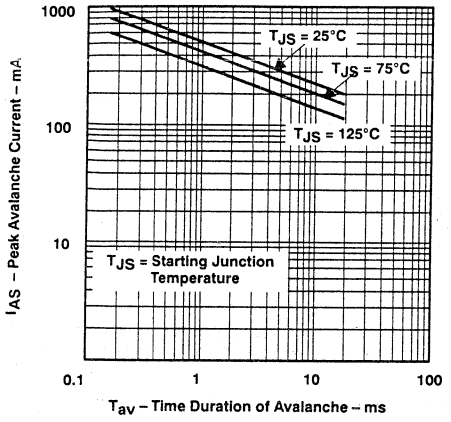


Figure 7

PEAK AVALANCHE CURRENT
vs
JUNCTION TEMPERATURE

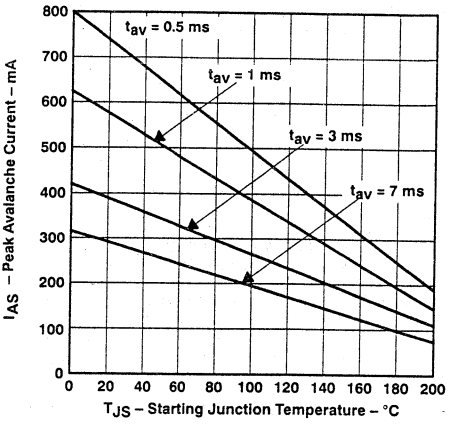


Figure 8

APPLICATION INFORMATION

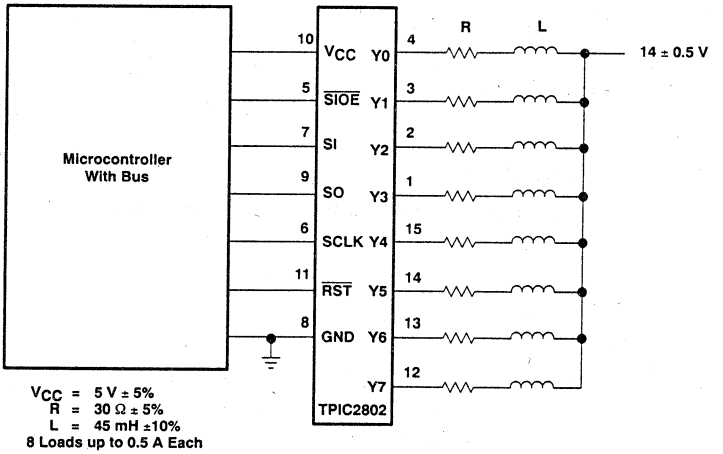


Figure 9. Microcontroller Driving Eight Loads Using a TPIC2802 for Load Interface

PRINCIPLES OF OPERATION

timing data transfer

Figure 10 shows the overall 8-bit data-byte transfer to and from the TPIC2802 interface bus. The logic state of the eight output drivers, Y0 through Y7, is latched into the shift register at time t_0 on the high-to-low transition of $\overline{SIOE}$. Therefore, the SO output data (DY0, DY1 . . .) represents the conditions at the Y-driver outputs at time t_0. The data at the SO output is updated on the low-to-high transition of SCLK.

Input data present at the SI input is clocked into the shift register on the high-to-low transition of SCLK. As shown in Figure 10 on the SI input, input data DI7 is clocked at time t_1, DI6 is clocked at time t_2, etc. Eight SCLK pulses are used to serially load the eight bits of new data into the device. After all the new data is serially loaded, the low-to-high transition of SIOE parallel loads the new data to the eight driver output latches, which in turn directly control the eight Y-driver outputs.

An unlimited amount of data can be shifted through the shift register (into the SI and out the SO), and this allows other devices to be cascaded in a daisy chain with the TPIC2802. Once the last data bit has been shifted into the TPIC2802, the $\overline{SIOE}$ input should be pulled high. The clock (SCLK) input should be low at both transitions of the $\overline{SIOE}$ input to avoid any false clicking of the shift register. The SCLK input is gated by the $\overline{SIOE}$ input, so the SCLK input is ignored whenever $\overline{SIOE}$ is high. At the rising edge of $\overline{SIOE}$, the shift register data is latched into the parallel latch and the output stages will be actuated by the new data. An internal 100-μs delay timer is also started on this rising edge. During the time delay, the outputs will be protected only by the analog current-limiting circuits, since the resetting of the parallel latches by fault conditions will be inhibited during this time period. This allows the device to overcome any high switching currents that can flow during turn-on. Once the delay has ended, the output voltages are sensed by the comparators and any output voltages higher than nominally 1.8 V are latched off.

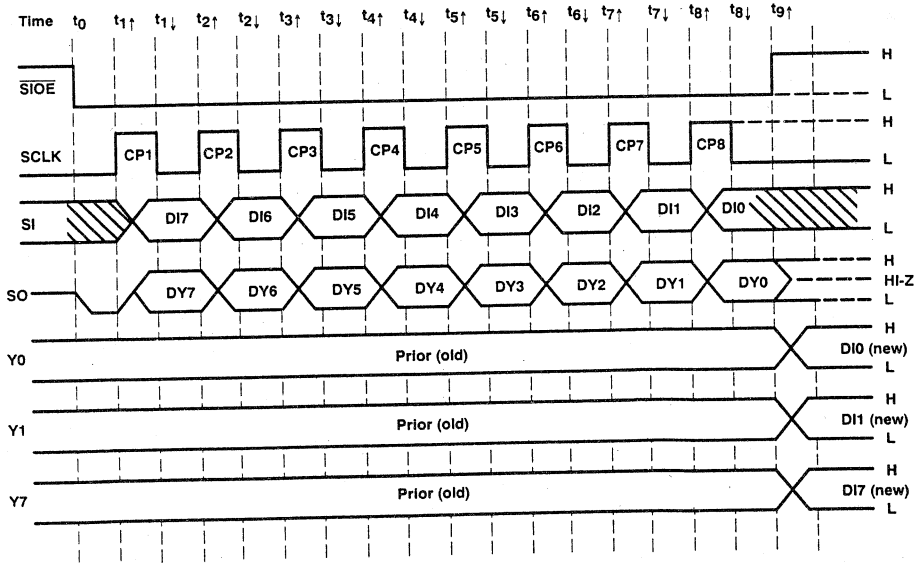


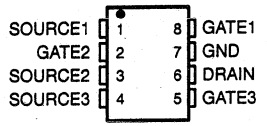
Figure 10. Data-Byte Transfer Timing

fault-conditions check

Open-circuit conditions on any output can be monitored or checked by programming that output off. After a short delay (microseconds), another control byte can be clocked into the device. If the diagnostic bit for that output comes back low, it indicates that the output is low and open circuited. A current overload condition can be detected by programming an output on. After waiting an appropriate length of time, another byte should be clocked into the TPIC2802. The diagnostic bit clocked back from the TPIC2802 in the subsequent data transfer should indicate a low output. If a high returns, a current overload is indicated. A quick overall check can be done by clocking in a test control byte and after a sufficient time delay, clock in another control byte. The diagnostic data is exclusive ORed with the original control byte. If a fault condition exists, a high will result from the subsequent exclusive OR.

- Low $r_{DS(on)}$ . . . 0.6 Ω Typ
- High-Voltage Outputs . . . 60 V
- Pulsed Current . . . 2.25 A Per Channel
- Fast Commutation Speed
- Direct Logic-Level Interface

D PACKAGE
(TOP VIEW)

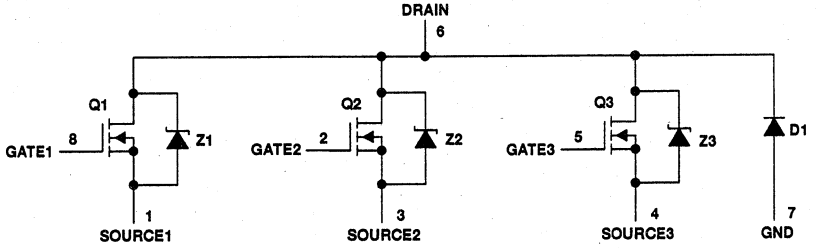


description

The TPIC3322L is a monolithic logic-level power DMOS array that consists of three electrically isolated N-channel enhancement-mode DMOS transistors configured with a common drain and open sources.

The TPIC3322L is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of −40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	0.75 A
Continuous source-to-drain diode current, T_C = 25°C	0.75 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	2.25 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	19 mJ
Continuous total power dissipation at (or below) T_C = 25°C	0.95 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 0.75 A, V_{GS} = 5 V, See Notes 2 and 3			0.45	0.53	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 0.75 A, See Notes 2 and 3			1.8		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 0.75 A, V_{GS} = 0, See Notes 2 and 3 and Figure 12			0.85	1	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 0.75 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.6	0.7	Ω
			T_C = 125°C		0.94	1	
g_{fs}	Forward transconductance	V_{DS} = 10 V, I_D = 0.5 A, See Notes 2 and 3 and Figure 9		0.75	0.9		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0, See Figure 11			115	145	pF
C_{oss}	Short-circuit output capacitance, common source				60	75	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	I_S = 0.375 A, di/dt = 100 A/µs, See Figures 1 and 14 V_{GS} = 0, V_{DS} = 48 V,	Z1, Z2, Z3		30		ns
			D1		85		
Q_{RR}	Total diode charge		Z1, Z2, Z3		0.03		µC
			D1		0.19		

resistive-load switching characteristics, T_C = 25°C

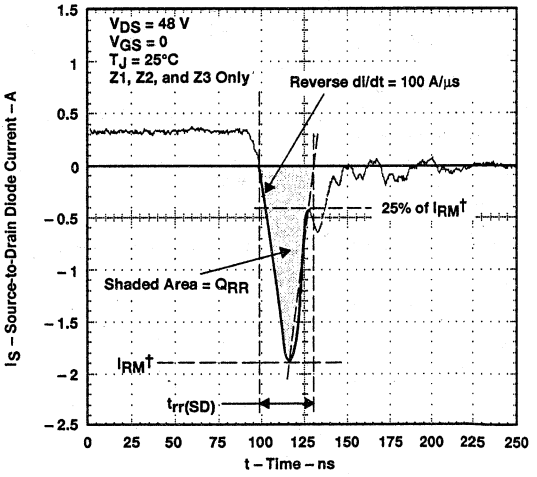
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 67 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		8	16	ns
$t_{d(off)}$	Turn-off delay time			12	24	
t_r	Rise time			14	28	
t_f	Fall time			13	26	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.375 A, V_{GS} = 5 V, See Figure 3		1.8	2.3	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.4	0.5	
Q_{gd}	Gate-to-drain charge			1.1	1.4	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, See Note 4	All outputs with equal power		130		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			44		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

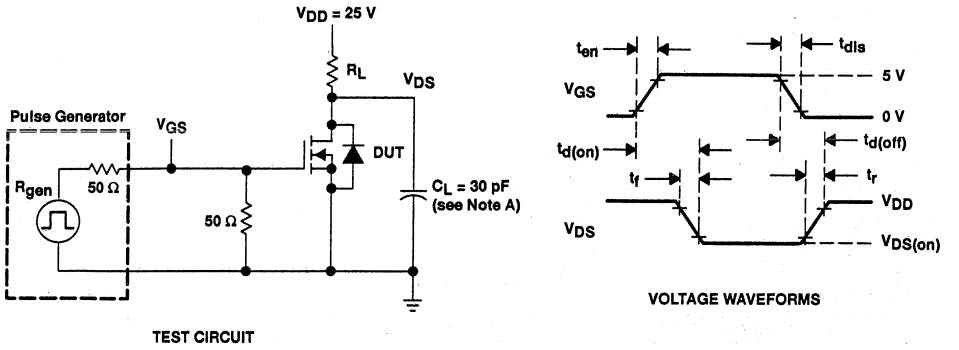
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
NOTE A: The above waveform represents D1 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

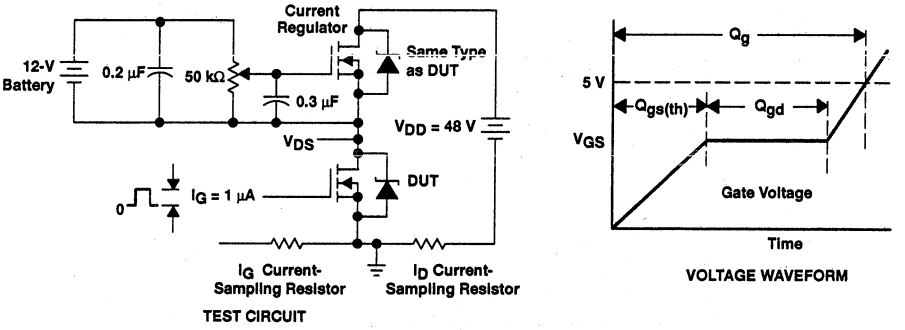
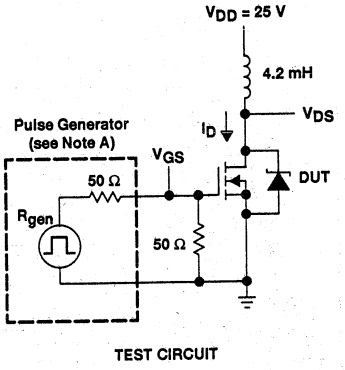
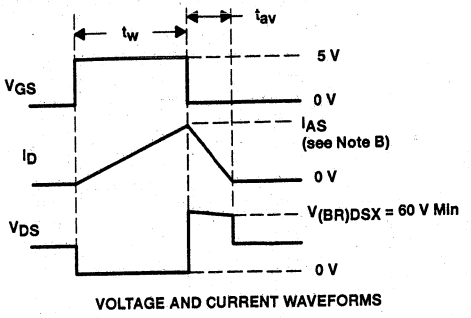


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 2.25$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 19$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

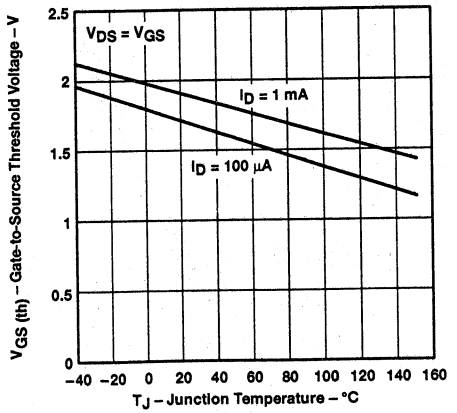


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

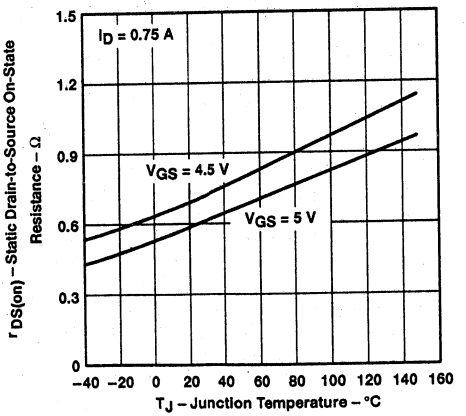


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

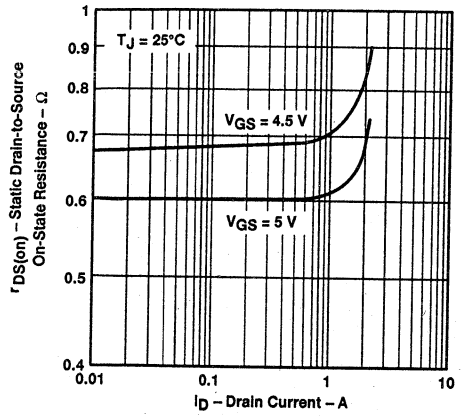


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

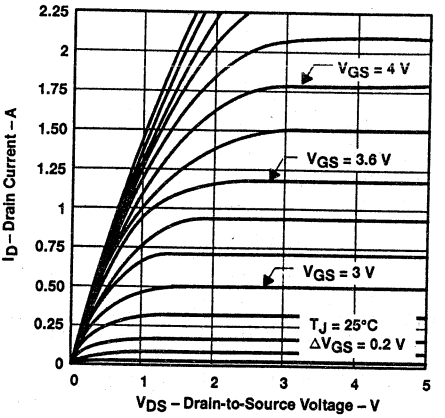


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

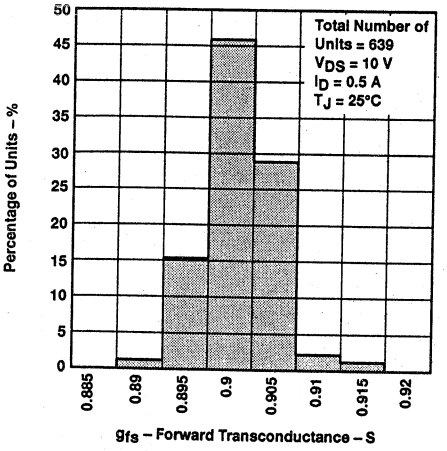


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

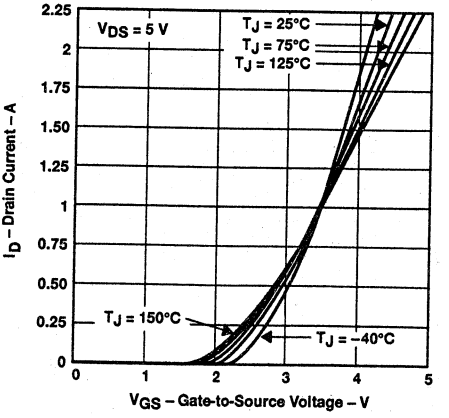


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

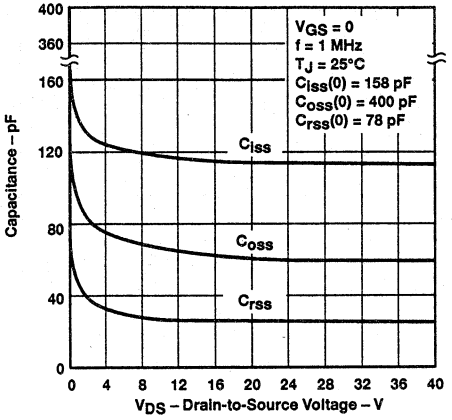


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

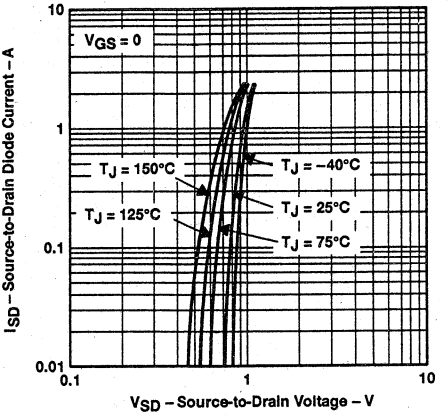


Figure 12

DRAIN-TO-SOURCE AND GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

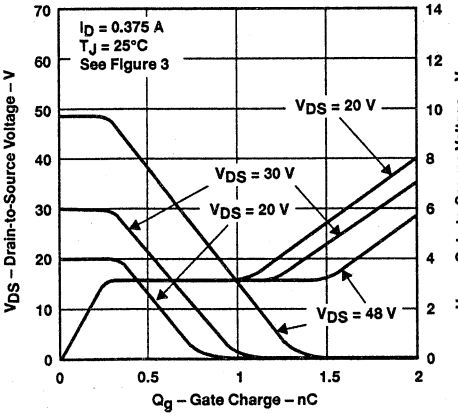


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

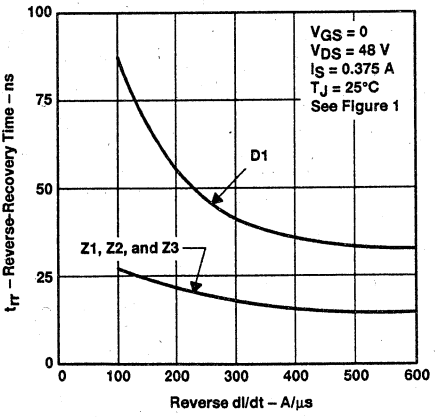
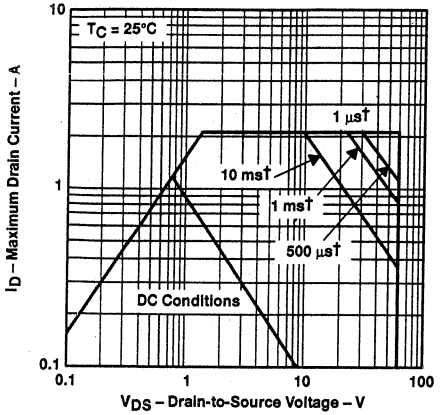


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

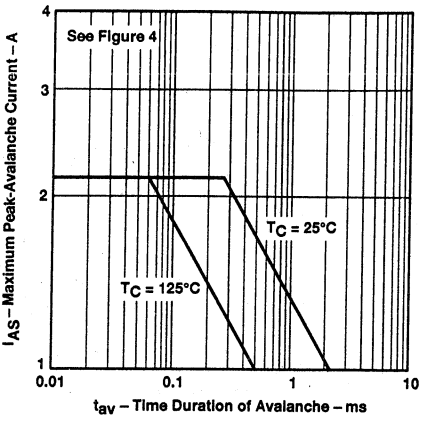
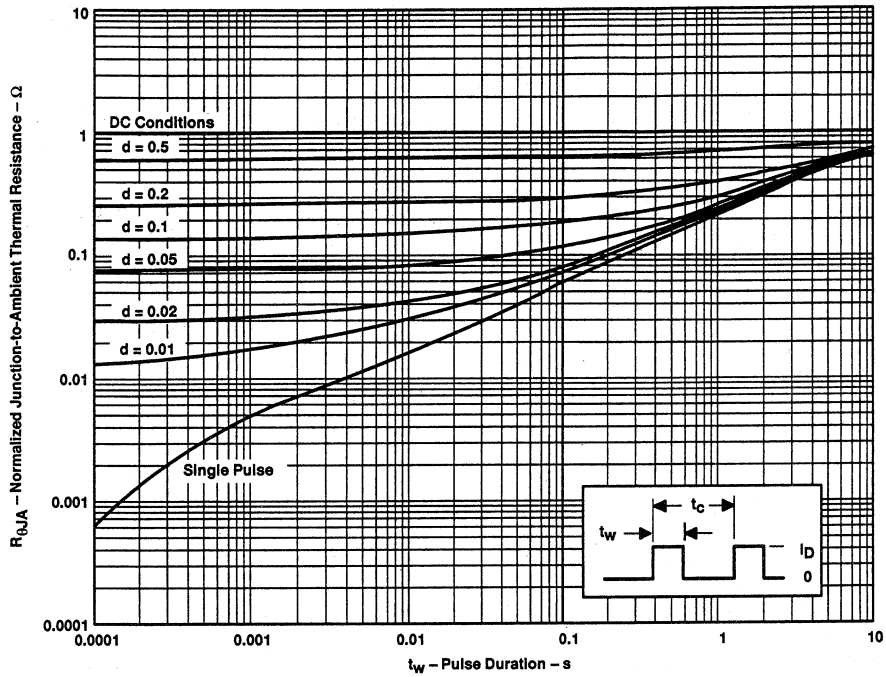


Figure 16

THERMAL INFORMATION

D PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink.

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

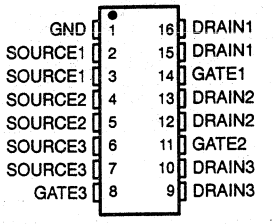
Figure 17

3-CHANNEL INDEPENDENT LOGIC-LEVEL POWER DMOS ARRAY

SLIS034A – JUNE 1994 – REVISED NOVEMBER 1994

- Low $r_{DS(on)}$ . . . 0.45 Ω Typ
- High-Voltage Outputs . . . 60 V
- Pulsed Current . . . 3 A Per Channel
- Fast Commutation Speed
- Direct Logic-Level Interface

D PACKAGE
(TOP VIEW)

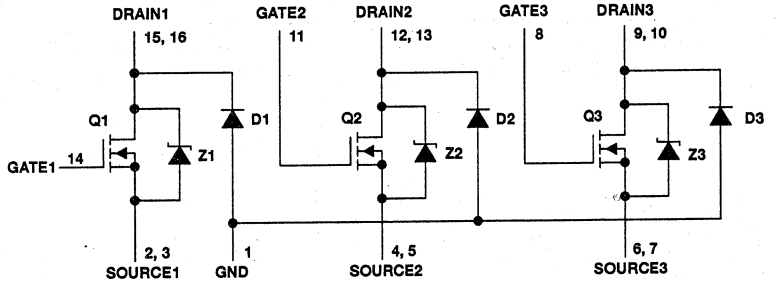


description

The TPIC5322L is a monolithic logic-level power DMOS array that consists of three electrically isolated independent N-channel enhancement-mode DMOS transistors.

The TPIC5322L is offered in a standard 16-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	3 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	18 mJ
Continuous total power dissipation at (or below) T_C = 25°C	1.09 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	V_{DS} = V_{GS},	1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, and D3)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, See Notes 2 and 3	V_{GS} = 5 V,		0.45	0.525	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, See Notes 2 and 3 and Figure 12	V_{GS} = 0,		0.85	1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A			3.7		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V,	V_{DS} = 0		10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.45	0.525	Ω
			T_C = 125°C		0.7	0.78	
g_{fs}	Forward transconductance	V_{DS} = 10 V, See Notes 2 and 3 and Figure 9	I_D = 0.5 A,	1	1.24		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz,	V_{GS} = 0, See Figure 11		135	170	pF
C_{oss}	Short-circuit output capacitance, common source				80	100	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 0.5 A, V_{GS} = 0, See Figures 1 and 14	V_{DS} = 48 V, di/dt = 100 A/µs,	Z1, Z2, Z3		35		ns
				D1, D2, D3		110		
Q_{RR}	Total diode charge			Z1, Z2,Z3		0.035		µC
				D1, D2, D2		0.35		

resistive-load switching characteristics, T_C = 25°C

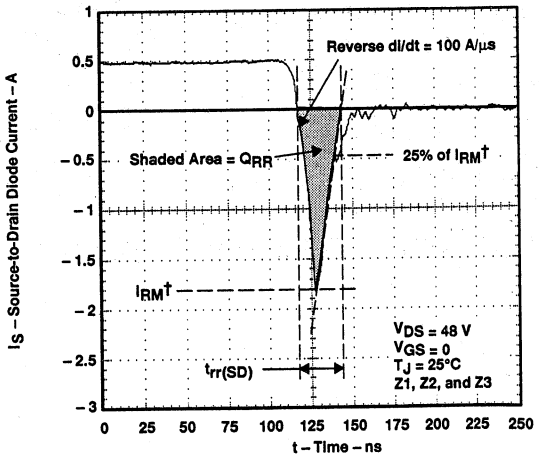
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 50 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		8	16	ns
$t_{d(off)}$	Turn-off delay time			15	30	
t_r	Rise time			5	10	
t_f	Fall time			13	26	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.5 A, V_{GS} = 5 V, See Figure 3		3.1	3.8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.4	0.5	
Q_{gd}	Gate-to-drain charge			1.3	1.6	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see Note 4)	All outputs with equal power		115		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			32		°C/W

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

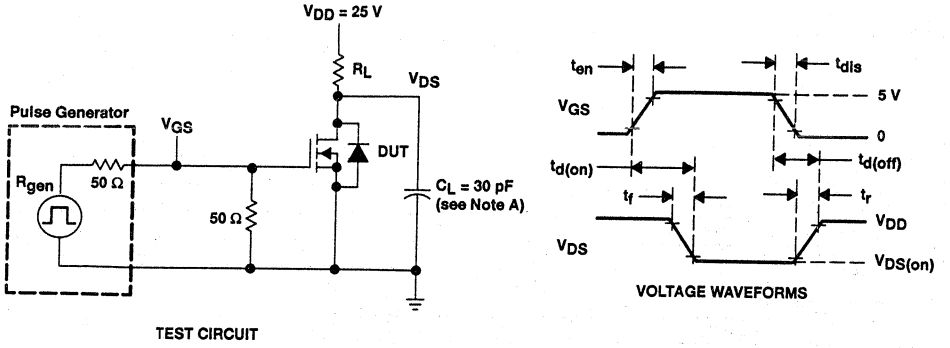
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
NOTE A: The above waveform is representative of D1, D2, and D3 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

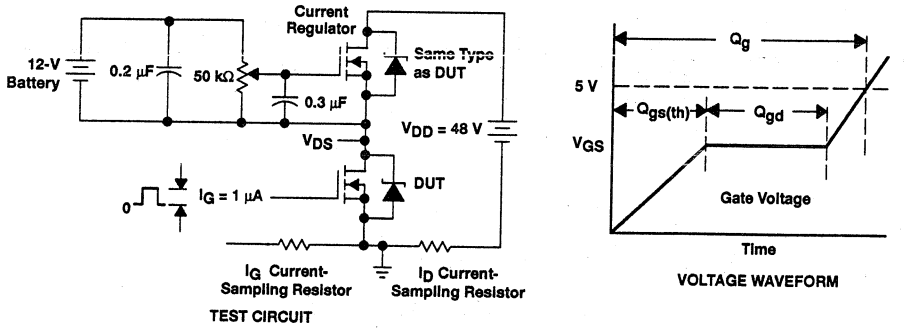
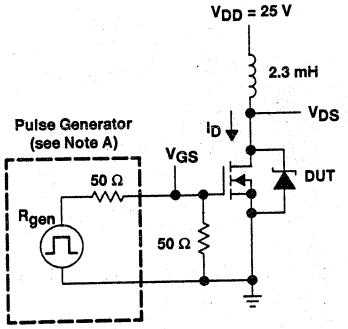
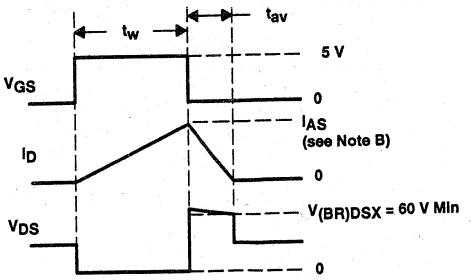


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 18$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

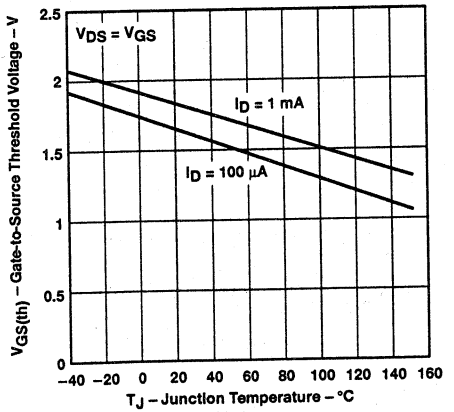


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

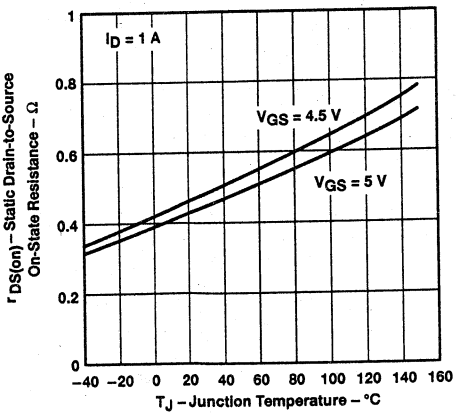


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

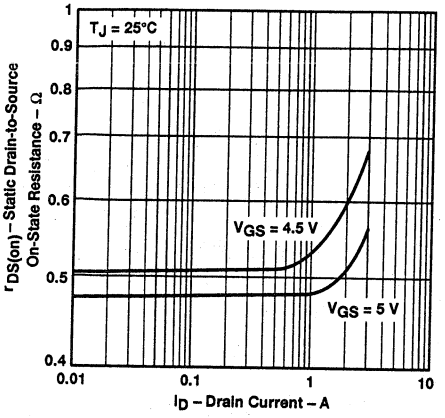


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

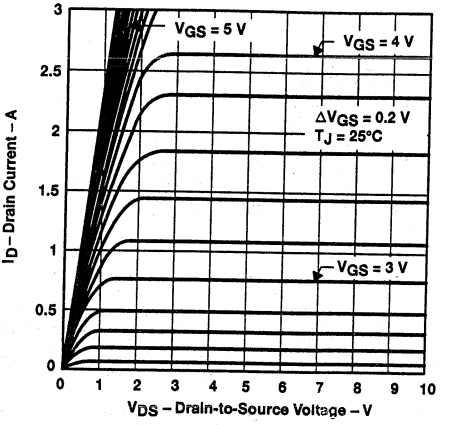


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

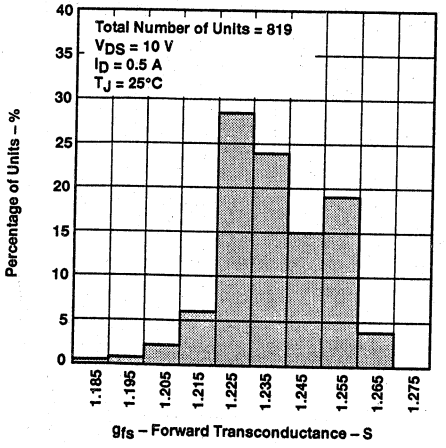


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

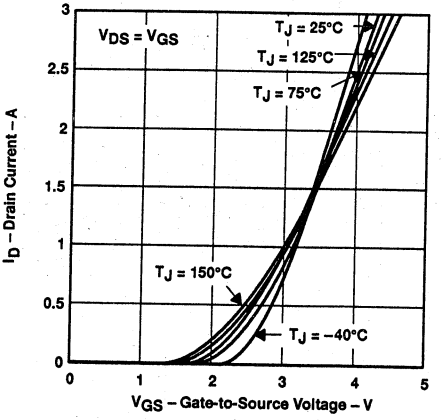


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

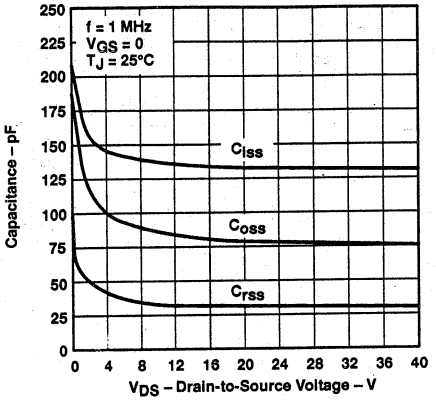


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

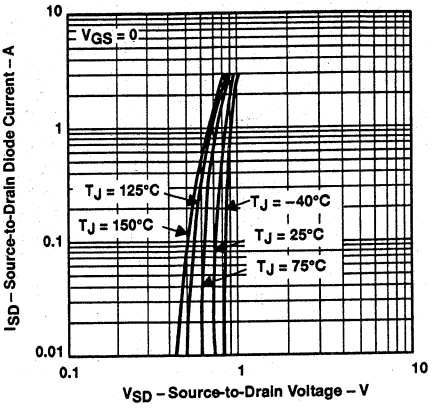


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

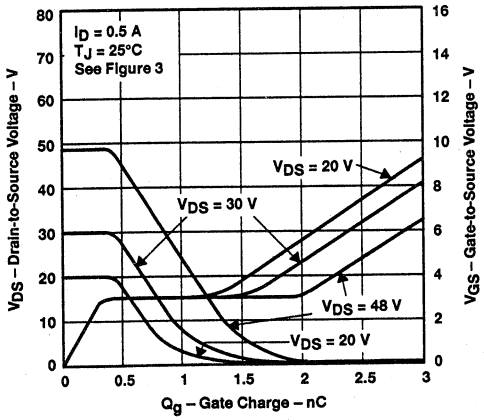


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

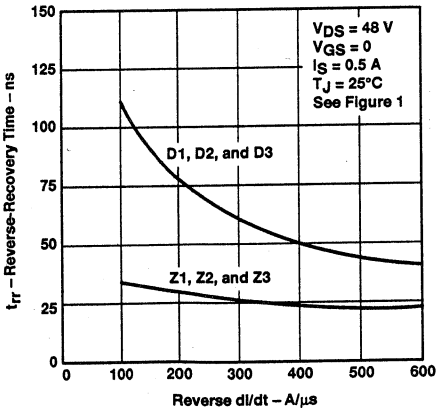
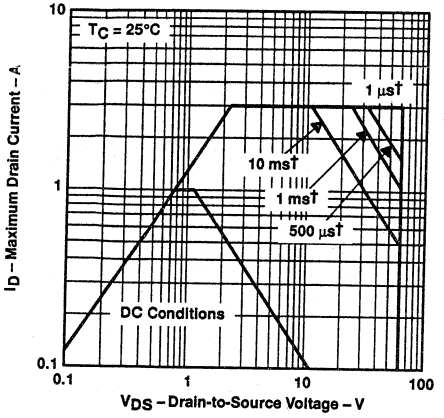


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

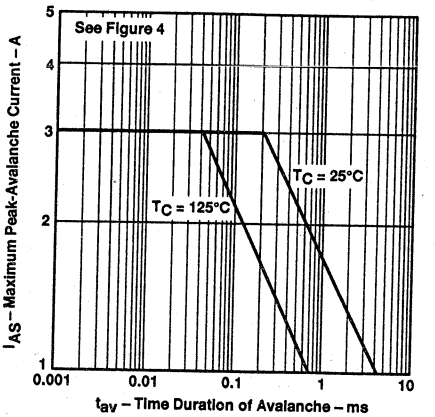
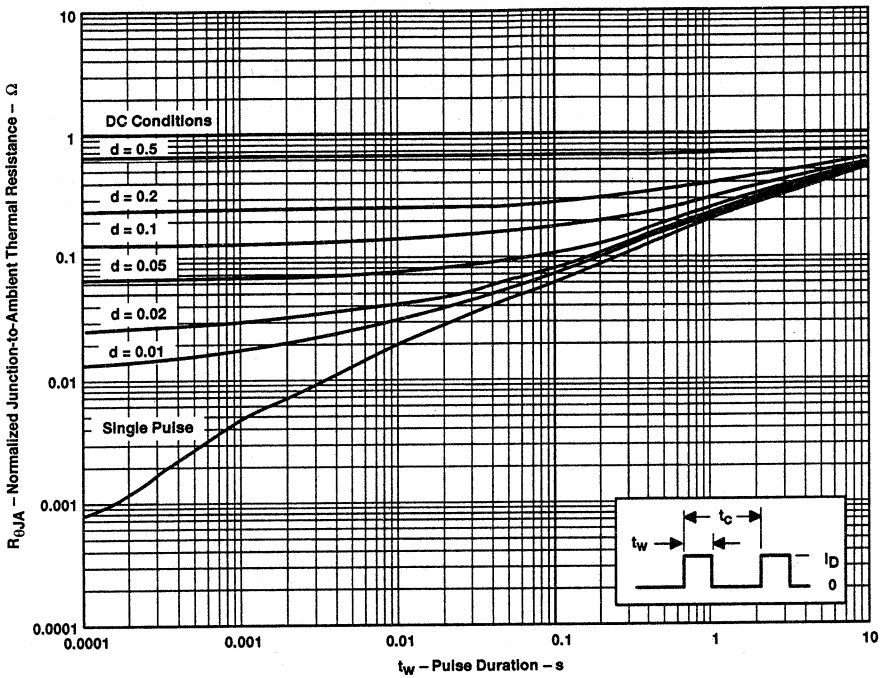


Figure 16

TEXAS INSTRUMENTS

THERMAL INFORMATION

D PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

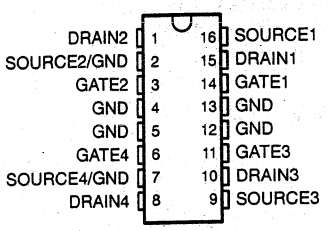
- Low $r_{DS(on)}$ . . . 0.3 Ω Typ
- High-Voltage Output . . . 60 V
- Pulsed Current . . . 10 A Per Channel
- Fast Commutation Speed

description

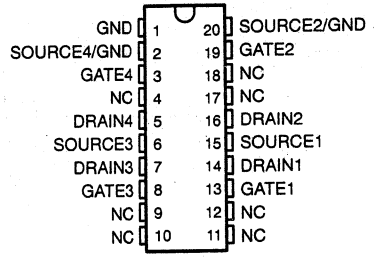
The TPIC5404 is a monolithic power DMOS transistor array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with common source.

The TPIC5404 is offered in a thermally enhanced dual-in-line (NE) package and a wide-body surface-mount (DW) package. The TPIC5404 is characterized for operation over the case temperature range of –40°C to 125°C.

NE PACKAGE
(TOP VIEW)

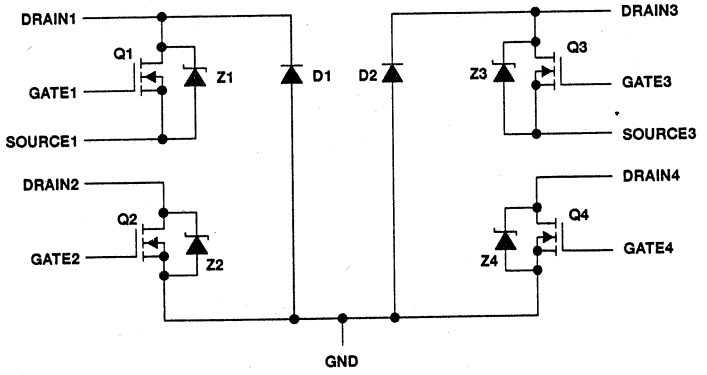


DW PACKAGE
(TOP VIEW)



NC – No internal connection

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage range, V_{GS}	±20
Continuous drain current, each output, T_C = 25°C: DW package	1.7 A
NE package	2 A
Continuous source-to-drain diode current (NE package)	2 A
Pulsed drain current, each output, T_C = 25°C (see Note 1 and Figure 15)	10 A
Single-pulse avalanche energy, T_C = 25°C (see Figures 4 and 16)	21 mJ
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Pulse duration = 10 ms, duty cycle = 6%

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
NE	2075 mW	16.6 mW/°C	415 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 2 A, V_{GS} = 10 V, See Notes 2 and 3			0.6	0.7	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 2 A (D1, D2), See Notes 2 and 3			7.5		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 2 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3			1	1.2	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V,	V_{DS} = 0		10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_R = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 2 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.3	0.35	Ω
			T_C = 125°C		0.41	0.5	
g_{fs}	Forward transconductance	V_{DS} = 15 V, See Notes 2 and 3	I_D = 1 A,	1.6	1.9		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz	V_{GS} = 0,		220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum, pulse duration ≤ 5 ms.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time, source-to-drain	I_S = 1 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, (Z1 and Z3), See Figure 1		120		ns
Q_{RR}	Total diode charge			0.12		µC
$t_{rr(SD)}$	Reverse recovery time, source-to-drain	I_S = 1 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, (Z2 and Z4), See Figure 1		280		ns
Q_{RR}	Total diode charge			0.9		µC

GND-to-drain diode characteristics, T_C = 25°C (see schematic, D1 and D2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_F = 1 A, V_{DS} = 48 V, di/dt = 100 A/µs, See Figure 1		260		ns
Q_{RR}	Total diode charge			2.2		µC

resistive-load switching characteristics, T_C = 25°C

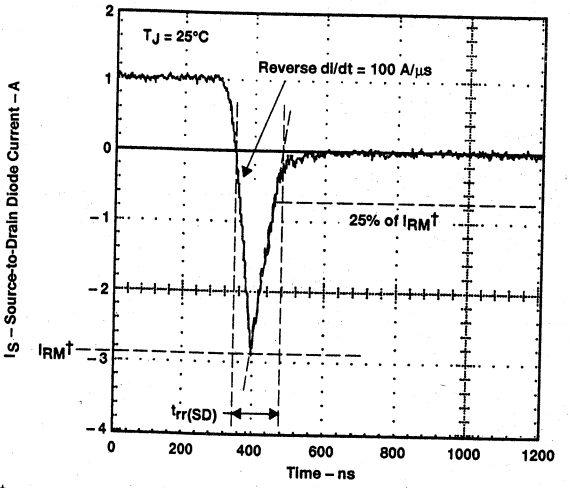
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 25 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		7	15	ns
$t_{d(off)}$	Turn-off delay time			25	50	
t_r	Rise time			15	30	
t_f	Fall time			25	50	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1 A, V_{GS} = 10 V, See Figure 3		6.6	8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.8	1	
Q_{gd}	Gate-to-drain charge			2.6	3.2	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DW package	All outputs with equal power, See Note 4		90		°C/W
		NE package			60		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

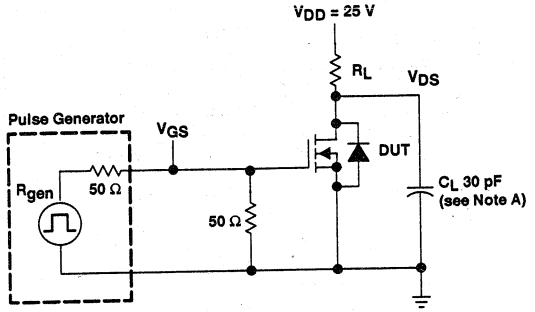
PARAMETER MEASUREMENT INFORMATION



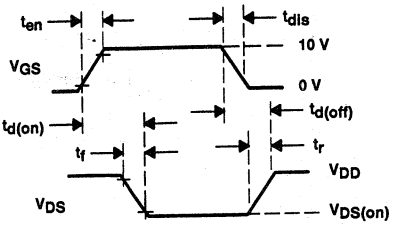
† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



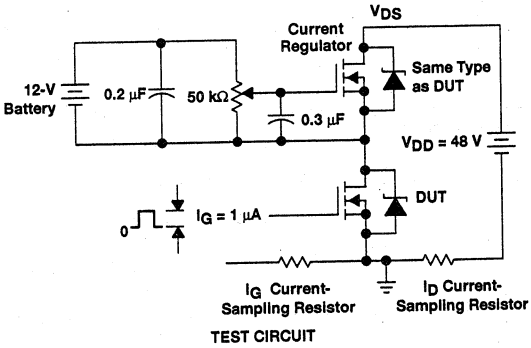
TEST CIRCUIT



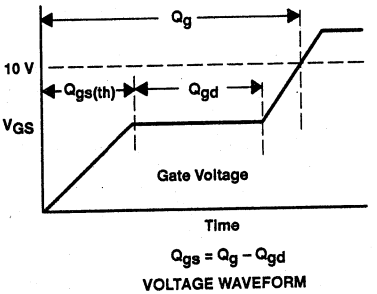
VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms



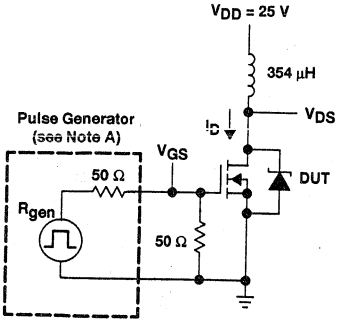
TEST CIRCUIT



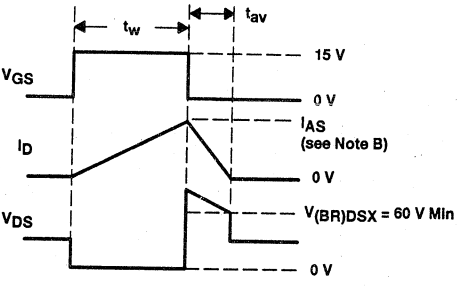
VOLTAGE WAVEFORM

Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 10$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 21$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

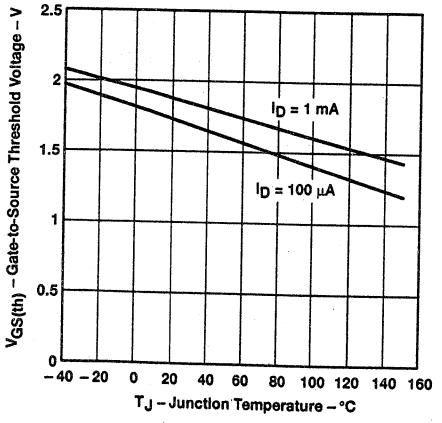


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

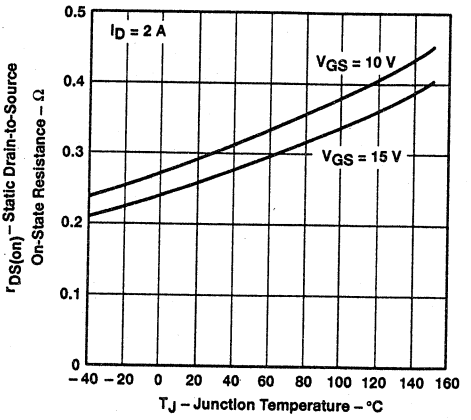


Figure 6

TYPICAL CHARACTERISTICS

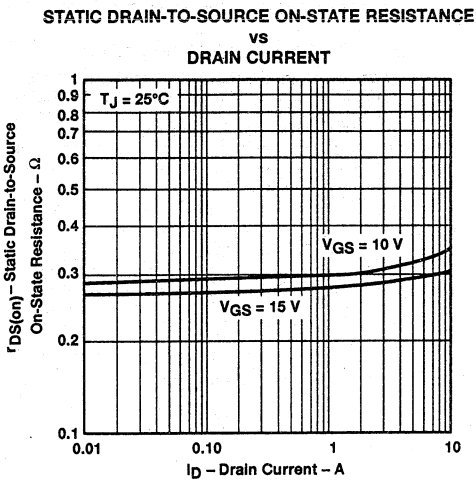


Figure 7

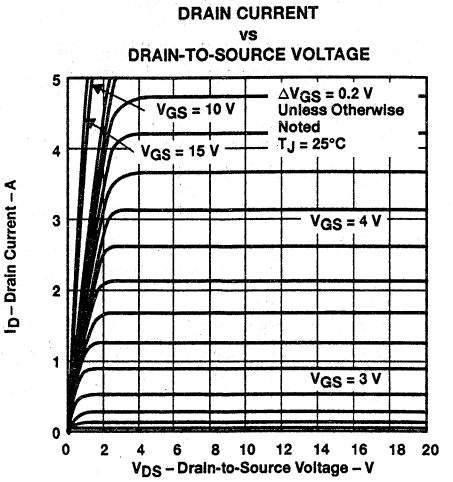


Figure 8

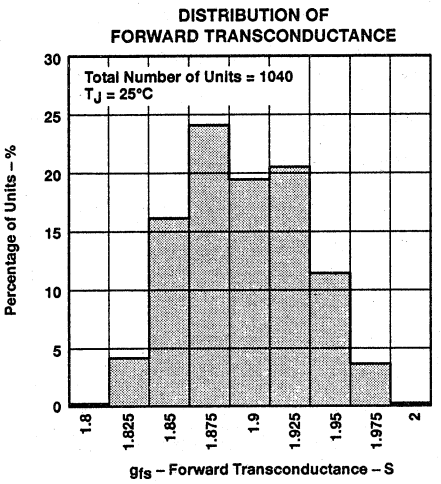


Figure 9

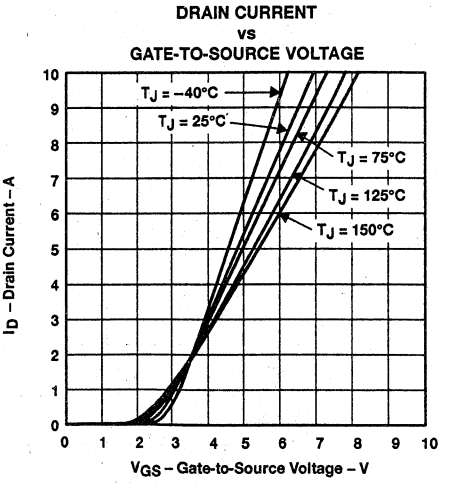


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

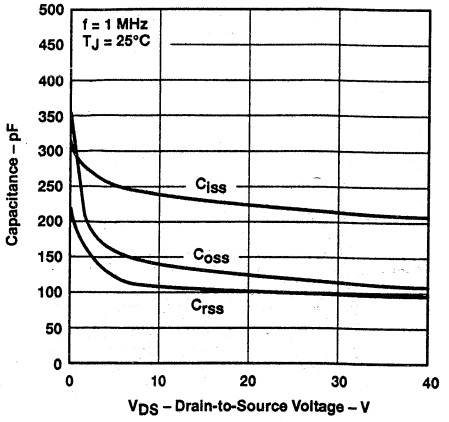


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

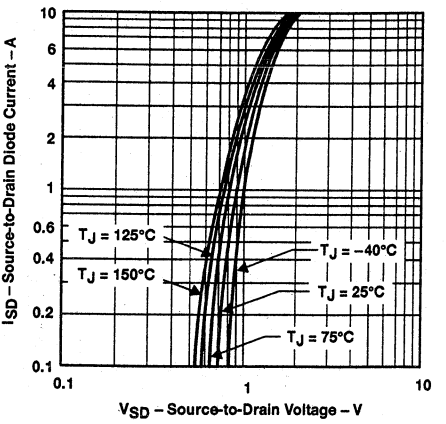


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

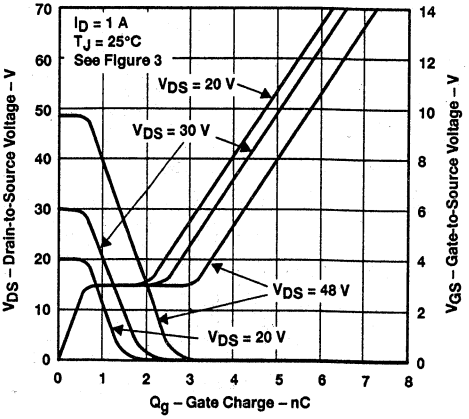


Figure 13

REVERSE RECOVERY TIME
vs
REVERSE di/dt

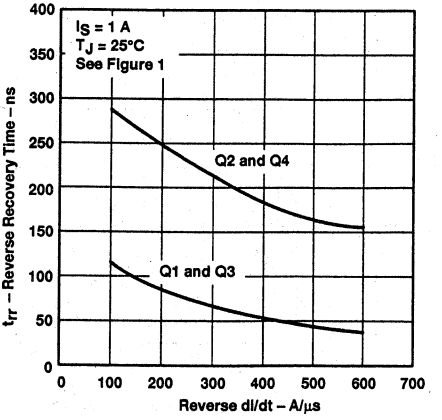
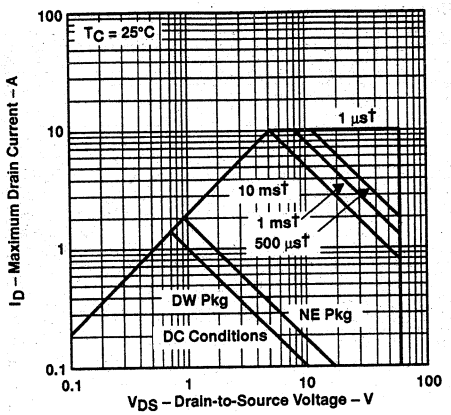


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 0.1 duty cycle

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

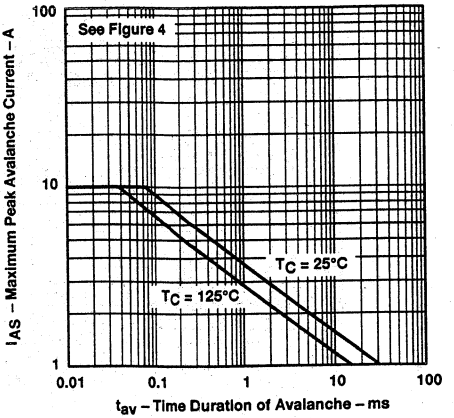
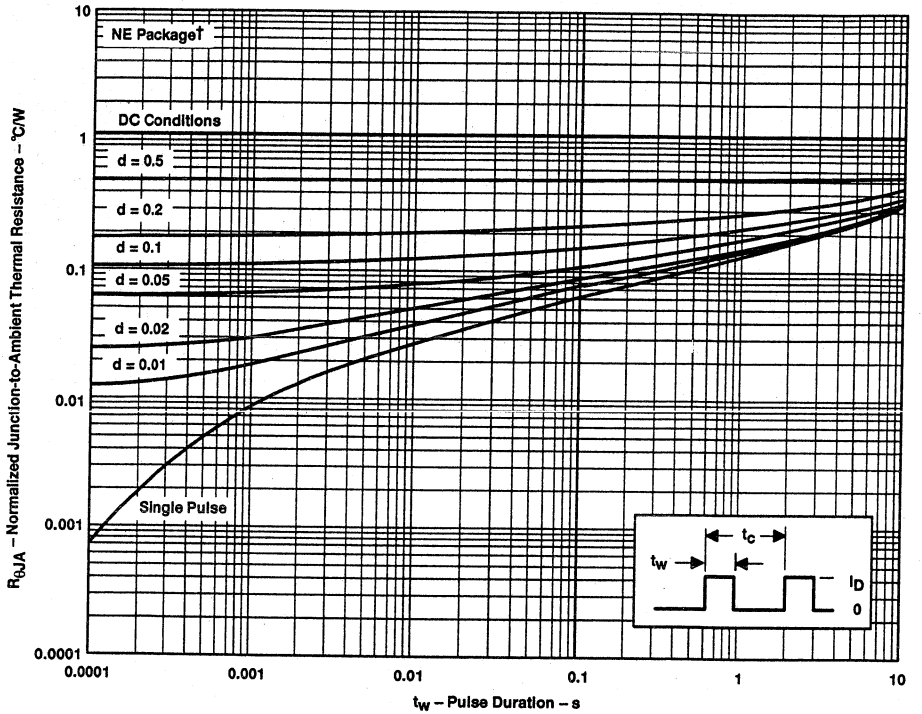


Figure 16

THERMAL INFORMATION

NE PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



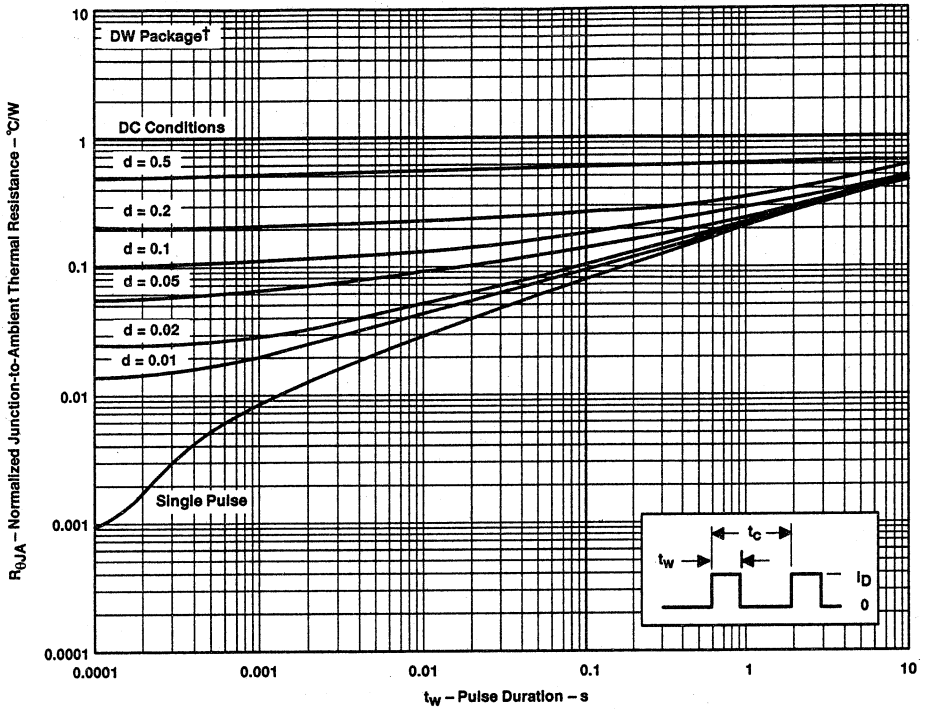
† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W / t_C

Figure 17

THERMAL INFORMATION

DW PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

Figure 18

SLIS026A – JUNE 1994 – REVISED NOVEMBER 1994

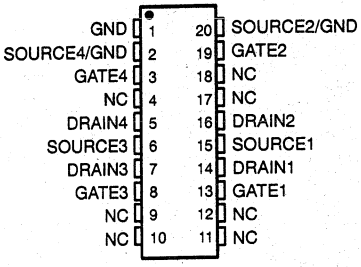
- Low $r_{DS(on)}$ . . . 0.4 Ω Typ
- High-Voltage Output . . . 60 V
- Pulsed Current . . . 3 A Per Channel
- Fast Commutation Speed
- Direct Logic-Level Interface

description

The TPIC5424L is a monolithic logic-level power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with a common source.

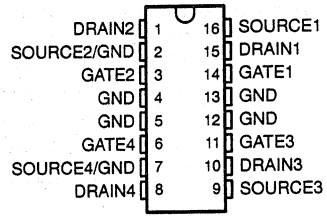
The TPIC5424L is offered in a 16-pin thermally enhanced dual-in-line (NE) package and a 20-pin wide-body surface-mount (DW) package. The TPIC5424L is characterized for operation over the case temperature range of –40°C to 125°C.

DW PACKAGE
(TOP VIEW)

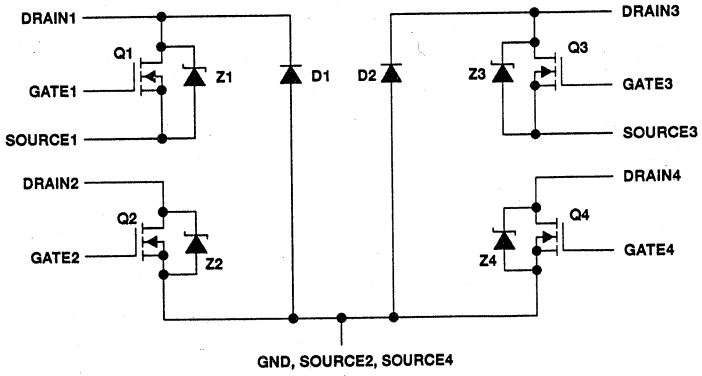


NC – No internal connection

NE PACKAGE
(TOP VIEW)



schematic



TEXAS INSTRUMENTS

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, T_C = 25°C	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	3 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	18 mJ
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	279 mW
NE	2075 mW	16.6 mW/°C	415 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, V_{GS} = 5 V, See Notes 2 and 3			0.4	0.48	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12			1	1.2	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A (D1, D2), See Notes 2 and 3			4.6		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 5 V,	V_{DS} = 0		10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 5 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V (D1, D2)	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.4	0.48	Ω
			T_C = 125°C		0.65	0.68	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 0.5 A, See Notes 2 and 3 and Figure 9		1.25	1.39		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0, See Figure 11			220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S =0.5 A, V_{GS} = 0, See Figures 1 and 14 V_{DS} = 48 V, di/dt = 100 A/µs,	Z1 and Z3		55		ns
			Z2 and Z4		150		
			D1 and D2		200		
Q_{RR}	Total diode charge		Z1 and Z3		0.06		µC
			Z2 and Z4		0.3		
			D1 and D2		0.7		

resistive-load switching characteristics, T_C = 25°C

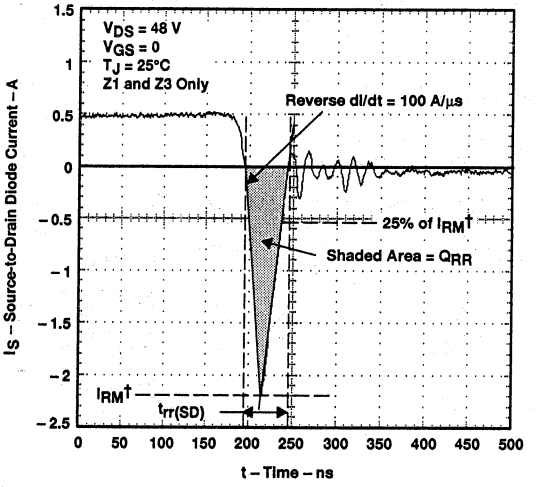
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 25 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		9	18	ns
$t_{d(off)}$	Turn-off delay time			20	40	
t_r	Rise time			21	42	
t_f	Fall time			25	50	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1 A, V_{GS} = 10 V, See Figure 3		3.9	5	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.55	0.8	
Q_{gd}	Gate-to-drain charge			2.5	3.6	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see Note 4)	DW package	All outputs with equal power		90		°C/W
		NE package			60		
$R_{\theta JC}$	Junction-to-case thermal resistance	DW package			30		°C/W
		NE package			25		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

PARAMETER MEASUREMENT INFORMATION

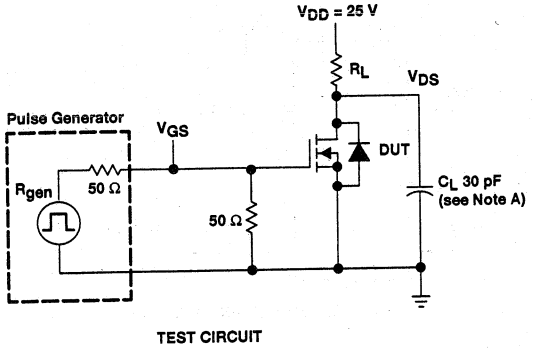


† I_{RM} = maximum recovery current

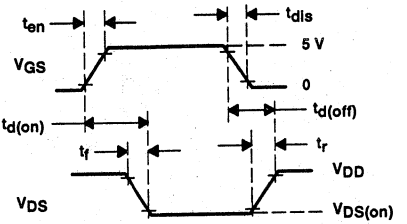
NOTE A: The above waveform is representative of Z2, Z4, D1, and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



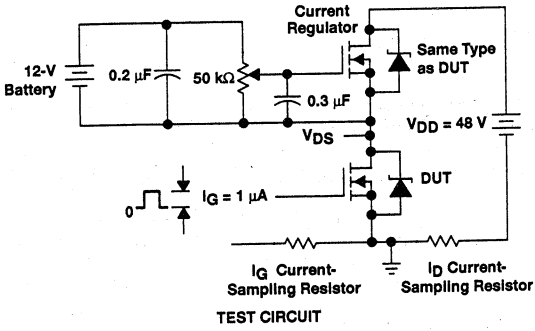
TEST CIRCUIT



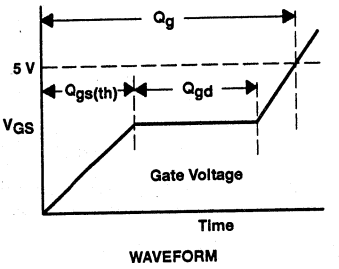
VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms



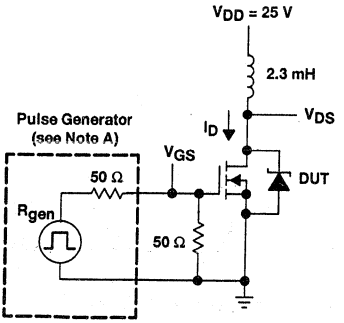
TEST CIRCUIT



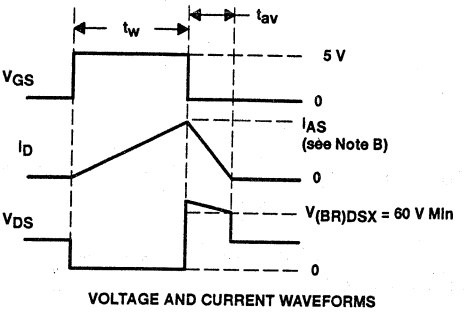
WAVEFORM

Figure 3. Gate-Charge Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 18$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

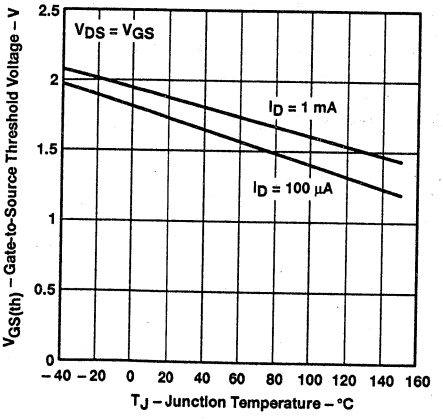


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

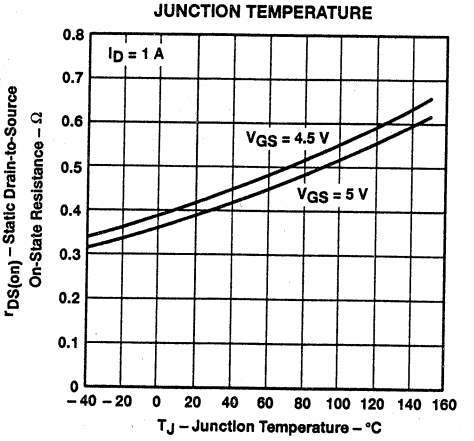


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

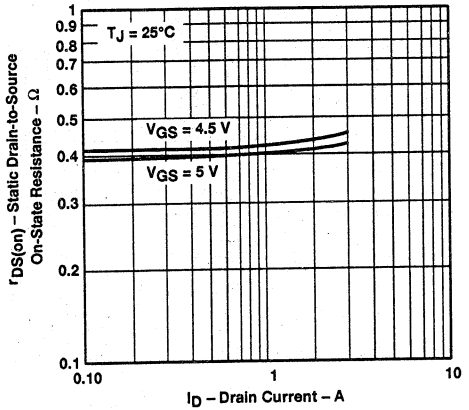


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

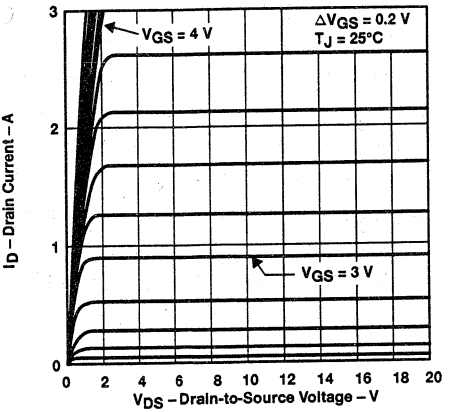


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

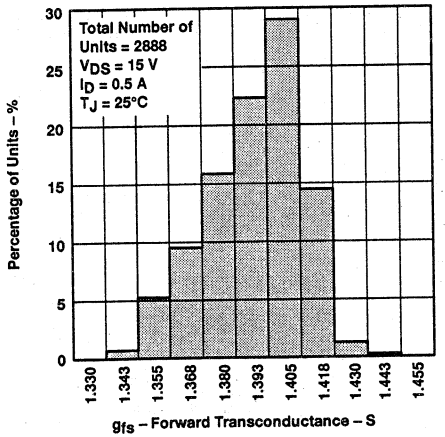


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

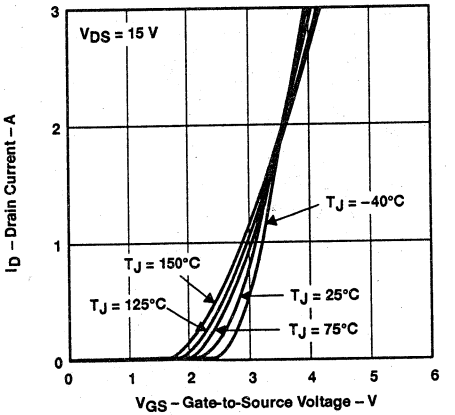


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

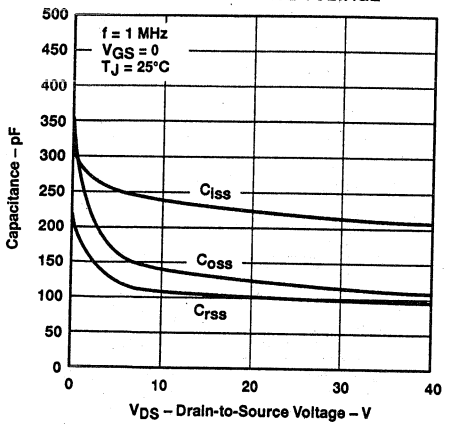


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

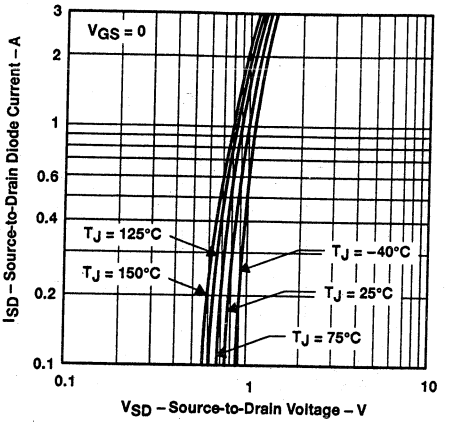


Figure 12

GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

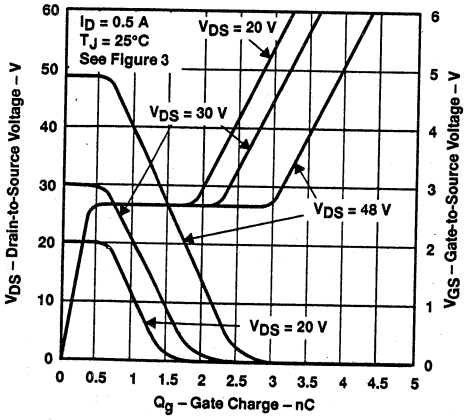


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE dI/dt

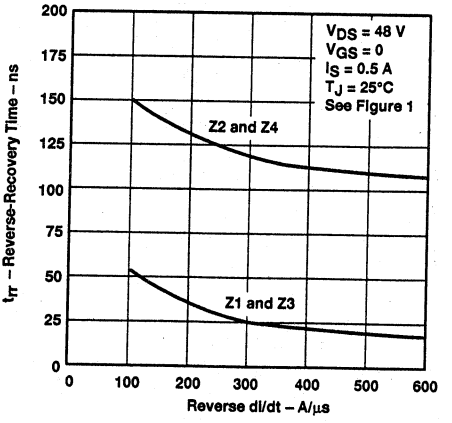
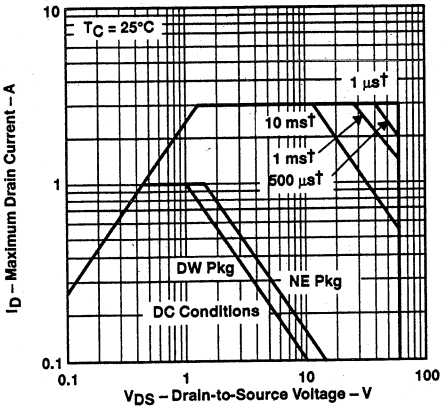


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

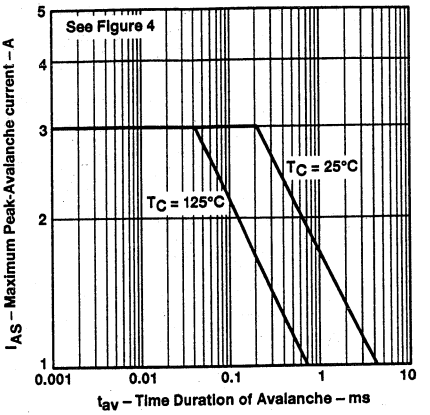
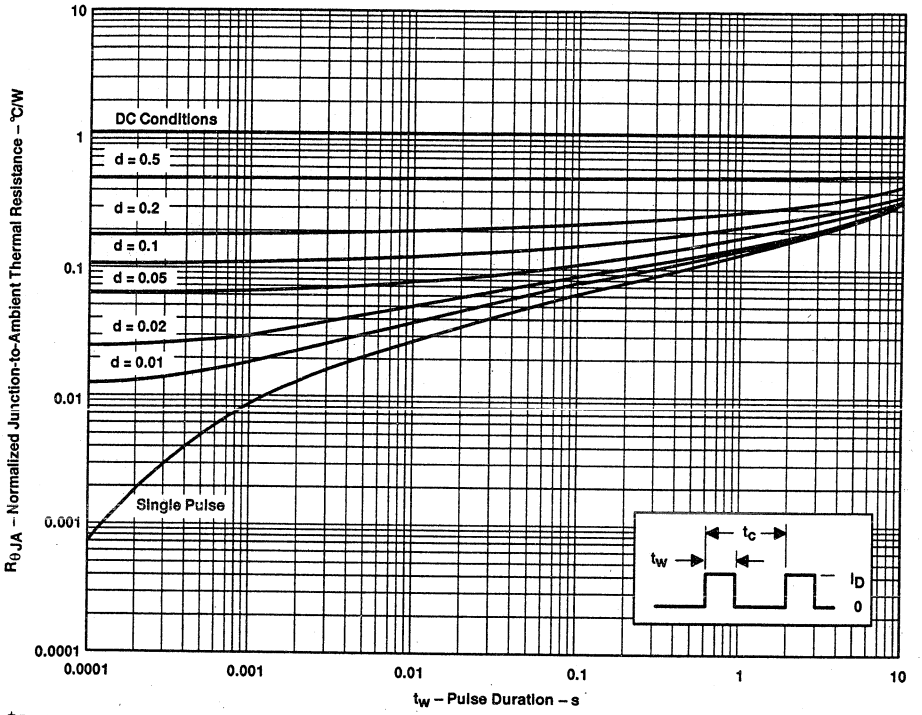


Figure 16

THERMAL INFORMATION

NE PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



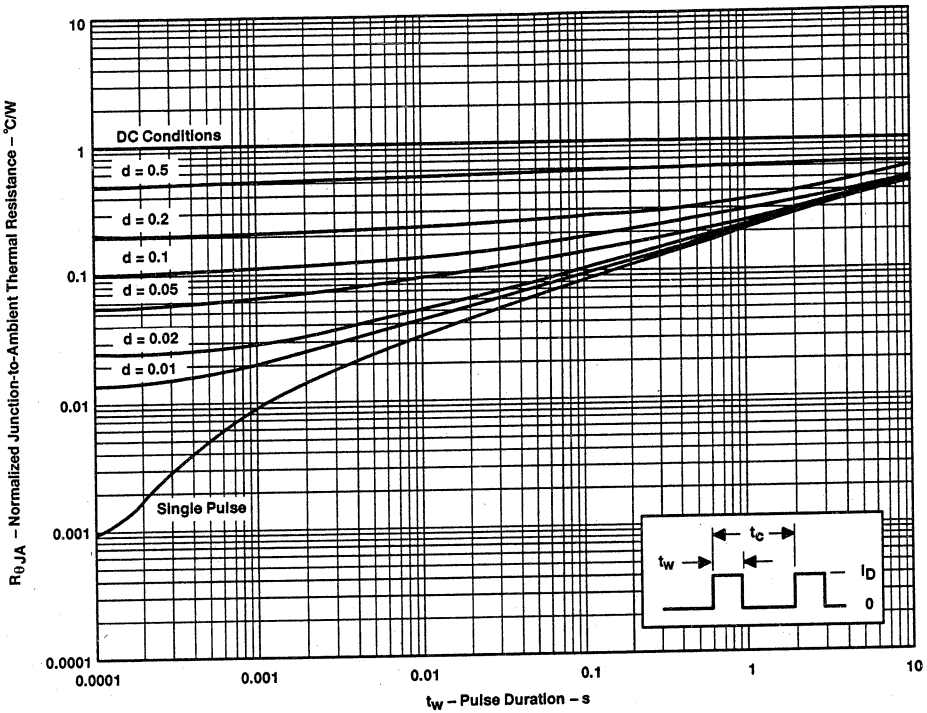
† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

THERMAL INFORMATION

DW PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

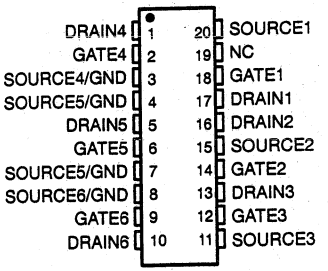
NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 18

SLIS033A – JUNE 1994 – REVISED NOVEMBER 1994

- Low $r_{DS(on)}$ . . . 0.4 Ω Typ
- High-Voltage Output . . . 60 V
- Pulsed Current . . . 3 A Per Channel
- Fast Commutation Speed
- Direct Logic-Level Interface

DW PACKAGE
(TOP VIEW)



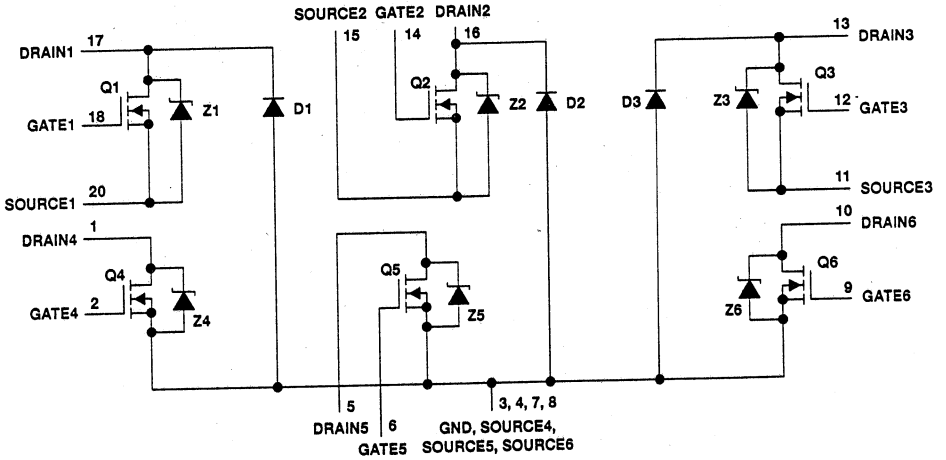
NC – No internal connection

description

The TPIC5621L is a monolithic logic-level power DMOS transistor array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors, three of which are configured with a common source.

The TPIC5621L is offered in a 20-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q2, and Q3)	100 V
Drain-to-GND voltage (Q1, Q2, and Q3)	100 V
Drain-to-GND voltage (Q4, Q5, and Q6)	60 V
Gate-to-source voltage range, V_{GS}	±20 V
Continuous drain current, each output, T_C = 25°C	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, I_{max}, T_C = 25°C (each output, see Note 1 and Figure 15)	3 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4, 15 and 16)	18 mJ
Continuous total dissipation (see Figure 15)	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	279 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, and D3)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, V_{GS} = 5 V, See Notes 2 and 3			0.4	0.48	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0 (Z1, Z2, Z3, Z4, Z5, Z6), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A (D1, D2, D3), See Notes 2 and 3			4.6		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V (D1, D2, D3)	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.4	0.48	Ω
			T_C = 125°C		0.65	0.68	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 0.5 A, See Notes 2 and 3 and Figure 9		1	1.29	1.45	S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0, See Figure 11			190	240	pF
C_{oss}	Short-circuit output capacitance, common source				100	125	
C_{rss}	Short-circuit reverse transfer capacitance, common source				40	50	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 0.5 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, See Figures 1 and 14	Z1, Z2, Z3		65		ns
			Z4, Z5, Z6		150		
			D1, D2, D3		200		
Q_{RR}	Total diode charge		Z1, Z2, Z3		0.06		µC
			Z4, Z5, Z6		0.3		
			D1, D2, D3		0.7		

resistive-load switching characteristics, T_C = 25°C

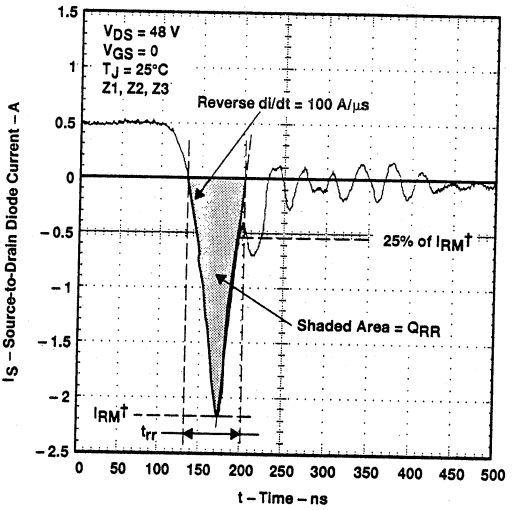
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 50 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		9	18	ns
$t_{d(off)}$	Turn-off delay time			20	40	
t_r	Rise time			21	42	
t_f	Fall time			25	50	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.5 A, V_{GS} = 5 V, See Figure 3		3.1	3.7	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.5	0.6	
Q_{gd}	Gate-to-drain charge			1.9	2.3	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see Note 4)	All outputs with equal power		90		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			27		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

PARAMETER MEASUREMENT INFORMATION



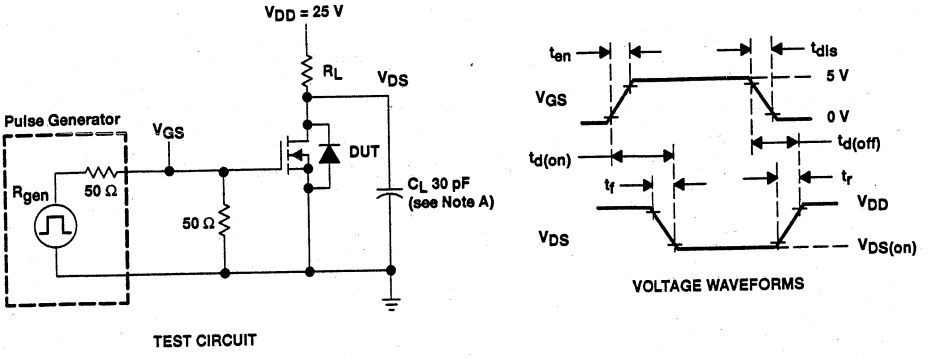
† I_{RM} = maximum recovery current

NOTE A: The above waveform is representative of Z4, Z5, Z6, D1, D2, and D3 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

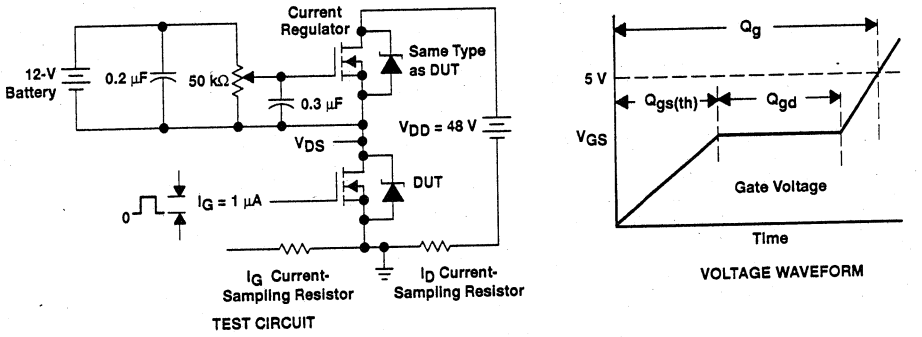
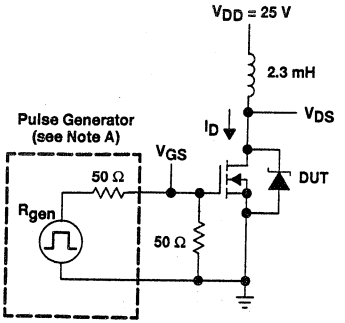
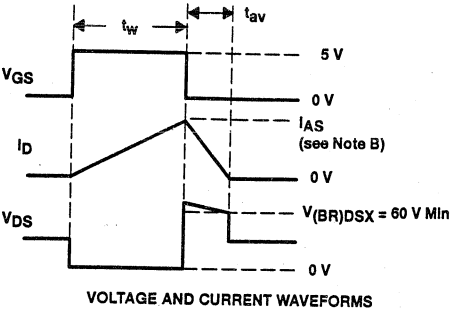


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current I_{AS} = 3 A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 18$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

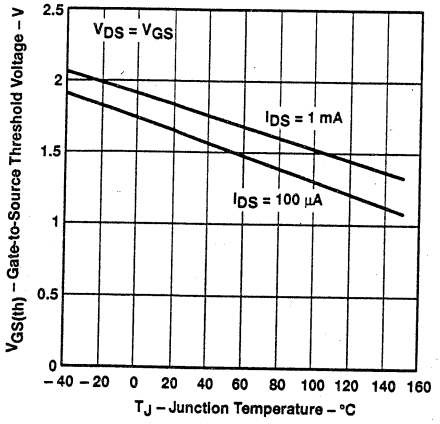


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

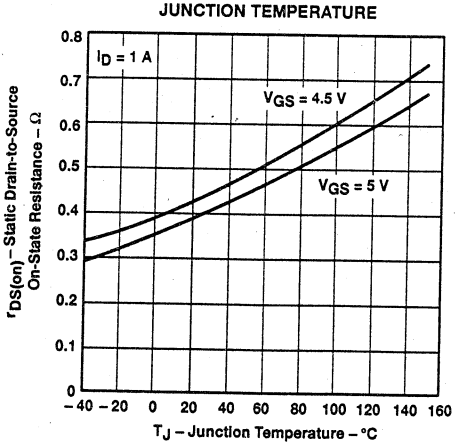


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

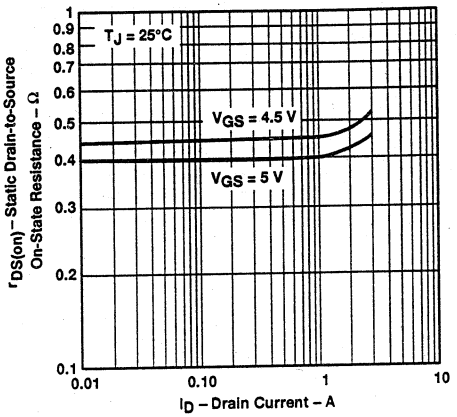


Figure 7

DRAIN-TO-SOURCE CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

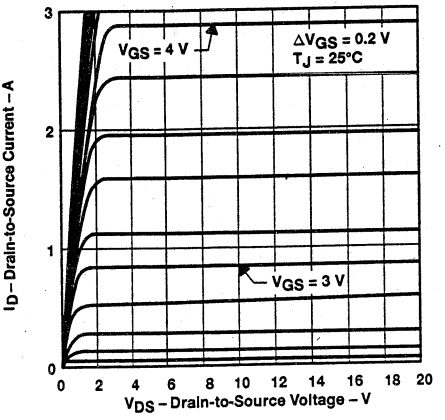


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

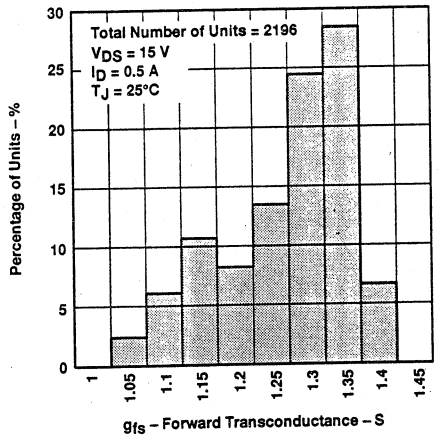


Figure 9

DRAIN-TO-SOURCE CURRENT
vs
GATE-TO-SOURCE VOLTAGE

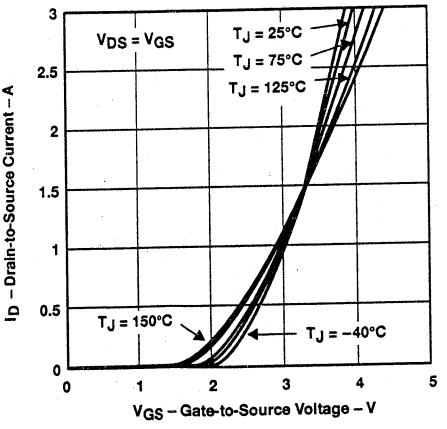


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

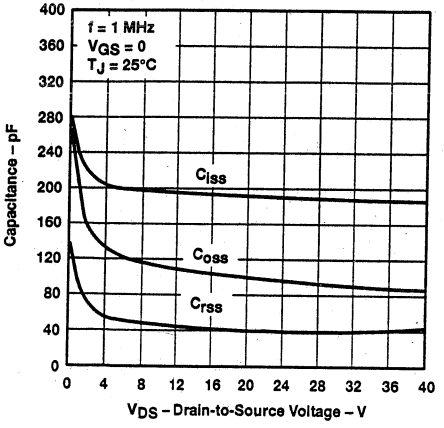


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

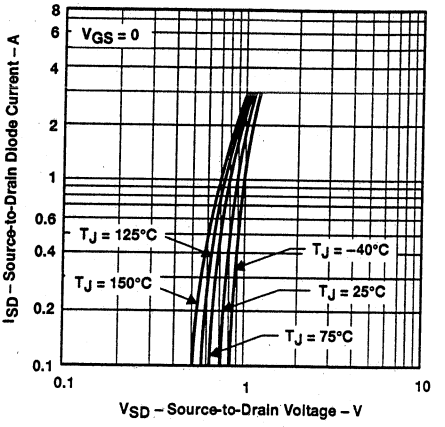


Figure 12

DRAIN-TO-SOURCE AND GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

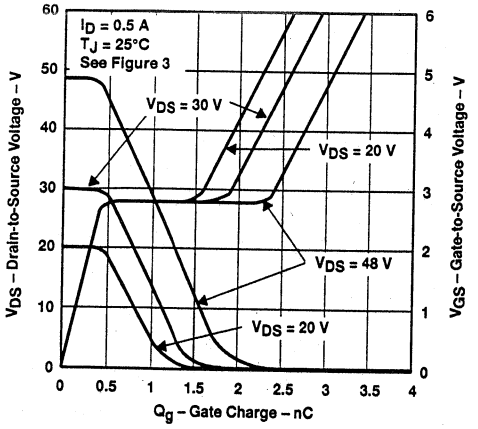


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

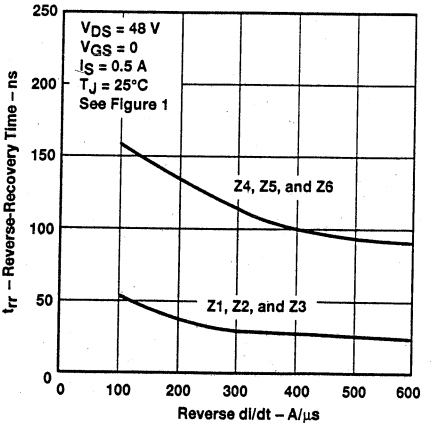
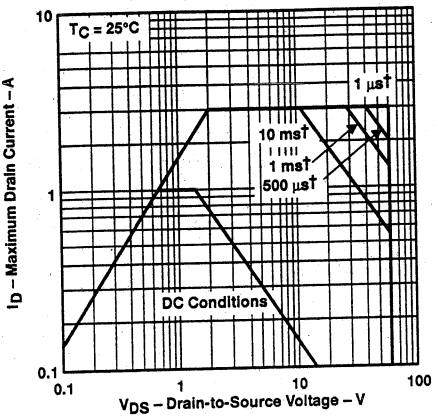


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

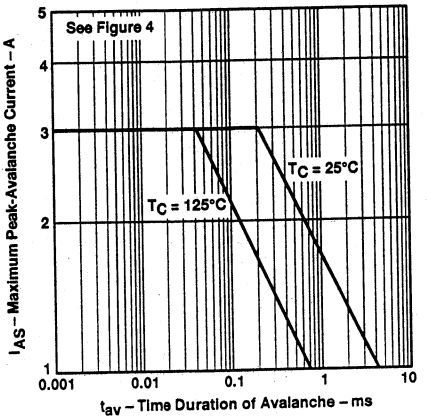
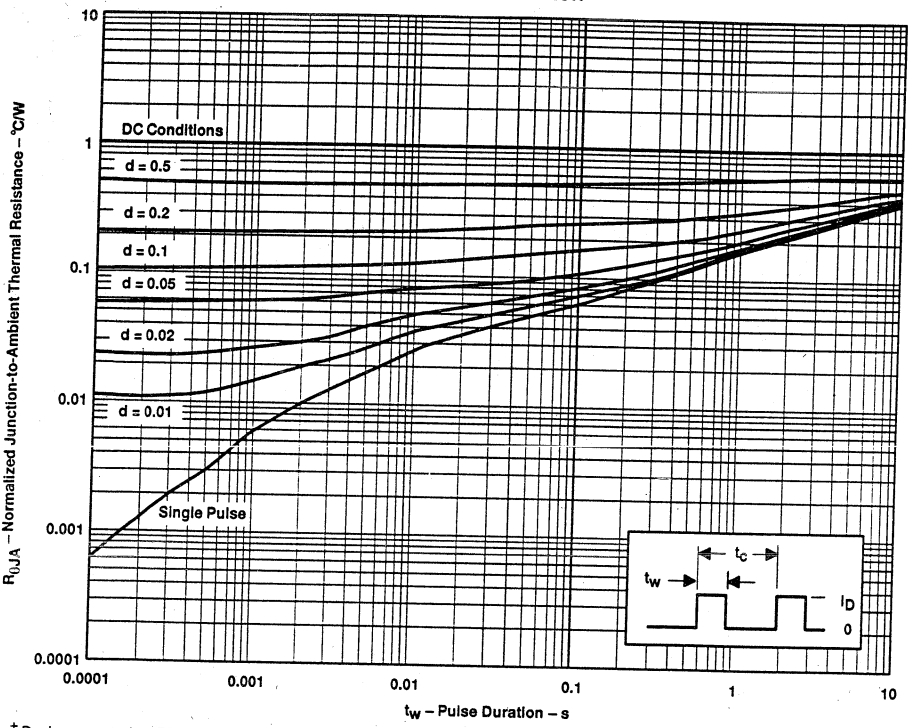


Figure 16

THERMAL INFORMATION

DW PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



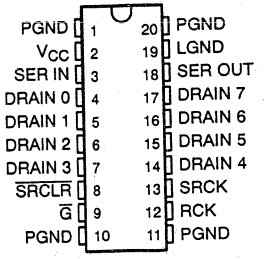
† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\, R_{\theta JA}$
t_W = pulse duration
t_c = cycle time
d = duty cycle = t_W/t_c

Figure 17

- Low $r_{DS(on)}$ . . . 1.3 Ω Typical
- Avalanche Energy . . . 75 mJ
- 8 Power DMOS Transistor Outputs of 250-mA Continuous Current
- 1.5-A Pulsed Current Per Output
- Output Clamp Voltage at 45 V
- Devices Are Cascadable
- Low Power Consumption

N OR DW PACKAGE
(TOP VIEW)

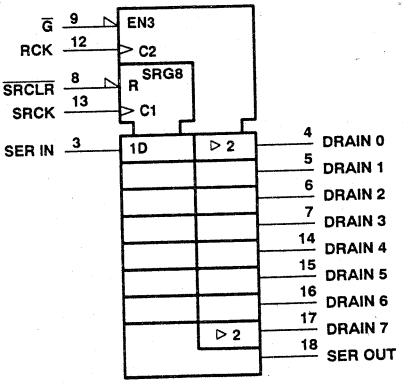


description

The TPIC6595 is a monolithic, high-voltage, high-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{SRCLR}$) is high. When $\overline{SRCLR}$ is low, the input shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

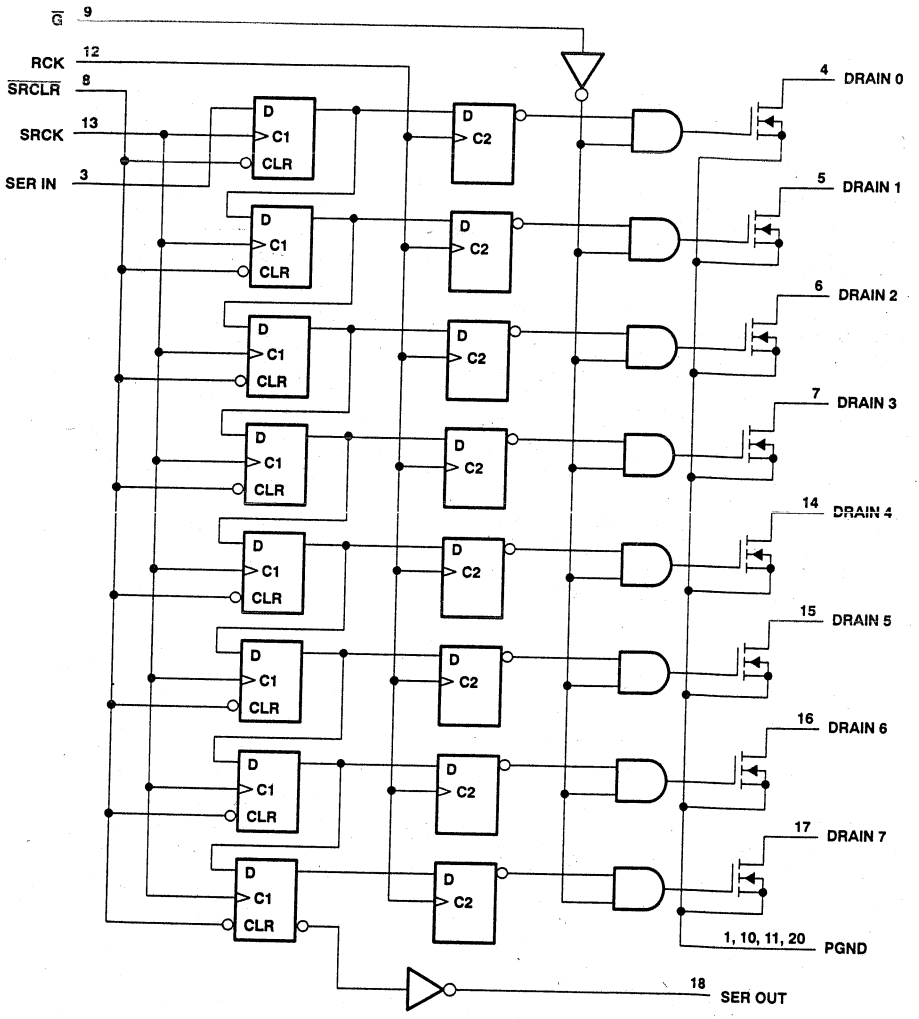
Outputs are low-side, open-drain DMOS transistors with output ratings of 45 V and 250-mA continuous sink current capability. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink current capability.

Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1,10,11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance.

A single-point connection between pin 19, logic ground (LGND) and pins 1, 10, 11, and 20, power ground (PGND) must be externally made in a manner that reduces crosstalk between the logic and load circuits.

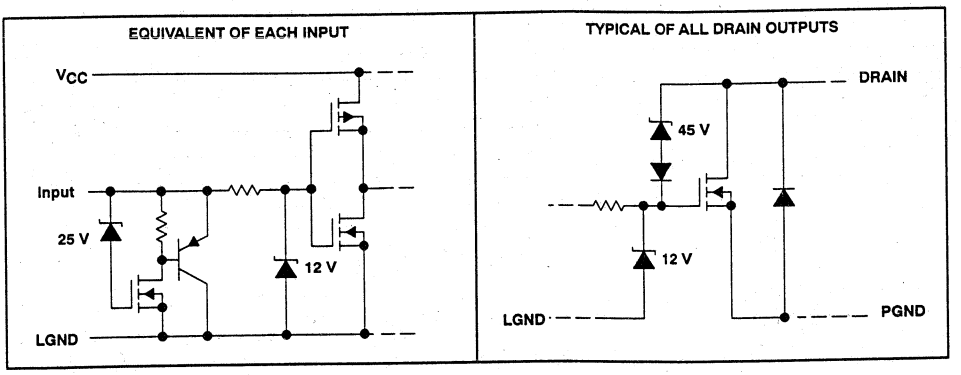
The TPIC6595 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic diagram (positive logic)



TEXAS INSTRUMENTS

schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic Input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	250 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS}, (see Figure 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2 %.
4. V_{DD} = 15 V, starting junction temperature, (T_{JS}) = 25°C, L = 100 mH, I_{AS} = 1A. See Figure 4.

DISSIPATION RATING TABLE

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−1.8	1.5	A
Setup time, t_{su}, SER IN high before SRCK↑ (see Figure 2)	10		ns
Hold time, t_h, SER IN high after SRCK↑ (see Figure 2)	10		ns
Pulse duration, t_w (see Figure 2)	20		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250 mA, See Note 3			0.85	1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = −20 mA, V_{CC} = 4.5 V		4.4	4.49		V
		I_{OH} = −4 mA, V_{CC} = 4.5 V		4.1	4.3		
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20 mA, V_{CC} = 4.5 V			0.002	0.1	V
		I_{OH} = 4 mA, V_{CC} = 4.5 V			0.2	0.4	
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				−1	µA
I_{CC}	Logic supply current	I_O = 0, All inputs low			15	100	µA
$I_{CC(FRQ)}$	Logic supply current frequency	f_{SRCK} = 5 MHz, I_O = 0, C_L = 30 pF, See Figures 1, 2, and 6			0.6	5	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, I_N = I_D, T_C = 85°C	See Notes 5, 6, and 7		250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V			0.05	1	µA
		V_{DS} = 40 V, T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 9 and 10		1.3	2	Ω
		I_D = 250 mA, T_C = 125°C, V_{CC} = 4.5 V			2	3.2	
		I_D = 500 mA, V_{CC} = 4.5 V			1.3	2	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 250 mA, See Figures 1, 2, and 11		650		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			150		ns
t_r	Rise time, drain output			750		ns
t_f	Fall time, drain output			425		ns
t_a	Reverse-recovery-current rise time	I_F = 250 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at 85°C case temperature.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		111	°C/W
		N package			108	

PARAMETER MEASUREMENT INFORMATION

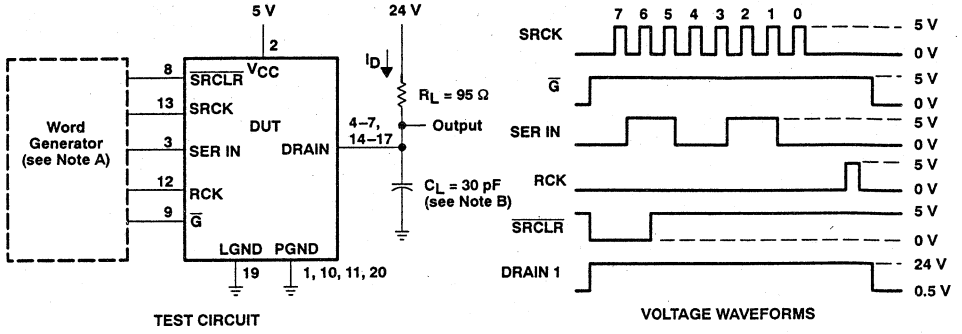


Figure 1. Resistive Load Operation

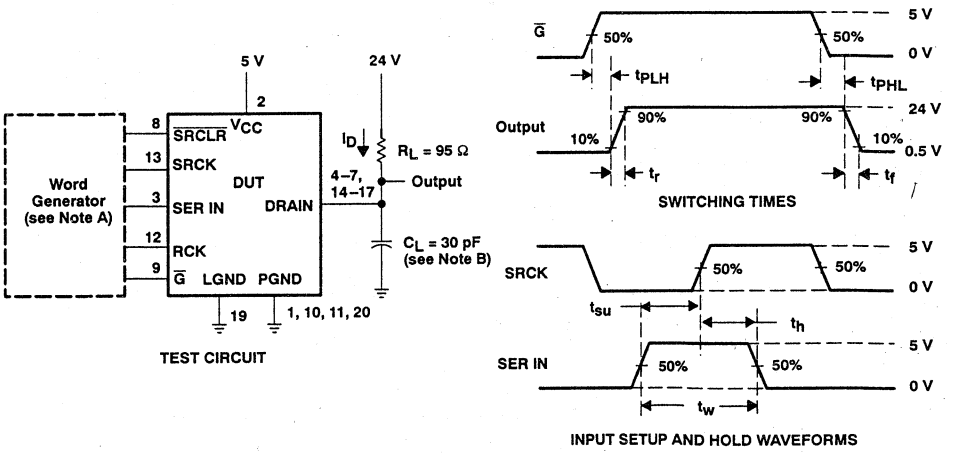
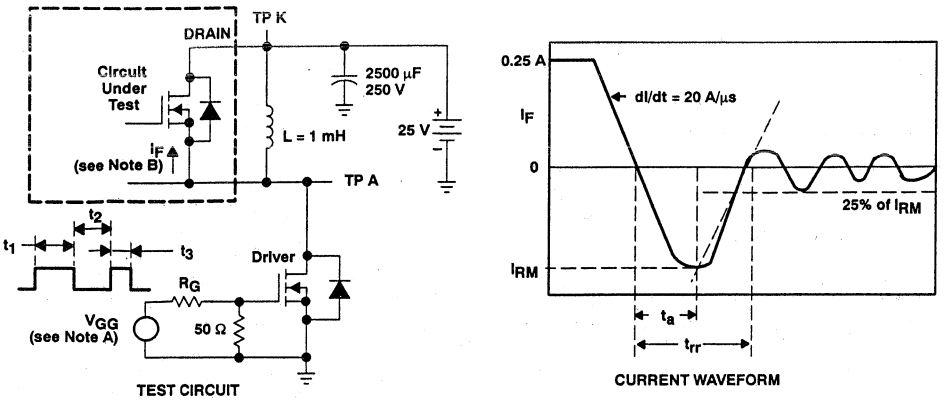


Figure 2. Switching Times

NOTES: A. Outputs DRAIN 1, 2, 5, and 6 low (PGND), all other DRAIN outputs are at 24 V. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

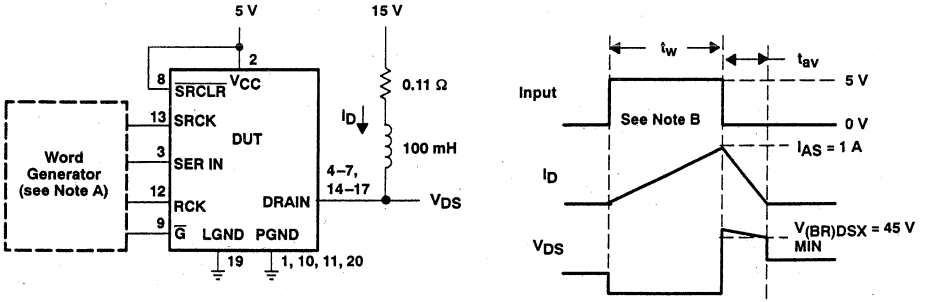
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/μs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t_1 = 10 μs, t_2 = 7 μs, and t_3 = 3 μs.

B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1 A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

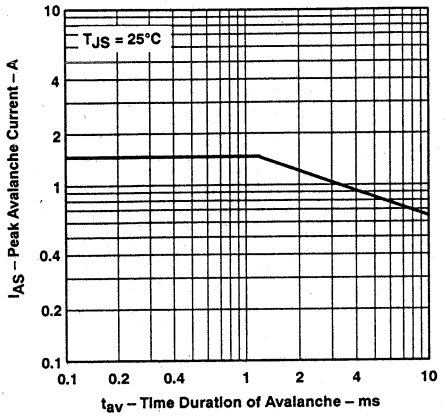


Figure 5

SUPPLY CURRENT
vs
FREQUENCY

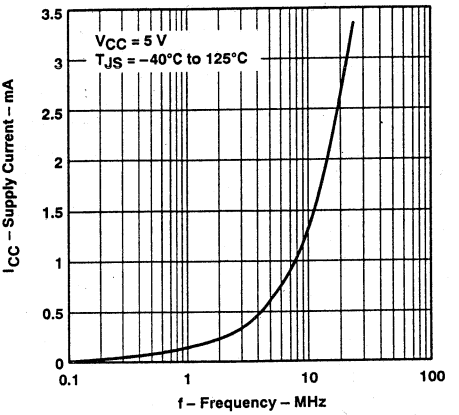


Figure 6

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

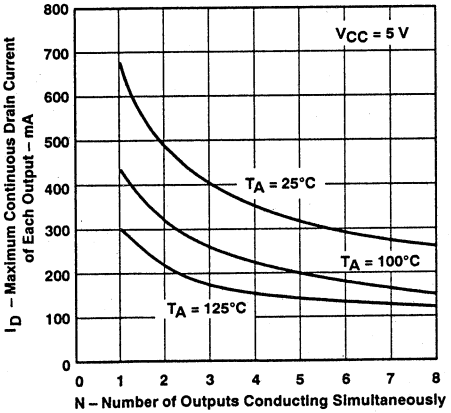


Figure 7

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

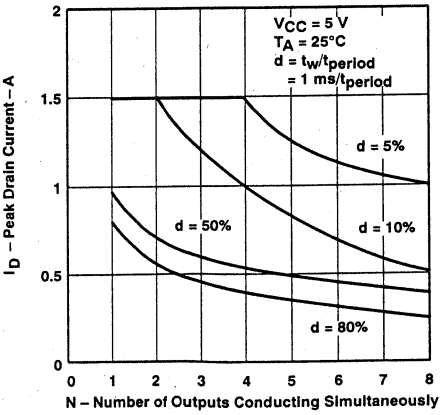


Figure 8

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

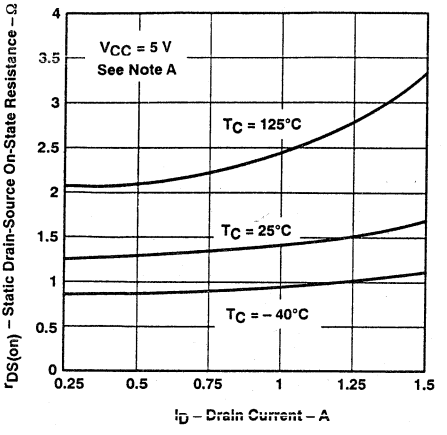


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

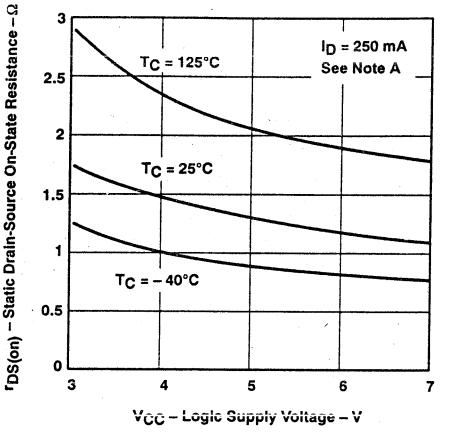


Figure 10

SWITCHING TIME vs TEMPERATURE

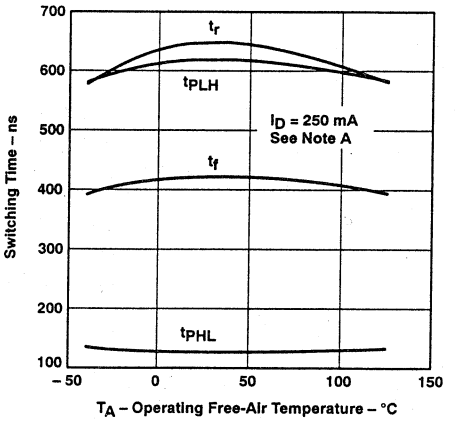


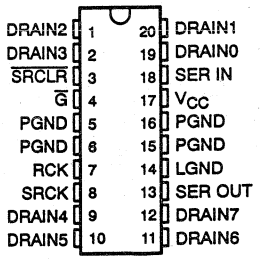
Figure 11

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

SLIS005 – D4075, APRIL 1993

- Low $r_{DS(on)}$ . . . 1 Ω Typical
- Output Short-Circuit Protection
- Avalanche Energy . . . 75 mJ
- Eight 350-mA DMOS Outputs
- 50-V Switching Capability
- Devices Are Cascadable
- Low Power Consumption

NE PACKAGE
(TOP VIEW)

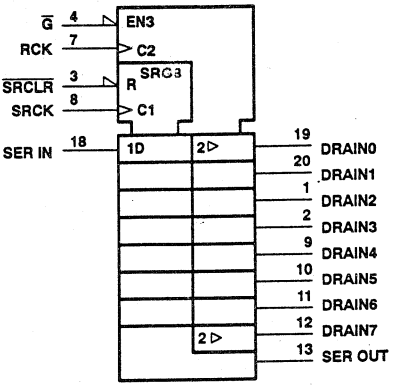


description

The TPIC6A595 is a monolithic, high-voltage, high-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{SRCLR}$) is high. When $\overline{SRCLR}$ is low, the input shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

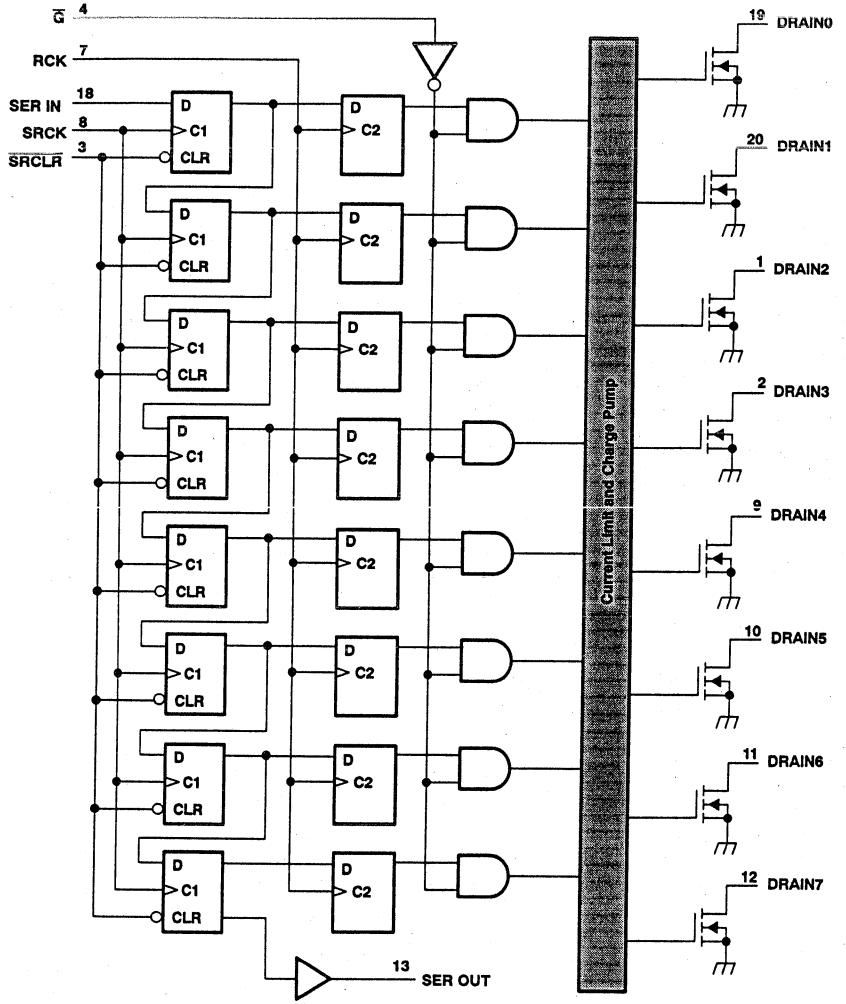
Outputs are low-side, open-drain DMOS transistors with output ratings of 50-V and 350-mA continuous sink current capability. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink current capability.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance.

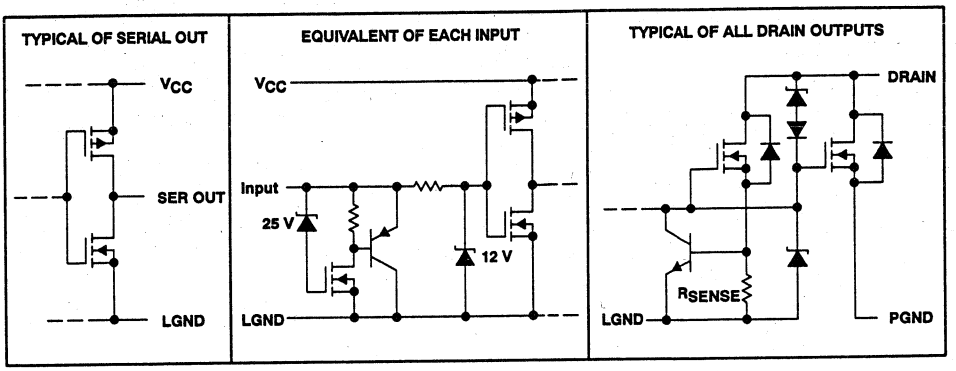
A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6A595 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current (see Note 3)	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	1.1 A
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	350 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	1.1 A
Single-pulse avalanche energy, E_{AS} (see Figure 6)	75 mJ
Avalanche current, I_{AS} (see Note 4)	600 mA
Continuous total dissipation at (or below) T_A = 25°C (see Note 5)	2.5 W
Continuous total dissipation at (or below) T_C = 100°C (see Note 5)	6 W
Operating case temperature range, T_C	−40°C to 125°C
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2 %.
4. V_{DD} = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 210 mH, I_{AS} = 600 mA. See Figure 6.
5. For operation above 25°C free-air temperature, derate linearly at the rate of 20 mW/°C. For operation above 100°C case temperature, derate linearly at the rate of 120 mW/°C. To avoid exceeding the design maximum junction temperature, this rating should not be exceeded.

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C (see Notes 3 and 6)	−1.8	0.6	A
Setup time, t_{su}, SER IN high before SRCK↑ (see Figure 2)	10		ns
Hold time, t_h, SER IN high after SRCK↑ (see Figure 2)	10		ns
Pulse duration, t_w (see Figure 2)	20		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics over recommended ranges of supply voltage and operating temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		50			V
V_{SD}	Source-drain diode forward voltage	I_F = 350 mA, See Note 3			0.8	1.1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = −20 μA		V_{CC}−0.1	V_{CC}		V
		I_{OH} = −4 mA		V_{CC}−0.5	V_{CC}−0.2		
V_{OL}	Low-level output voltage, SER OUT	I_{OL} = 20 μA			0	0.1	V
		I_{OL} = 4 mA			0.2	0.5	
I_{IH}	High-level input current	$V_I = V_{CC}$				1	μA
I_{IL}	Low-level input current	V_I = 0				−1	μA
I_{OK}	Output current at which chopping starts	T_C = 25°C, See Note 6 and Figures 3 and 4		0.6	0.8	1.1	A
I_{CC}	Logic supply current	I_O = 0, $V_I = V_{CC}$ or 0			0.5	5	mA
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, $V_I = V_{CC}$ or 0,	I_O = 0, V_{CC} = 5 V, C_L = 30 pF, See Figure 7		1.3		mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, V_{CC} = 5 V,	$I_N = I_D$, T_C = 85°C, See Notes 6, 7, and 8		350		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V,	T_C = 25°C		0.1	1	μA
		V_{DS} = 40 V,	T_C = 125°C		0.2	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 350 mA, T_C = 25°C	See Notes 6 and 7 and Figures 10 and 11		1	1.5	Ω
		I_D = 350 mA, T_C = 125°C			1.7	2.5	

† All typical values are at V_{CC} = 5 V, T_C = 25°C

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$	C_L = 30 pF, I_D = 350 mA, See Figures 1, 2, and 12		30		ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$			125		ns
t_r	Rise time, drain output			60		ns
t_f	Fall time, drain output			30		ns
t_a	Reverse-recovery-current rise time	I_F = 350 mA, di/dt = 20 A/μs, See Notes 6 and 7 and Figure 5		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 μs, duty cycle ≤ 2%.
6. Technique should limit $T_J - T_C$ to 10°C maximum.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
8. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at 85°C case temperature.

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	All 8 outputs with equal power		8.3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	All 8 outputs with equal power		50	°C/W

PARAMETER MEASUREMENT INFORMATION

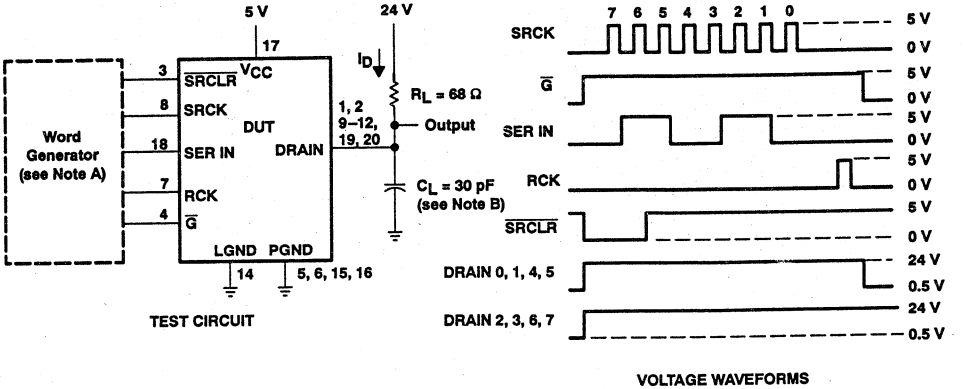


Figure 1. Resistive Load Operation

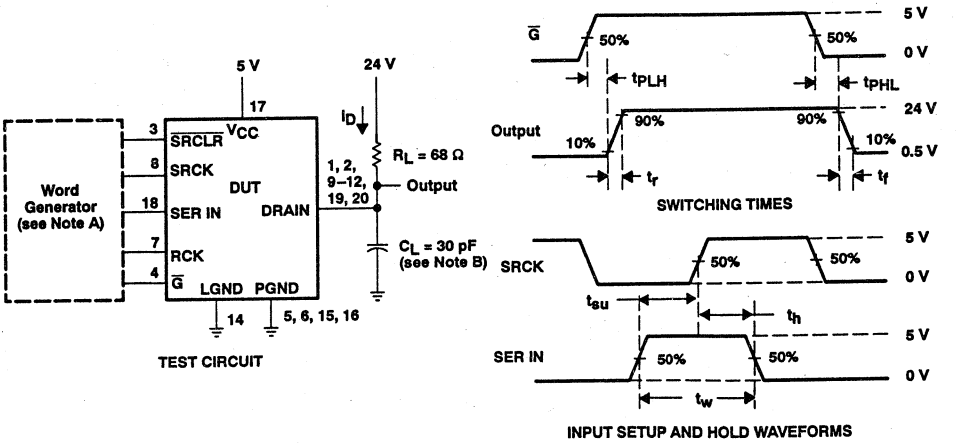
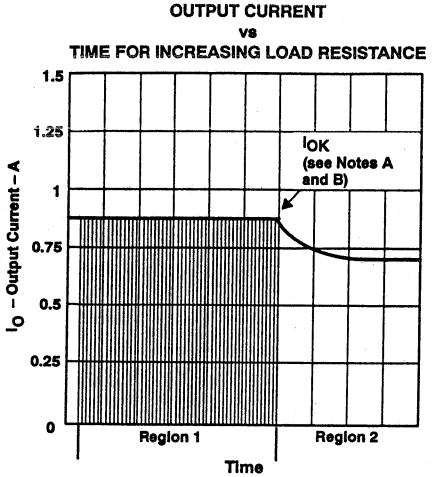
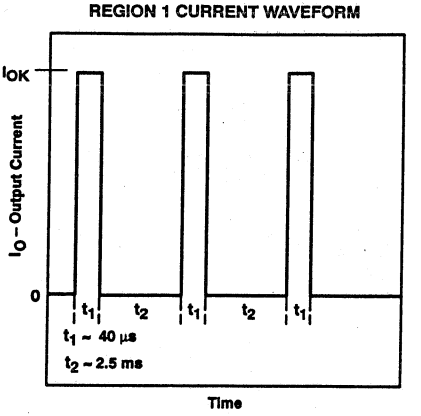


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION





First output current pulses after turn-on in chopping mode with resistive load.

NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK}. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.
B. Region 1 duty cycle is approximately 2%.

Figure 3. Chopping-Mode Characteristics

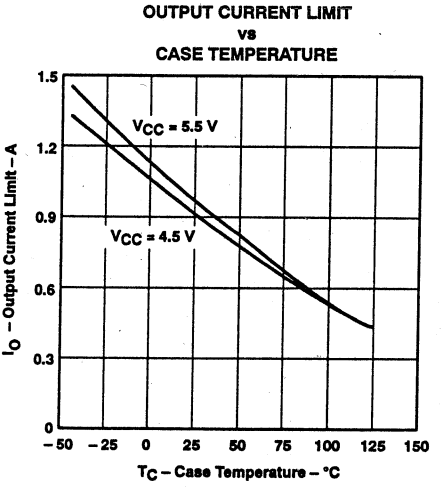
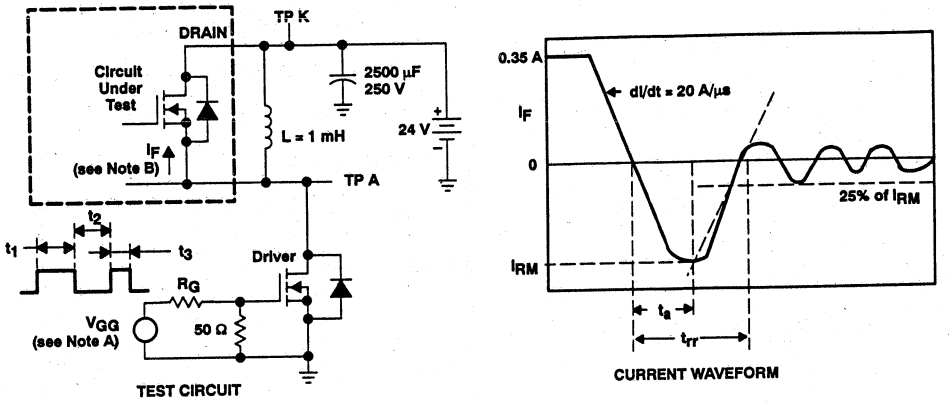


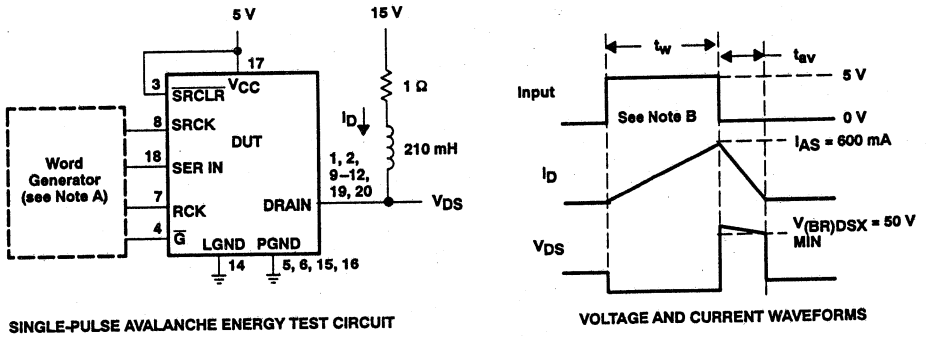
Figure 4. Output Current-Limit Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/μs. A V_{GG} double-pulse train is used to set I_F = 0.35 A, where t_1 = 10 μs, t_2 = 7 μs, and t_3 = 3 μs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, Z_O = 50 Ω.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 600 mA.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ.

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREQUENCY

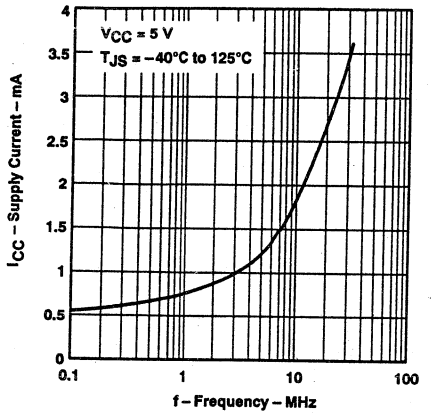


Figure 7

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

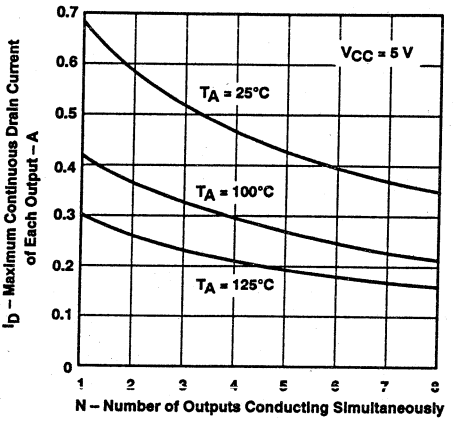


Figure 8

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

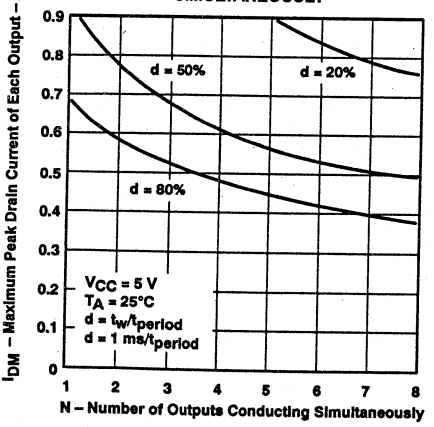
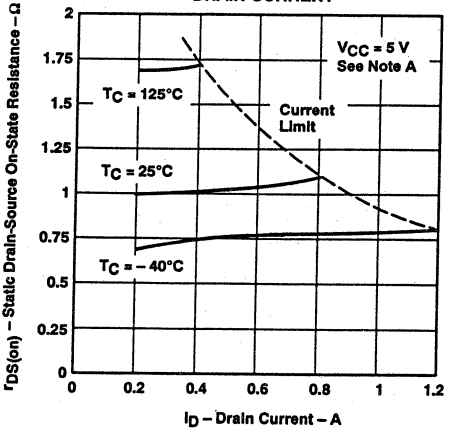


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT



NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 10

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

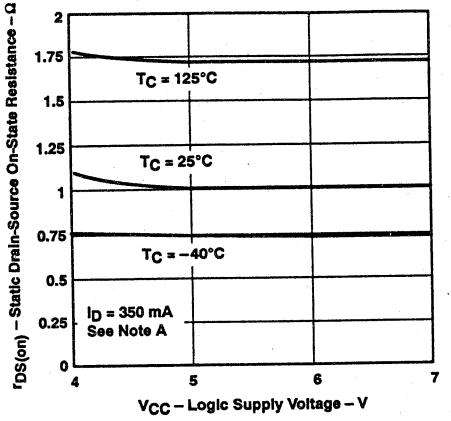


Figure 11

SWITCHING TIME vs TEMPERATURE

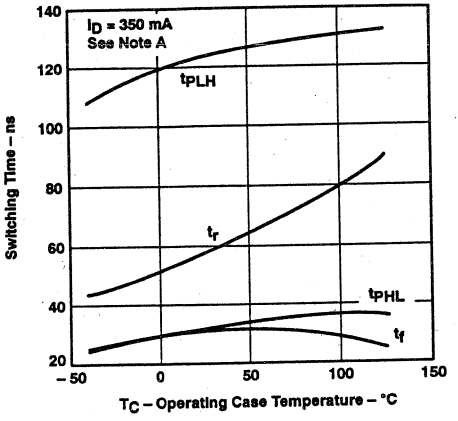


Figure 12

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

TRANSIENT THERMAL IMPEDANCE vs ON TIME

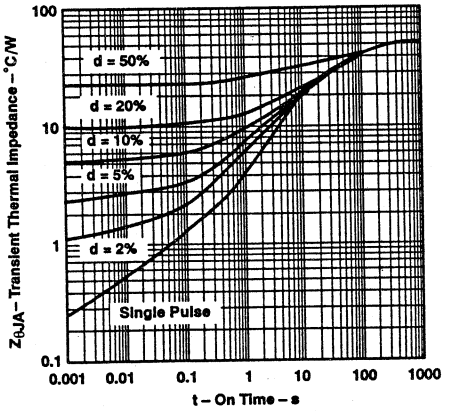


Figure 13

The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_{\theta(t_W + t_C)} + Z_{\theta(t_W)} - Z_{\theta(t_C)}$$

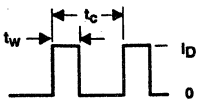
Where:

$Z_{\theta(t_w)}$ = the single-pulse thermal impedance for $t = t_w$ seconds

$Z_{\theta(t_c)}$ = the single-pulse thermal impedance for $t = t_c$ seconds

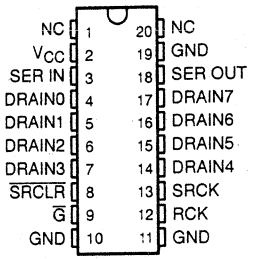
$Z_{\theta(t_w + t_c)}$ = the single-pulse thermal impedance for $t = t_w + t_c$ seconds

$d = t_w/t_c$



- Low $r_{DS(on)}$ . . . 5 Ω Typical
- Avalanche Energy . . . 30 mJ
- Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current
- 500-mA Typical Current-Limiting Capability
- Output Clamp Voltage . . . 50 V
- Devices Are Cascadable
- Low Power Consumption

DW OR N PACKAGE
(TOP VIEW)



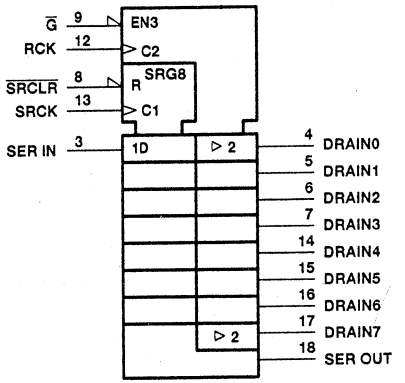
NC – No internal connection

description

The TPIC6B595 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{SRCLR}$) is high. When $\overline{SRCLR}$ is low, the input shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink-current capability. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

logic symbol†

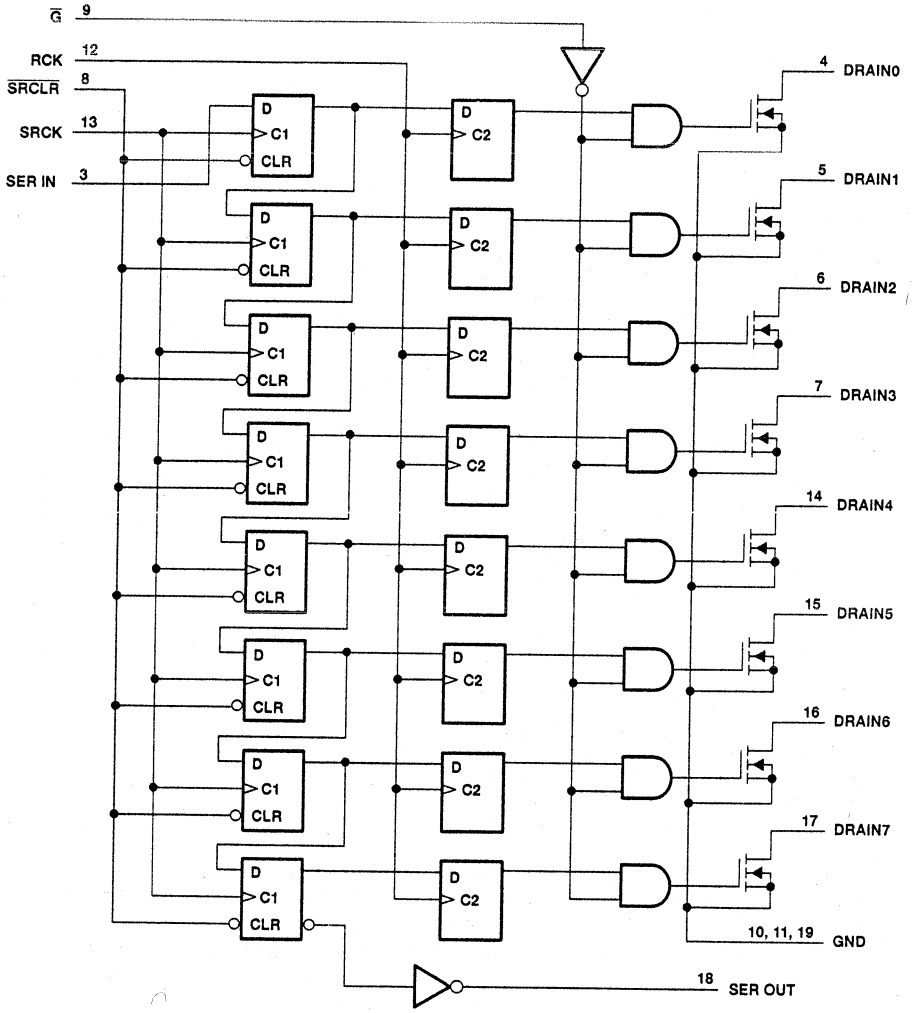


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

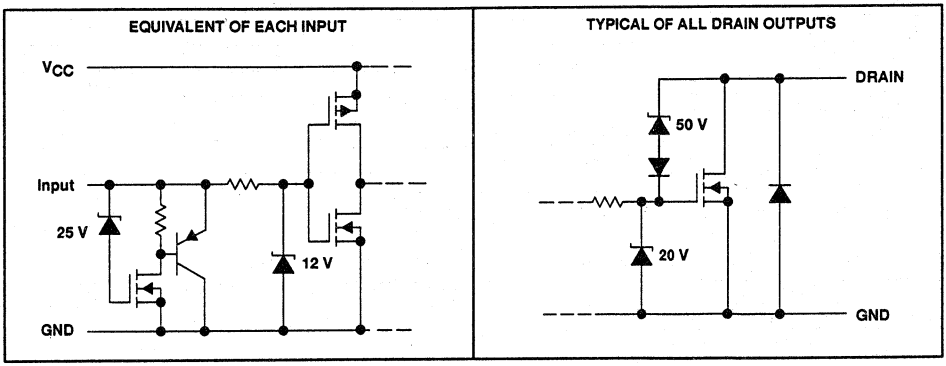
Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B595 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-to-drain diode anode current	500 mA
Pulsed source-to-drain diode anode current (see Note 3)	1 A
Pulsed drain current, each output, all outputs on, I_D, T_C = 25°C (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, I_D, T_C = 25°C	150 mA
Peak drain current single output, I_{DM}, T_C = 25°C (see Note 3)	500 mA
Single-pulse avalanche energy, E_{AS} (see Figure 4)	30 mJ
Avalanche current, I_{AS} (see Note 4)	500 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 200 mH, I_{AS} = 0.5 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	T_C ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−500	500	mA
Setup time, SER IN high before SRCK↑, t_{su} (see Figure 2)	20		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	20		ns
Pulse duration, t_w (see Figure 2)	40		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA		50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 100 mA			0.85	1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = −20 µA, V_{CC} = 4.5 V		4.4	4.49		V
		I_{OH} = −4 mA, V_{CC} = 4.5 V		4	4.2		
V_{OL}	Low-level output voltage, SER OUT	I_{OL} = 20 µA, V_{CC} = 4.5 V			0.005	0.1	V
		I_{OL} = 4 mA, V_{CC} = 4.5 V			0.3	0.5	
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				−1	µA
I_{CC}	Logic supply current	V_{CC} = 5.5 V	All outputs off		20	100	µA
			All outputs on		150	300	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, C_L = 30 pF, All outputs off,	See Figures 2 and 6		0.4	5	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, I_N = I_D, T_C = 85°C	See Notes 5, 6, and 7		90		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V, V_{CC} = 5.5 V			0.1	5	µA
		V_{DS} = 40 V, V_{CC} = 5.5 V, T_C = 125°C			0.15	8	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 100 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 7 and 8		4.2	5.7	Ω
		I_D = 100 mA, T_C = 125°C, V_{CC} = 4.5 V			6.8	9.5	
		I_D = 350 mA, V_{CC} = 4.5 V			5.5	8	

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

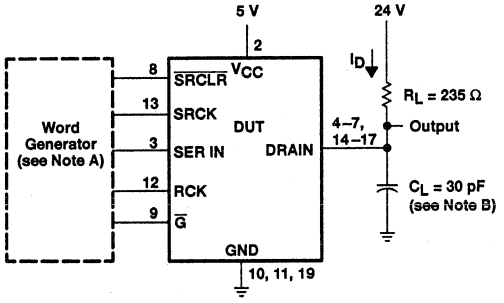
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 100 mA, See Figures 1, 2, and 9		150		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			90		ns
t_r	Rise time, drain output			200		ns
t_f	Fall time, drain output			200		ns
t_a	Reverse-recovery-current rise time	I_F = 100 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

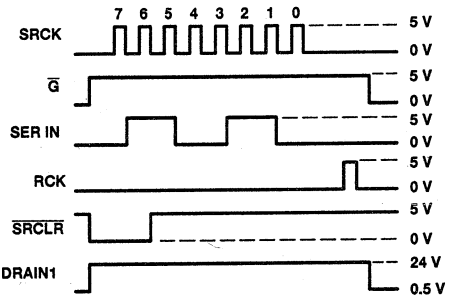
thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		90	°C/W
		N package			95	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

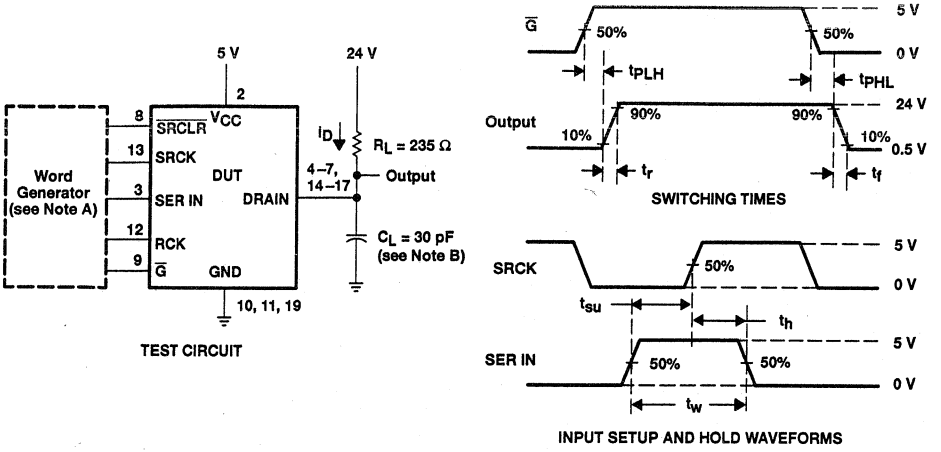


VOLTAGE WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, t_w = 300 ns, pulsed repetition rate (PRR) = 5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

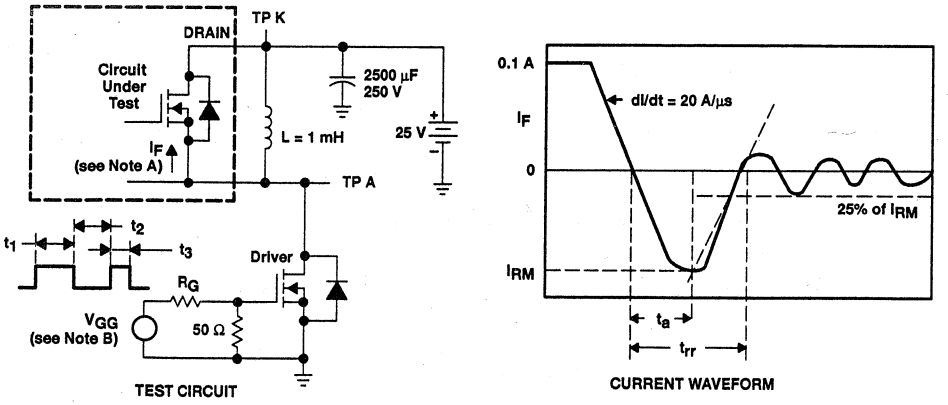
Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

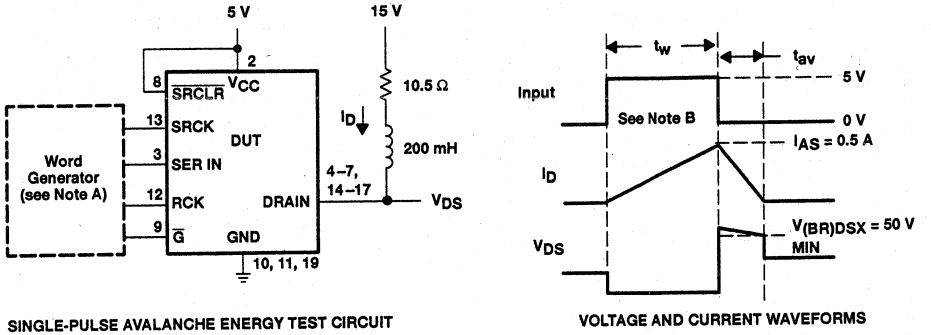
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms



NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
B. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/μs. A V_{GG} double-pulse train is used to set $I_F = 0.1$ A, where $t_1 = 10$ μs, $t_2 = 7$ μs, and $t_3 = 3$ μs.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$
B. Input pulse duration, t_w, is increased until peak current $I_{AS} = 0.5$ A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

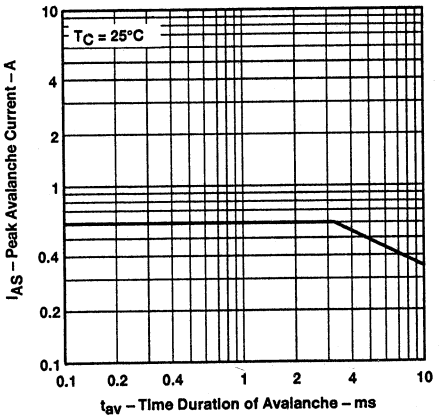


Figure 5

SUPPLY CURRENT
vs
FREQUENCY

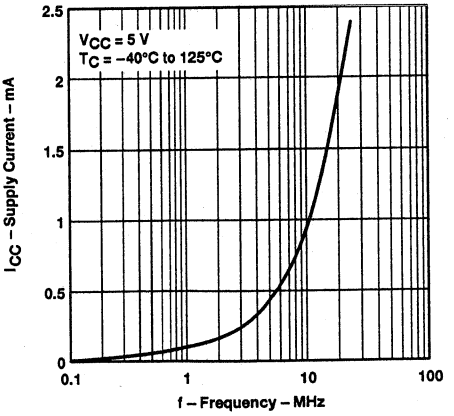


Figure 6

TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

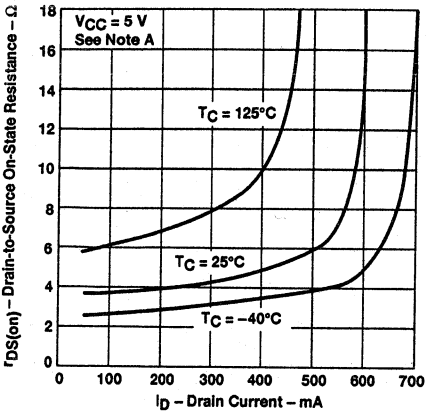


Figure 7

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
LOGIC SUPPLY VOLTAGE

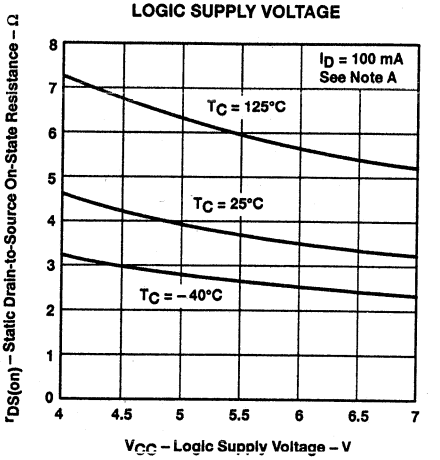


Figure 8

SWITCHING TIME
vs
CASE TEMPERATURE

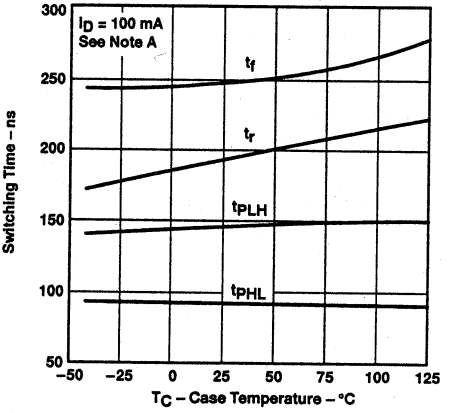


Figure 9

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

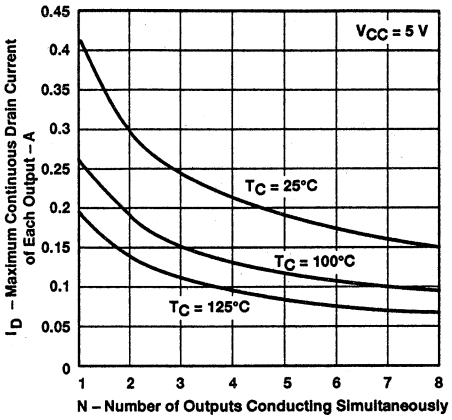


Figure 10

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

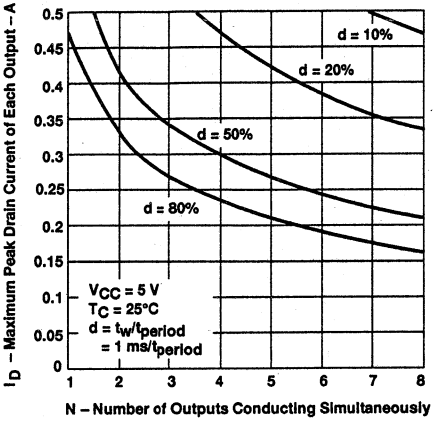
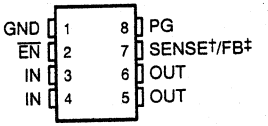


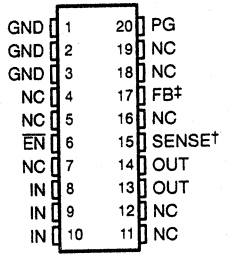
Figure 11

- **Available in 5-V, 4.85-V, and 3.3-V Fixed-Output and Adjustable Versions**
- **Very Low-Dropout Voltage . . . Maximum of 32 mV at I_O = 100 mA (TPS7150)**
- **Very Low Quiescent Current – Independent of Load . . . 285 μA Typ**
- **Extremely Low Sleep-State Current 0.5 μA Max**
- **2% Tolerance Over Full Range of Load, Line, and Temperature for Fixed-Output Versions**
- **Output Current Range of 0 mA to 500 mA**
- **TSSOP Package Option Offers Reduced Component Height for Critical Applications**
- **Power Good (PG) Status Output**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



NC – No internal connection
† SENSE – Fixed voltage options only (TPS7133, TPS7148, and TPS7150)
‡ FB – Adjustable version only (TPS7101)

description

The TPS71xx integrated circuits are a family of micropower low-dropout (LDO) voltage regulators. An order of magnitude reduction in dropout voltage and quiescent current over conventional LDO performance is achieved by replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 32 mV at an output current of 100 mA for the TPS7150) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and remains independent of output loading (typically 285 μA over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. The LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ ($\overline{enable}$) shuts down the regulator, reducing the quiescent current to 0.5 μA maximum at T_J = 25°C.

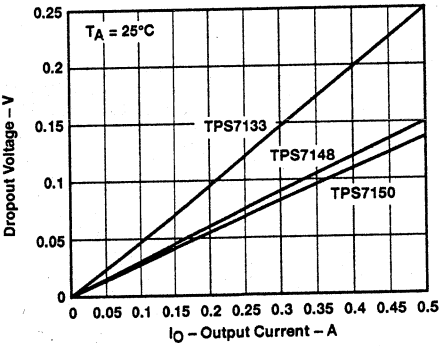


Figure 1. Dropout Voltage Versus Output Current

Power good (PG) reports low output voltage and can be used to implement a power-on reset or a low-battery indicator.

The TPS71xx is offered in 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version). The TPS71xx family is available in PDIP (8 pin), SO (8 pin), and TSSOP (20 pin) packages. The TSSOP has a maximum height of 1.2 mm.

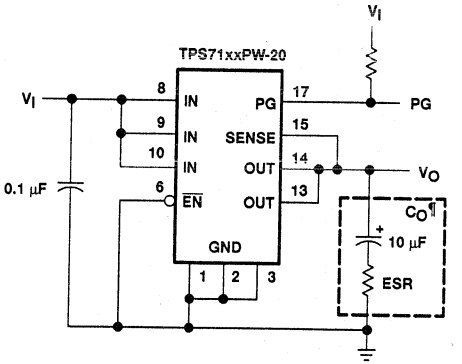
AVAILABLE OPTIONS

PART NUMBER	OUTPUT VOLTAGE			UNIT
	MIN	TYP	MAX	
TPS7150QPWLE†	4.9	5	5.1	V
TPS7150QD‡				
TPS7150QP				
TPS7148QPWLE†	4.75	4.85	4.95	V
TPS7148QD‡				
TPS7148QP				
TPS7133QPWLE†	3.23	3.3	3.37	V
TPS7133QD‡				
TPS7133QP				
TPS7101QPWLE†	Adjustable§ 1.2 V to 9.75 V			V
TPS7101QD‡				
TPS7101QP				

† The PW package is only available left-end taped and reeled.

‡ The D package is available taped and reeled. Add R suffix to device type (e.g., TPS7150QDR).

§ The TPS7101Q is programmable using an external resistor divider (see application information).



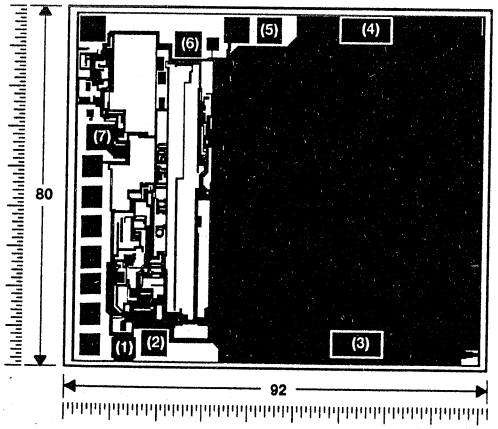
¶ Capacitor selection is nontrivial. See application information section for details.

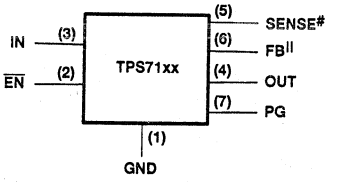
Figure 2. Typical Application Configuration

TPS71xx chip information

Thermal compression or ultrasonic bonding can be used on the doped-aluminum bonding pad. Chips can be mounted with conductive epoxy or a gold-silicon preform. Contact factory for die sales.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

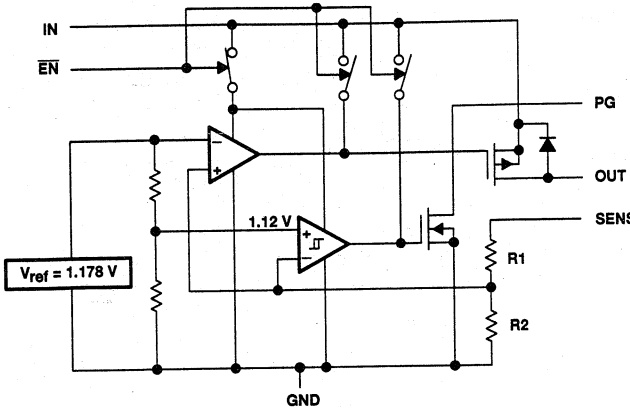
ALL DIMENSIONS ARE IN MILS.

SENSE – Fixed voltage options only (TPS7133, TPS7148, and TPS7150)

|| FB – Adjustable version only (TPS7101)

NOTE: For most applications, OUT and SENSE should be tied together as close as possible to the device; for other implementations, refer to SENSE-pin connection discussion in the applications information section of this data sheet.

functional block diagram



RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS7101	0	∞	Ω
TPS7133	420	233	kΩ
TPS7148	726	233	kΩ
TPS7150	756	233	kΩ

NOTE: Resistors are nominal values only.

† For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to SENSE-pin connection discussion in applications information section.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Input voltage range§, V_I, PG, SENSE, $\overline{EN}$ ..... −0.3 to 10 V
Output current, I_O ..... 2 A
Continuous total power dissipation ..... See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J ..... −55°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
§ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
P	1175 mW	9.4 mW/°C	752 mW	235 mW
PW¶	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING	$T_C = 125°C$ POWER RATING
D	2188 mW	17.5 mW/°C	1400 mW	438 mW
P	2738 mW	21.9 mW/°C	1752 mW	548 mW
PW¶	4025 mW	32.2 mW/°C	2576 mW	805 mW

¶ Refer to thermal information section for detailed power dissipation considerations when using the TSSOP package.

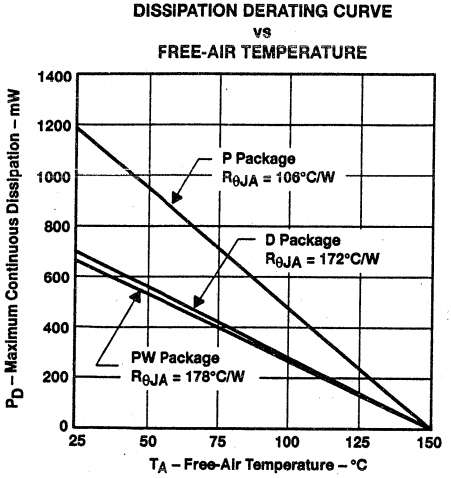


Figure 3

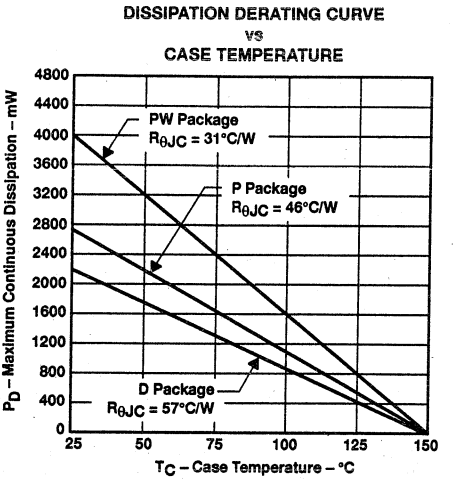


Figure 4

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I†	TPS7101Q	2.5	10	V
	TPS7133Q	3.77	10	
	TPS7148Q	5.2	10	
	TPS7150Q	5.33	10	
High-level input voltage at $\overline{EN}$, V_{IH}		2		V
Low-level input voltage at $\overline{EN}$, V_{IL}			0.5	V
Output current range, I_O		0	500	mA
Operating virtual junction temperature range, T_J		–40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for your maximum output current, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

Because the TPS7101 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 2 in the electrical characteristics table. The minimum value of 2.5 V is the absolute lower limit for the recommended input voltage range for the TPS7101.

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 µF/ESR† = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T_J	MIN	TYP	MAX	UNIT
Ground current (active mode)	$\overline{EN} \le 0.5$ V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 500 mA	25°C		285	350	µA
		−40°C to 125°C			460	
Input current (standby mode)	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	µA
		−40°C to 125°C			2	
Output current limit	V_O = 0 V, V_I = 10 V	25°C		1.2	2	A
		−40°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	µA
		−40°C to 125°C			1	
PG leakage current	Normal operation, V_{PG} = 10 V	25°C		0.02	0.5	µA
		−40°C to 125°C			0.5	
Output voltage temperature coefficient		−40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{EN}$ logic high (standby mode)	2.5 V ≤ V_I ≤ 6 V	−40°C to 125°C	2			V
	6 V ≤ V_I ≤ 10 V		2.7			
$\overline{EN}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V	25°C			0.5	V
		−40°C to 125°C			0.5	
$\overline{EN}$ hysteresis voltage		25°C		50		mV
$\overline{EN}$ input current	0 V ≤ V_I ≤ 10 V	25°C	−0.5		0.5	µA
		−40°C to 125°C	−0.5		0.5	
Minimum V_I for active pass element		25°C		2.05	2.5	V
		−40°C to 125°C			2.5	
Minimum V_I for valid PG	I_{PG} = 300 µA	25°C		1.06	1.5	V
		−40°C to 125°C			1.9	

† ESR refers to the equivalent resistance, including internal resistance and series resistance.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7101Q electrical characteristics at I_O = 10 mA, V_I = 3.5 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF/ESR† = 1 Ω, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V, I_O = 10 mA		25°C		1.178		V
	2.5 V ≤ V_I ≤ 10 V, 5 mA ≤ I_O ≤ 500 mA, See Note 1		−40°C to 125°C	1.143		1.213	V
Reference voltage temperature coefficient			−40°C to 125°C		61	75	ppm/°C
Pass-element series resistance (see Note 2)	V_I = 2.4 V, 50 µA ≤ I_O ≤ 150 mA		25°C		0.7	1	Ω
			−40°C to 125°C			1	
	V_I = 2.4 V, 150 mA ≤ I_O ≤ 500 mA		25°C		0.83	1.3	
			−40°C to 125°C			1.3	
	V_I = 2.9 V, 50 µA ≤ I_O ≤ 500 mA		25°C		0.52	0.85	
			−40°C to 125°C			0.85	
	V_I = 3.9 V, 50 µA ≤ I_O ≤ 500 mA		25°C		0.32		
	V_I = 5.9 V, 50 µA ≤ I_O ≤ 500 mA		25°C		0.23		
Input regulation	V_I = 2.5 V to 10 V, 50 µA ≤ I_O ≤ 500 mA, See Note 1		25°C			18	mV
			−40°C to 125°C			25	
Output regulation	I_O = 5 mA to 500 mA, 2.5 V ≤ V_I ≤ 10 V, See Note 1		25°C			14	mV
			−40°C to 125°C			25	
	I_O = 50 µA to 500 mA, 2.5 V ≤ V_I ≤ 10 V, See Note 1		25°C			22	mV
			−40°C to 125°C			54	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	48	59		dB
			−40°C to 125°C	44			
		I_O = 500 mA, See Note 1	25°C	45	54		
			−40°C to 125°C	44			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 µF	25°C		95		µVrms
		C_O = 10 µF	25°C		89		
		C_O = 100 µF	25°C		74		
PG trip-threshold voltage§	V_{FB} voltage decreasing from above V_{PG}		−40°C to 125°C	0.92 × $V_{FB(nom)}$		0.98 × $V_{FB(nom)}$	V
PG hysteresis voltage§	Measured at V_{FB}		25°C		12		mV
PG output low voltage§	I_{PG} = 400 µA, V_I = 2.13 V		25°C		0.1	0.4	V
			−40°C to 125°C			0.4	
FB input current			25°C	−10	0.1	10	nA
			−40°C to 125°C	−20		20	

† ESR refers to the equivalent resistance including internal resistance and series resistance.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.
§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When V_I < 2.9 V and I_O > 150 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 31) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figure 30.

TPS7133Q electrical characteristics at I_O = 10 mA, V_I = 4.3 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF/ESR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
Output voltage	V_I = 4.3 V,	I_O = 10 mA	25°C		3.3		V
	4.3 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	–40°C to 125°C	3.23		3.37	
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V	25°C		0.02	6	mV
			–40°C to 125°C			8	
	I_O = 100 mA,	V_I = 3.23 V	25°C		47	60	
			–40°C to 125°C			80	
	I_O = 500 mA,	V_I = 3.23 V	25°C		235	300	
			–40°C to 125°C			400	
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 500 mA	V_I = 3.23 V,	25°C		0.47	0.6	Ω
			–40°C to 125°C			0.8	
Input regulation	V_I = 4.3 V to 10 V,	50 µA ≤ I_O ≤ 500 mA	25°C			20	mV
			–40°C to 125°C			27	
Output regulation	I_O = 5 mA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		21	38	mV
			–40°C to 125°C			75	
	I_O = 50 µA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		30	60	mV
			–40°C to 125°C			120	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	43	54		dB
			–40°C to 125°C	40			
		I_O = 500 mA	25°C	39	49		
			–40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 µF	25°C		274		µVrms
		C_O = 10 µF	25°C		228		
		C_O = 100 µF	25°C		159		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C	0.92 × $V_{O(nom)}$		0.98 × $V_{O(nom)}$	V
PG hysteresis voltage			25°C		35		mV
PG output low voltage	I_{PG} = 1 mA,	V_I = 2.8 V	25°C		0.22	0.4	V
			–40°C to 125°C			0.4	

† ESR refers to the equivalent resistance including internal resistance and series resistance.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7148Q electrical characteristics at I_O = 10 mA, V_I = 5.85 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF/ESR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
Output voltage	V_I = 5.85 V,	I_O = 10 mA	25°C		4.85		V
	5.85 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	−40°C to 125°C	4.75		4.95	
Dropout voltage	I_O = 10 mA,	V_I = 4.75 V	25°C		0.08	6	mV
			−40°C to 125°C			8	
	I_O = 100 mA,	V_I = 4.75 V	25°C		30	37	
			−40°C to 125°C			54	
	I_O = 500 mA,	V_I = 4.75 V	25°C		150	180	
			−40°C to 125°C			250	
Pass-element series resistance	(4.75 V − V_O)/I_O, I_O = 500 mA	V_I = 4.75 V,	25°C		0.32	0.35	Ω
			−40°C to 125°C			0.52	
Input regulation	V_I = 5.85 V to 10 V,	50 µA ≤ I_O ≤ 500 mA	25°C			27	mV
			−40°C to 125°C			37	
Output regulation	I_O = 5 mA to 500 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		12	42	mV
			−40°C to 125°C			80	
	I_O = 50 µA to 500 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		42	60	mV
			−40°C to 125°C			130	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	42	53		dB
			−40°C to 125°C	39			
		I_O = 500 mA	25°C	39	50		
			−40°C to 125°C	35			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 µF	25°C		410		µVrms
		C_O = 10 µF	25°C		328		
		C_O = 100 µF	25°C		212		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C	0.92 × $V_{O(nom)}$		0.98 × $V_{O(nom)}$	V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 4.12 V	25°C		0.2	0.4	V
			−40°C to 125°C			0.4	

† ESR refers to the equivalent resistance including internal resistance and series resistance.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7150Q electrical characteristics at I_O = 10 mA, V_I = 6 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF/ESR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V,	I_O = 10 mA	25°C		5		V
	6 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	–40°C to 125°C	4.9		5.1	
Dropout voltage	I_O = 10 mA,	V_I = 4.88 V	25°C		0.13	6	mV
			–40°C to 125°C			8	
	I_O = 100 mA,	V_I = 4.88 V	25°C		27	32	
			–40°C to 125°C			47	
	I_O = 500 µA,	V_I = 4.88 V	25°C		146	170	
			–40°C to 125°C			230	
Pass-element series resistance	(4.88 V – V_O)/I_O, I_O = 500 mA	V_I = 4.88 V.	25°C		0.29	0.32	Ω
			–40°C to 125°C			0.47	
Input regulation	V_I = 6 V to 10 V,	50 µA ≤ I_O ≤ 500 mA	25°C			25	mV
			–40°C to 125°C			32	
Output regulation	I_O = 5 mA to 500 mA,	6 V ≤ V_I ≤ 10 V	25°C		30	45	mV
			–40°C to 125°C			86	
	I_O = 50 µA to 500 mA,	6 V ≤ V_I ≤ 10 V	25°C		45	65	mV
			–40°C to 125°C			140	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	45	55		dB
			–40°C to 125°C	40			
		I_O = 500 mA	25°C	42	52		
			–40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 µF	25°C		430		µVrms
		C_O = 10 µF	25°C		345		
		C_O = 100 µF	25°C		220		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C	0.92 × $V_{O(nom)}$		0.98 × $V_{O(nom)}$	V
PG hysteresis voltage			25°C		53		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 4.25 V	25°C		0.2	0.4	V
			–40°C to 125°C			0.4	

† ESR refers to the equivalent resistance including internal resistance and series resistance.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

THERMAL INFORMATION

In response to system-miniaturization trends, integrated circuits are being offered in low-profile and fine-pitch surface-mount packages. Implementation of many of today's high-performance devices in these packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are illustrated in this discussion:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

Figure 5 is an example of a thermally enhanced PWB layout for the 20-lead TSSOP package. This layout involves adding copper on the PWB to conduct heat away from the device. The $R_{\theta JA}$ for this component/board system is illustrated in Figure 6. The family of curves illustrates the effect of increasing the size of the copper-heat-sink surface area. The PWB is a standard FR4 board (L × W × H = 3.2 inch × 3.2 inch × 0.062 inch); the board traces and heat sink area are 1-oz (per square foot) copper.

Figure 7 shows the thermal resistance for the same system with the addition of a thermally conductive compound between the body of the TSSOP package and the PWB copper routed directly beneath the device. The thermal conductivity for the compound used in this analysis is 0.815 W/m · °C.

Using these figures to determine the system $R_{\theta JA}$ allows the maximum power-dissipation limit to be calculated with the equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}}$$

Where

$T_{J(max)}$ is the maximum allowable junction temperature or 125°C.

This limit should then be applied to the internal power dissipated by the TPS71xx regulator. The equation for calculating total internal power dissipation of the TPS71xx is:

$$P_{D(total)} = (V_I - V_O) \cdot I_O + V_I \cdot I_Q$$

Because the quiescent current of the TPS71xx family is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = (V_I - V_O) \cdot I_O$$

For a 20-lead TSSOP/FR4 board system with thermally conductive compound between the board and the device body, where T_A = 55°C, airflow = 100 ft/min, copper heat sink area = 1 cm^2, the maximum power-dissipation limit can be calculated. As indicated in Figure 7, the system $R_{\theta JA}$ is 94°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}} = \frac{125°C - 55°C}{94°C/W} = 745 \text{ mW}$$

If the system implements a TPS7148 regulator where V_I = 6 V and I_O = 385 mA, the internal power dissipation is:

$$P_{D(total)} = (V_I - V_O) \cdot I_O = (6 - 4.85) \cdot 0.385 = 443 \text{ mW}$$

THERMAL INFORMATION

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the maximum limit. When it does, one of two corrective actions can be taken. The power-dissipation limit can be raised by increasing the airflow or the heat-sink area. Alternatively, the internal power dissipation of the regulator can be lowered by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

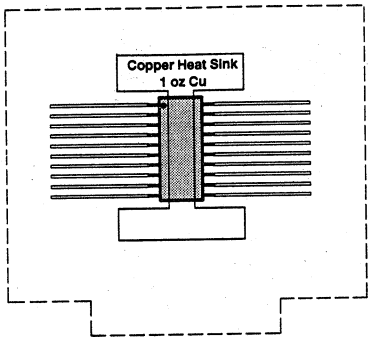


Figure 5. Thermally Enhanced PWB Layout (not to scale) for the 20-Pin TSSOP

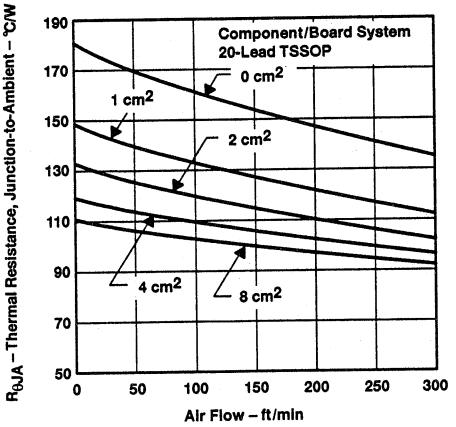


Figure 6

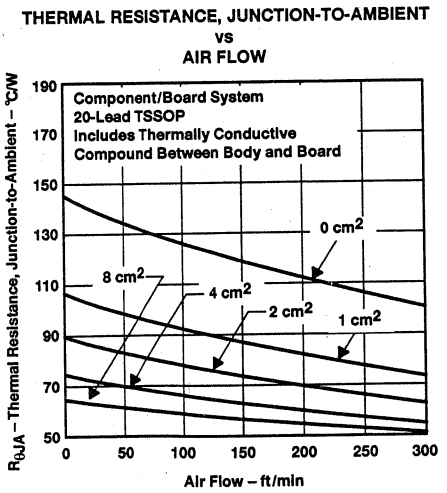


Figure 7

APPLICATION INFORMATION

The TPS71xx series of low-dropout (LDO) regulators is designed to overcome many of the shortcomings of earlier-generation LDOs, while adding features such as a power-saving shutdown mode and a power-good indicator. The TPS71xx family includes three fixed-output voltage regulators: the TPS7133 (3.3 V), the TPS7148 (4.85 V), and the TPS7150 (5 V). The family also offers an adjustable device, the TPS7101 (adjustable from 1.2 V to 9.75 V).

device operation

The TPS71xx, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that those devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent-current versus load-current curves. The TPS71xx uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS71xx specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS71xx quiescent current remains low even when the regulator drops out, eliminating both problems.

Included in the TPS71xx family is a 4.85-V regulator, the TPS7148. Designed specifically for 5-V cellular systems, its 4.85-V output, regulated to within ± 2%, allows for operation within the low-end limit of 5-V systems specified to ± 5% tolerance; therefore, maximum regulated operating lifetime is obtained from a battery pack before the device drops out, adding crucial talk minutes between charges.

The TPS71xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2 μA. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 μs.

minimum load requirements

The TPS71xx family is stable even at zero load; no minimum load is required for operation.

sense-pin connection

The SENSE pin of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047-pF to 0.1-μF) improves load transient response and noise rejection if the TPS71xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

APPLICATION INFORMATION

external capacitor requirements (continued)

As with most LDO regulators, the TPS71xx family requires an output capacitor for stability. A low-ESR 10-µF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 8). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to −40°C). Where component height and/or mounting area is a problem, physically smaller, 10-µF devices can be screened for ESR. Figures 39 through 46 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 µF), the output capacitance can be reduced to 4.7 µF, provided ESR is maintained between 0.7 and 2.5 Ω. Because minimum capacitor ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As show in the ESR graphs (Figures 39 through 46), minimum ESR is not a problem when using 10-µF or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS71xx family. This information (along with the ESR graphs, Figures 39 through 46) is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

All load and temperature conditions with up to 1 µF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 µF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 µF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 µF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 µF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 µF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 µF, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 µF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 µF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 µF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 µF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 µF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 µF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.

APPLICATION INFORMATION

external capacitor requirements (continued)

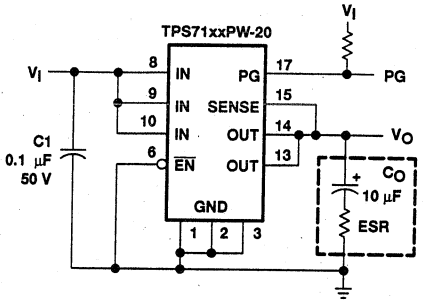


Figure 8. Typical Application Circuit

programming the TPS7101 adjustable LDO regulator

Programming the adjustable regulators is accomplished using an external resistor divider as shown in Figure 9. The equation governing the output voltage is:

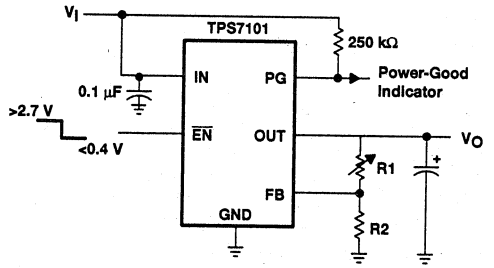
$$V_O = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where

V_{ref} = reference voltage, 1.178 V typ

Resistors R1 and R2 should be chosen for approximately 7-µA divider current. A recommended value for R2 is 169 kΩ with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving equation 1 for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \cdot R2 \quad (2)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	191	169	kΩ
3.3 V	309	169	kΩ
3.6 V	348	169	kΩ
4 V	402	169	kΩ
5 V	549	169	kΩ
6.4 V	750	169	kΩ

Figure 9. TPS7101 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

power-good indicator

The TPS71xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or as a low-battery indicator. PG does not assert itself when the regulated output voltage falls out of the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

regulator protection

The TPS71xx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS71xx also features internal current limiting and thermal protection. During normal operation, the TPS71xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_Q	Quiescent current	vs Output current	10
		vs Input voltage	11
		vs Free-air temperature	12
V_{DO}	Dropout voltage	vs Output current	13
ΔV_{DO}	Change in dropout voltage	vs Free-air temperature	14
ΔV_O	Change in output voltage	vs Free-air temperature	15
V_O	Output voltage	vs Input voltage	16
ΔV_O	Change in output voltage	vs Input voltage	17
V_O	Output voltage	vs Output current	18
			19
			20
			21
	Ripple rejection	vs Frequency	22
			23
			24
			25
	Noise	vs Frequency	26
			27
			28
			29
$r_{DS(on)}$	Pass-element resistance	vs Input voltage	30
R	Divider resistance	vs Free-air temperature	31
$I_{I(SENSE)}$	SENSE current	vs Free-air temperature	32
	FB leakage current	vs Free-air temperature	33
V_I	Minimum input voltage for active-pass element	vs Free-air temperature	34
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$I_{I(EN)}$	Input current (EN)	vs Free-air temperature	36
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V_{PG}	Power-good (PG) voltage	vs Output voltage	38
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			40
	ESR total equivalent resistance	vs Ceramic capacitance	41
			42
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			44
	ESR total equivalent resistance	vs Ceramic capacitance	45
			46

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT
vs
OUTPUT CURRENT

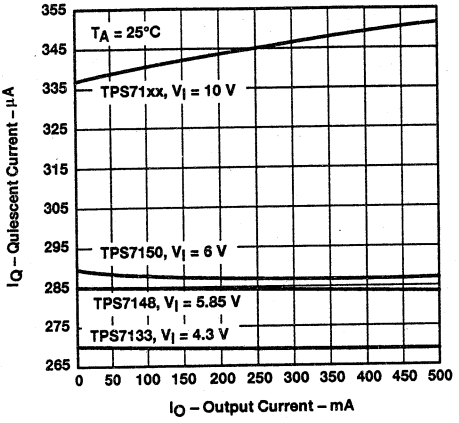


Figure 10

QUIESCENT CURRENT
vs
INPUT VOLTAGE

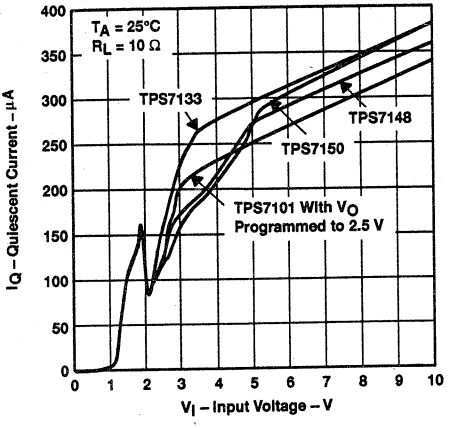


Figure 11

TPS7148Q
QUIESCENT CURRENT
vs
FREE-AIR TEMPERATURE

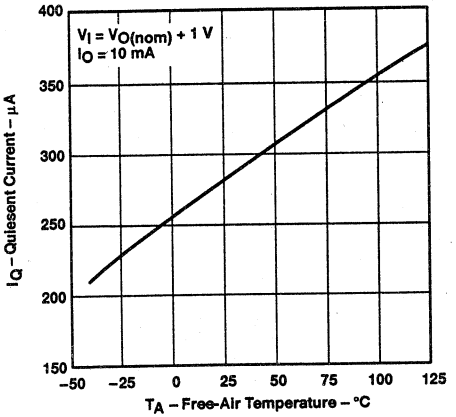


Figure 12

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

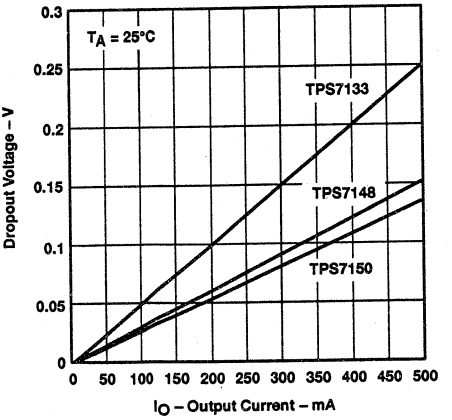


Figure 13

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

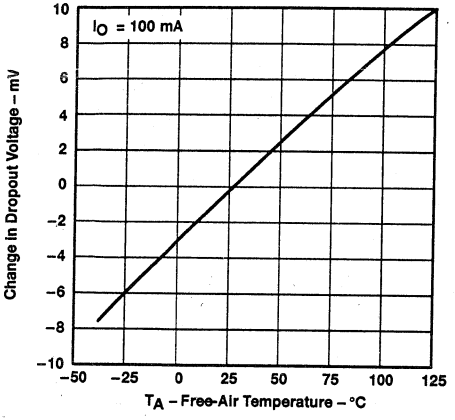


Figure 14

CHANGE IN OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

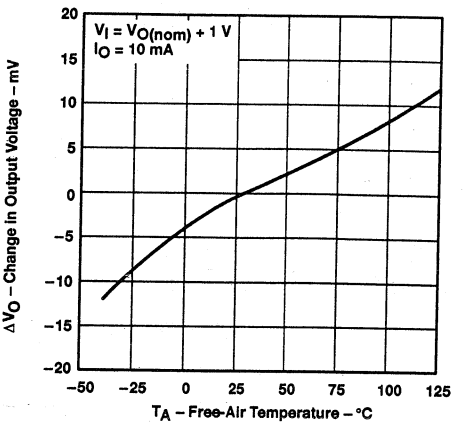


Figure 15

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

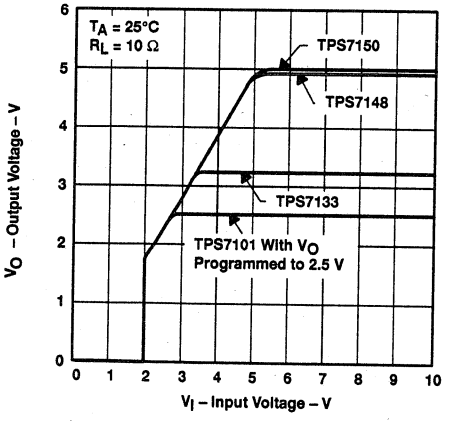


Figure 16

CHANGE IN OUTPUT VOLTAGE
vs
INPUT VOLTAGE

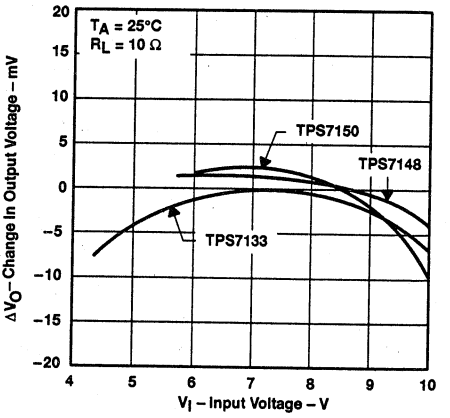


Figure 17

TYPICAL CHARACTERISTICS

TPS7101Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

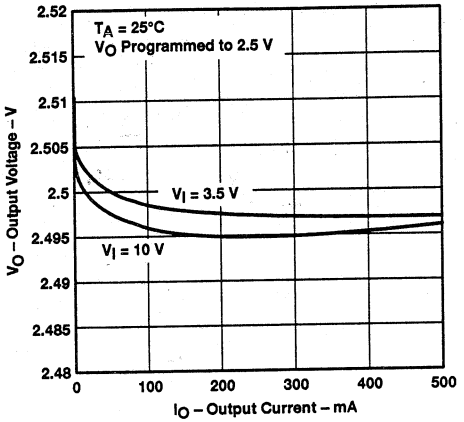


Figure 18

TPS7133Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

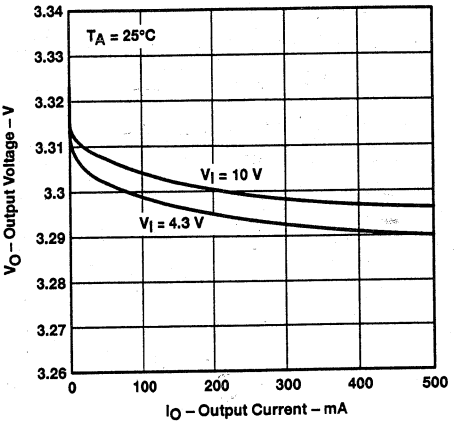


Figure 19

TPS7148Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

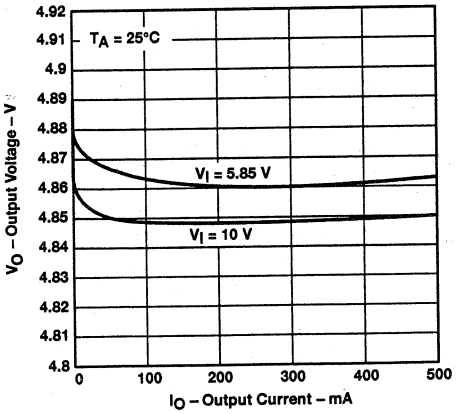


Figure 20

TPS7150Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

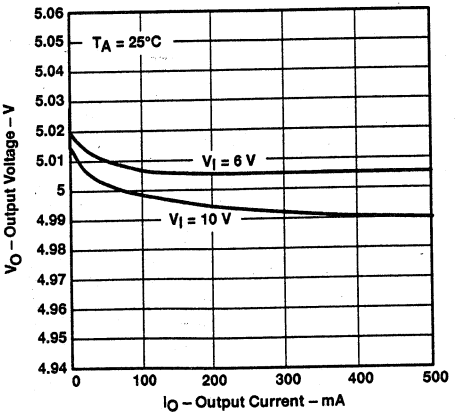


Figure 21

TYPICAL CHARACTERISTICS

TPS7101Q
RIPPLE REJECTION
vs
FREQUENCY

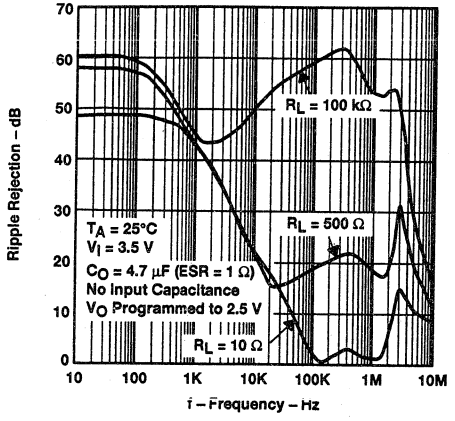


Figure 22

TPS7133Q
RIPPLE REJECTION
vs
FREQUENCY

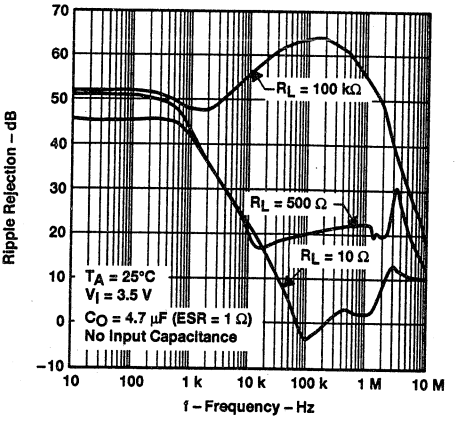


Figure 23

TPS7148Q
RIPPLE REJECTION
vs
FREQUENCY

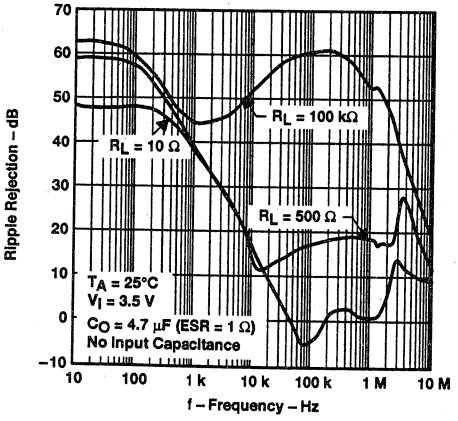


Figure 24

TPS7150Q
RIPPLE REJECTION
vs
FREQUENCY

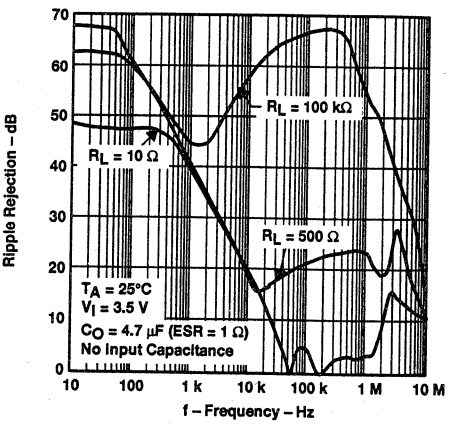


Figure 25

TYPICAL CHARACTERISTICS

TPS7101Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

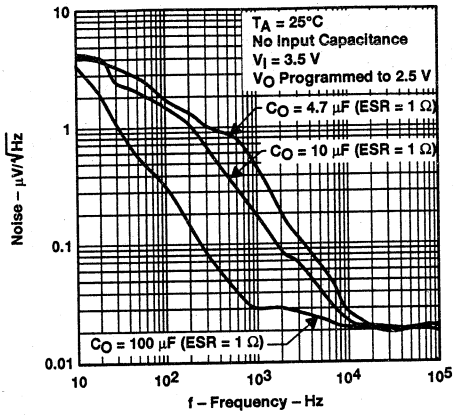


Figure 26

TPS7133Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

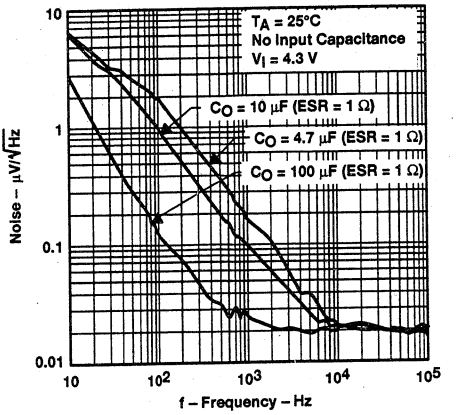


Figure 27

TPS7148Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

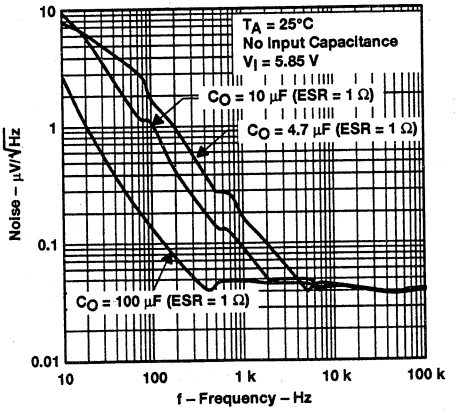


Figure 28

TPS7150Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

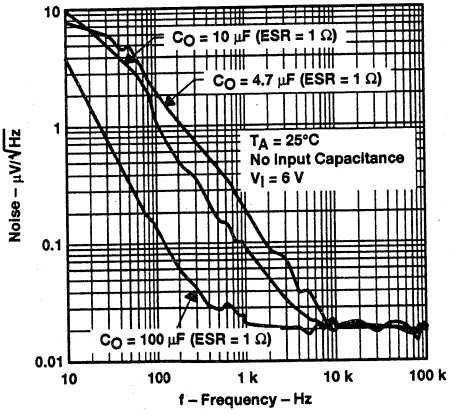


Figure 29

TYPICAL CHARACTERISTICS

PASS-ELEMENT RESISTANCE
vs
INPUT VOLTAGE

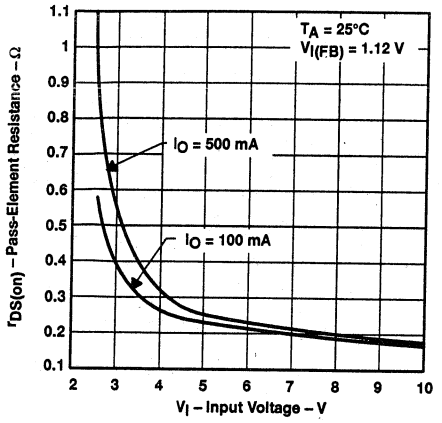


Figure 30

DIVIDER RESISTANCE
vs
FREE-AIR TEMPERATURE

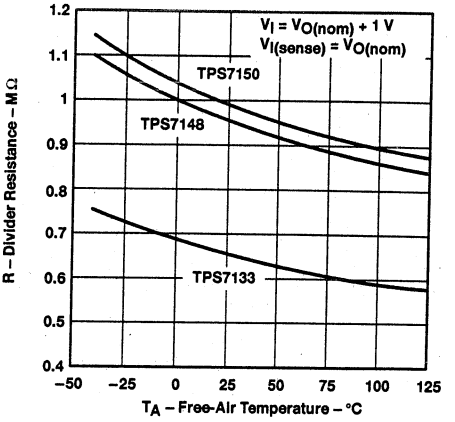


Figure 31

FIXED-OUTPUT VERSIONS
SENSE PIN CURRENT
vs
FREE-AIR TEMPERATURE

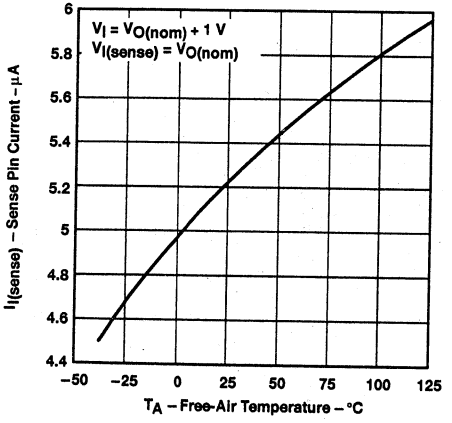


Figure 32

ADJUSTABLE VERSION
FB LEAKAGE CURRENT
vs
FREE-AIR TEMPERATURE

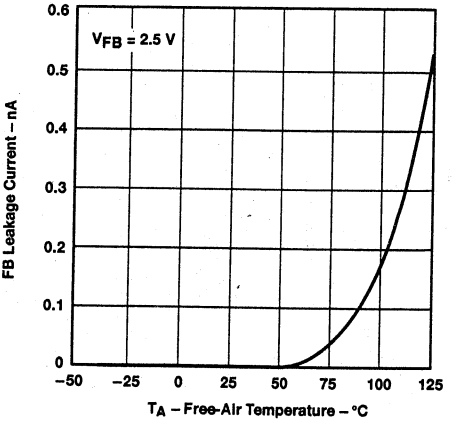


Figure 33

TYPICAL CHARACTERISTICS

MINIMUM INPUT VOLTAGE FOR ACTIVE PASS ELEMENT vs FREE-AIR TEMPERATURE

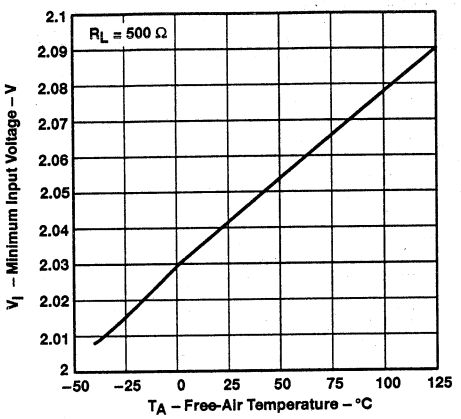


Figure 34

MINIMUM INPUT VOLTAGE FOR VALID POWER GOOD (PG) vs FREE-AIR TEMPERATURE

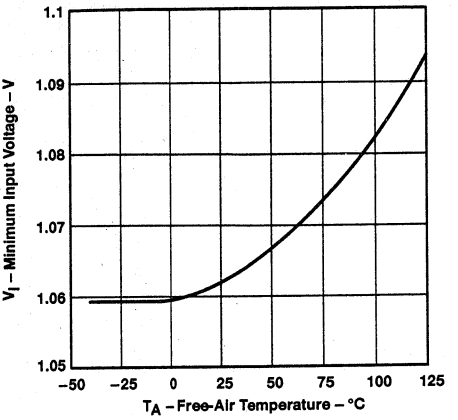


Figure 35

$\overline{EN}$ INPUT CURRENT vs FREE-AIR TEMPERATURE

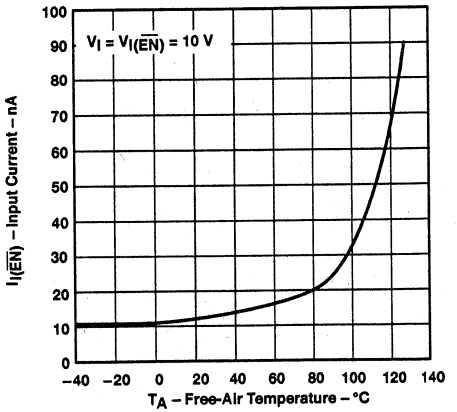


Figure 36

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE FROM
ENABLE ($\overline{EN}$)

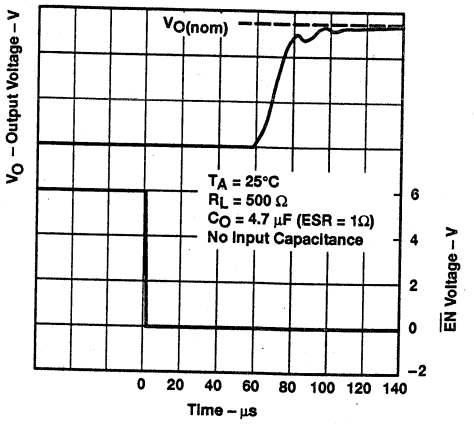


Figure 37

POWER-GOOD (PG) VOLTAGE
vs
OUTPUT VOLTAGE

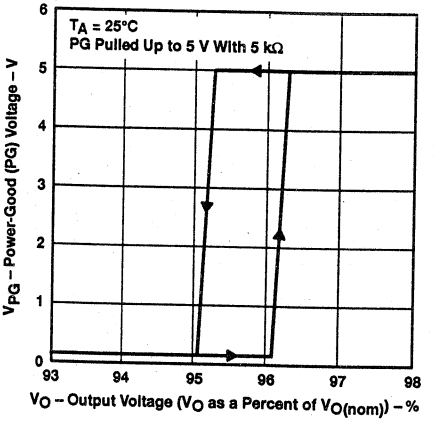


Figure 38

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
OUTPUT CURRENT

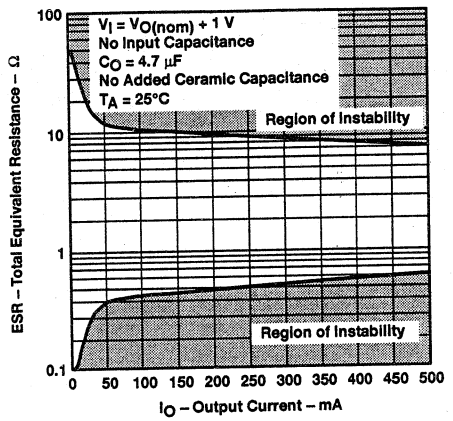


Figure 39

TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
OUTPUT CURRENT

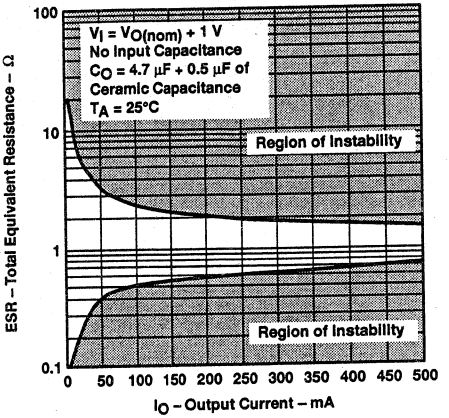


Figure 40

TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

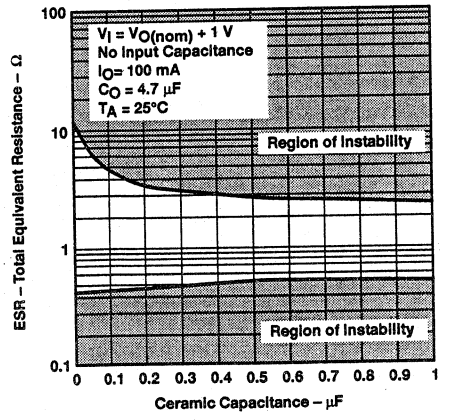


Figure 41

TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

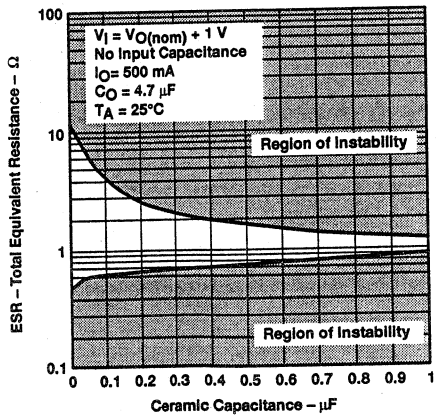


Figure 42

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
OUTPUT CURRENT

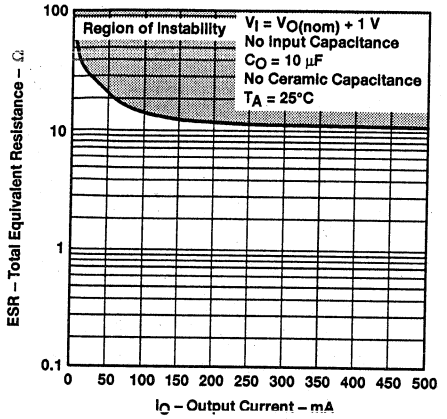


Figure 43

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
OUTPUT CURRENT

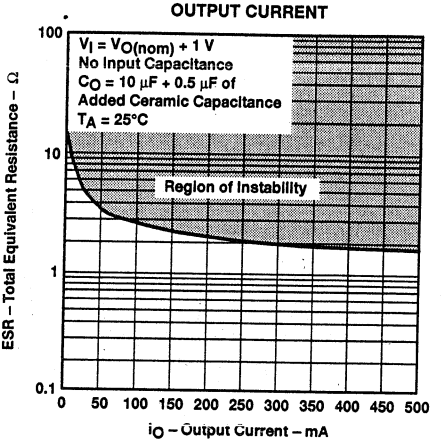


Figure 44

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

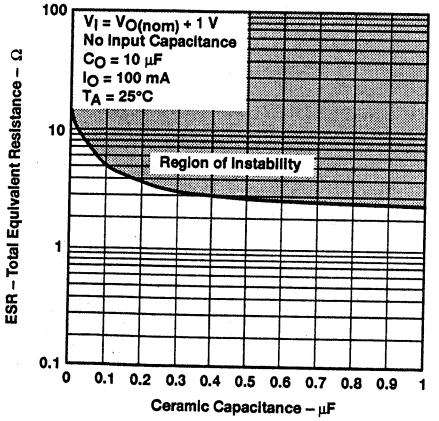


Figure 45

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

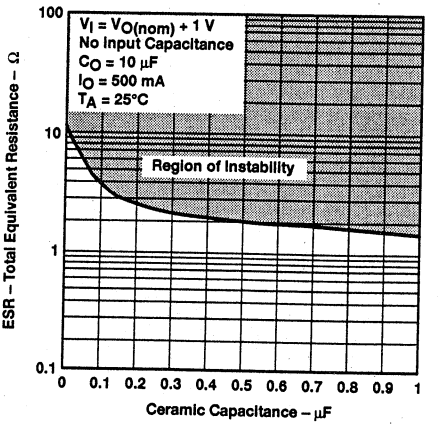
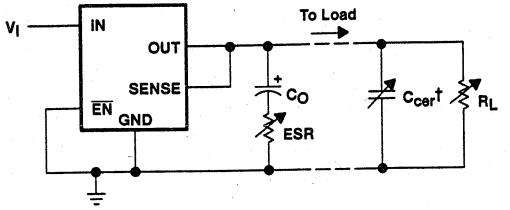


Figure 46

†ESR values below 0.1 Ω are not recommended.

TYPICAL CHARACTERISTICS



† Ceramic capacitor

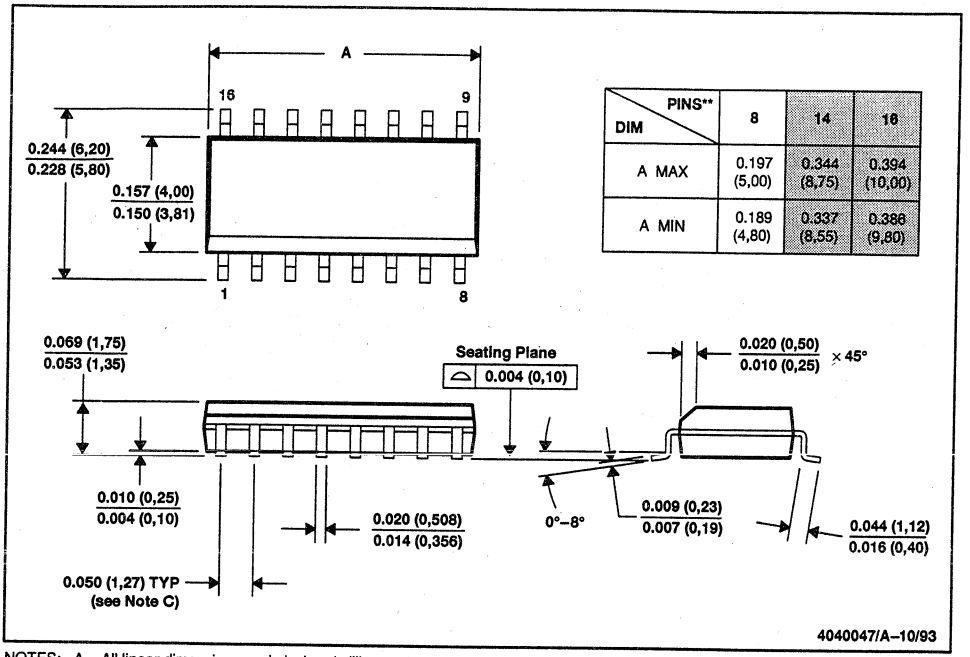
Figure 47. Test Circuit for Typical Regions of Stability (Figures 39 through 46)

MECHANICAL DATA

D/R-PDSO-G**

16 PIN SHOWN

PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE

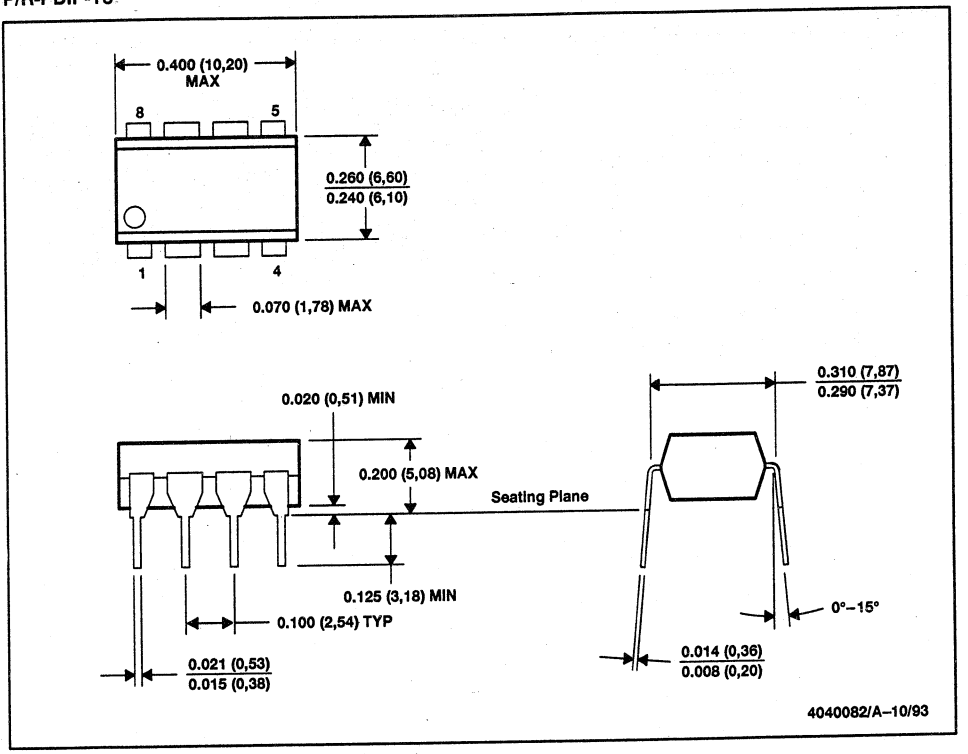


DIM \ PINS**	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).

MECHANICAL DATA

P/R-PDIP-T8 **PLASTIC DUAL-IN-LINE PACKAGE**



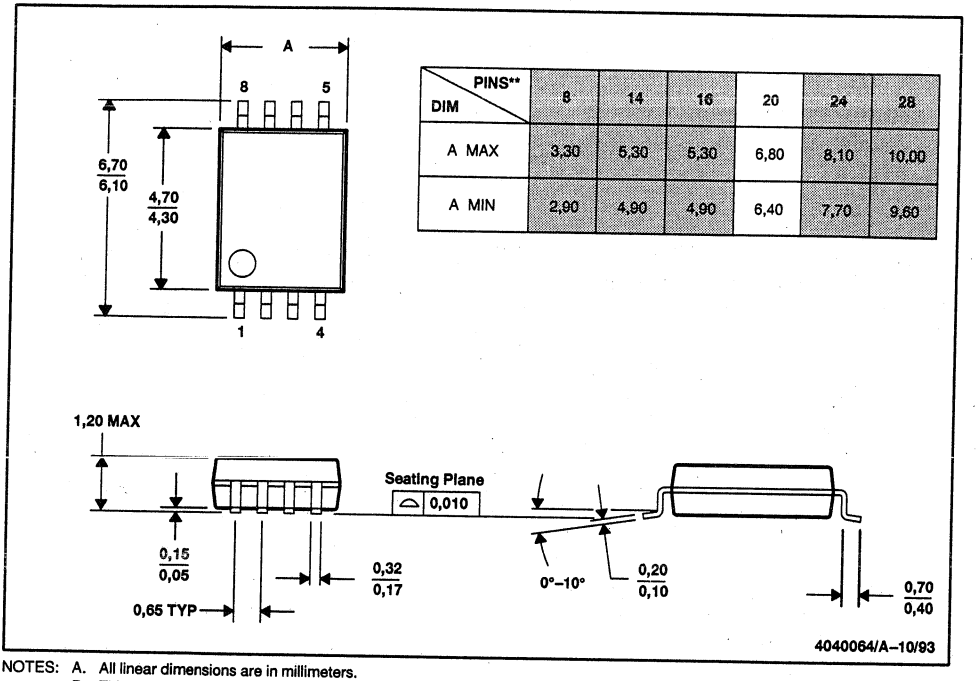
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

MECHANICAL DATA

PW/R-PDSO-G**

PLASTIC SMALL-OUTLINE PACKAGE

8 PIN SHOWN



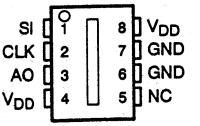
DIM \ PINS**	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Leads are within 0,127 radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

SOES009A – D4059, NOVEMBER 1992 – REVISED AUGUST 1993

- **Contains 64-Bit Static Shift Register**
- **Contains Analog Buffer With Sample and Hold for Analog Output Over Full Clock Period**
- **Single-Supply Operation**
- **Operates With 500-kHz Shift Clock**
- **8-Pin Clear Plastic DIP Package**
- **Advanced LinCMOS™ Technology**

(TOP VIEW)



NC – No internal connection

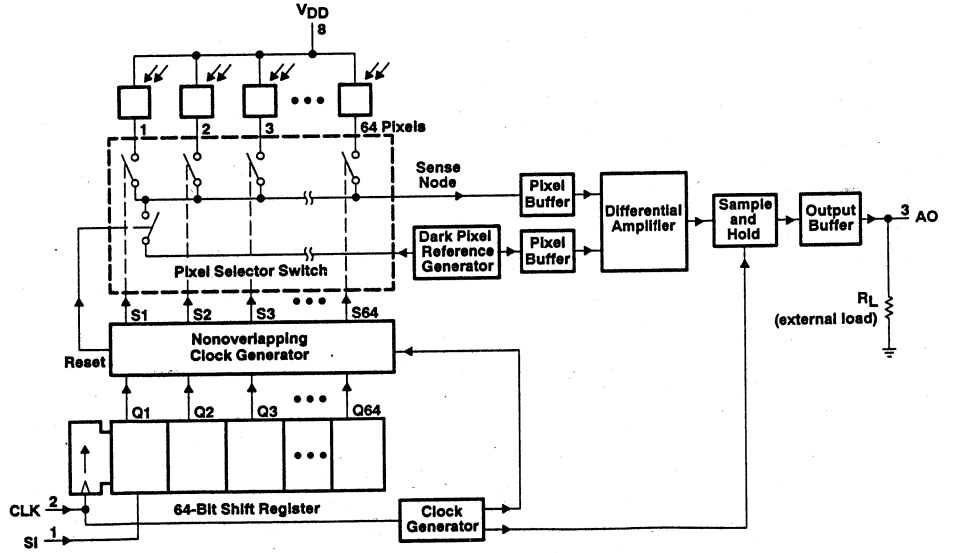
description

The TSL213 integrated opto sensor consists of 64 charge-mode pixels arranged in a 64 × 1 linear array. Each pixel measures 120 µm × 70 µm with 125-µm center-to-center spacing. Operation is simplified by internal logic requiring only clock and start-integration-pulse signals.

The TSL213 is intended for use in a wide variety of applications including linear and rotary encoding, linear positioning, edge and mark detection, and contact imaging.

The TSL213 is supplied in an 8-pin dual-in-line clear plastic package.

functional block diagram



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
AO	3	Analog output
CLK	2	Clock. The clock controls charge transfer, pixel output, and reset.
GND	6, 7	Ground (substrate). All voltages are referenced to the substrate.
NC	5	No internal connection
SI	1	Serial input. The serial input defines the end of the integration period and initiates the pixel output sequence.
V_{DD}	4, 8	Supply voltages. These supply power to the analog and digital circuits.

detailed description

sensor elements

The line of sensor elements, called pixels, consists of 64 discrete photosensing areas. Light energy striking a pixel generates electron-hole pairs in the region under the pixel. The field generated by the bias on the pixel causes the electrons to collect in the element while the holes are swept into the substrate. The amount of charge accumulated in each element is directly proportional to the amount of incident light and the integration time.

device operation

Operation of the 64 × 1 array sensor consists of two time periods: an integration period during which charge is accumulated in the pixels and an output period during which signals are transferred to the output. The integration period is defined by the interval between serial-input (SI) pulses and includes the output period (see Figure 1). The required length of the integration period depends upon the amount of incident light and the desired output signal level.

sense node

On completion of the integration period, the charge contained in each pixel is transferred in turn to the sense node under the control of the clock (CLK) and SI signals. The signal voltage generated at this node is directly proportional to the amount of charge and inversely proportional to the capacitance of the sense node.

reset

An internal reset signal is generated by the nonoverlapping clock generator (NOCG) and occurs every clock cycle. Reset establishes a known voltage on the sense node in preparation for the next charge transfer. This voltage is used as a reference level for the differential signal amplifier.

shift register

The 64-bit shift register controls the transfer of charge from the pixels to the output stages and provides timing signals for the NOCG. The SI signal provides the input to the shift register and is shifted under direct control of the clock.

The output period is initiated by the presence of the SI input pulse coincident with a rising edge of CLK (see Figures 1 and 2). The analog output voltage corresponds to the level of the first pixel after settling time (t_s) and remains constant for a minimum time, t_v. A voltage corresponding to each succeeding pixel is available at each rising edge of the clock. The output period ends on the rising edge of the 65th clock cycle, at which time the output assumes the high-impedance state. The 65th clock cycle terminates the output of the last pixel and clears the shift register in preparation for the next SI pulse. To achieve minimum integration time, the SI pulse may be present on the 66th rising edge of the clock to immediately reinitiate the output phase. When the output period has been initiated by an SI pulse, the clock must be allowed to complete 65 positive-going transitions in order to reset the internal logic to a known state.

sample and hold

The sample-and-hold signal generated by the NOCG is used to hold the analog output voltage of each pixel constant until the next pixel is clocked out. The signal is sampled while CLK is high and held constant while CLK is low.

nonoverlapping clock generators

The NOCG circuitry provides internal control signals for the sensor, including reset and pixel-charge sensing. The signals are synchronous and are controlled by the outputs of the shift register.

initialization

Initialization of the sensor elements may be necessary on power up or during operation after any period of clock or SI inactivity exceeding the integration time. The initialization phase consists of 12 to 15 consecutively performed output cycles and clears the pixels of any charge that may have accumulated during the inactive period.

output enable

The internally-generated output-enable signal enables the output stage of the sensor during the output period (64 clock cycles). During the remainder of the integration period, the output stage is in the high-impedance state that allows output interconnections of multiple devices without interference.

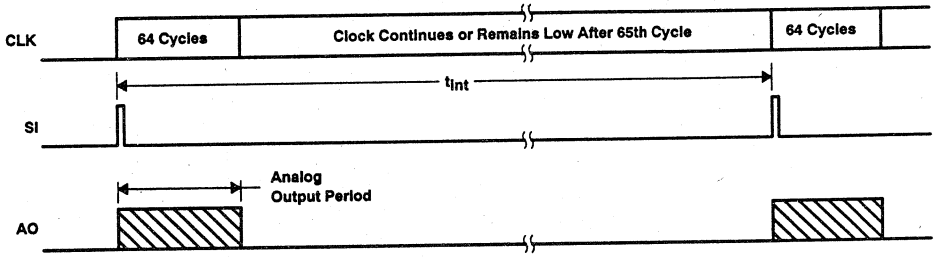


Figure 1. Timing Waveforms

absolute maximum ratings, T_A = 25°C (unless otherwise noted) (see Note 1)†

Supply voltage range, V_{DD}	−0.5 V to 7 V
Digital input current range, I_I	−20 mA to 20 mA
Operating case temperature range, T_C (see Note 2)	−10°C to 85°C
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to the network GND.
2. Case temperature is the surface temperature of the plastic package measured directly over the integrated circuit.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5		5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	V_{DD} × 0.7		V_{DD}	V
Low-level input voltage, V_{IL}	0		V_{DD} × 0.3	V
Wavelength of light source, λ		750		nm
Clock input frequency, f_{clock}	10		500	kHz
Pulse duration, CLK low, t_w	1			μs
Sensor integration time, t_{int}		5		ms
Setup time, SI before CLK↑, $t_{su(SI)}$	50			ns
Hold time, SI after CLK↑, $t_{h(SI)}$	50			ns
External resistive load, AO, R_L		330		Ω
Total number of TSL213 outputs connected together			10	
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, V_{DD} = 5 V, T_A = 25°C, f_{clock} = 180 kHz, λ_p = 565 nm, R_L = 330 Ω, C_L = 330 pF, t_{int} = 5 ms, E_e = 20 μW/cm² (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog output voltage saturation level	E_e = 51 μW/cm²	3	3.4		V
Analog output voltage (white, average over 64 pixels)		1.75	2		V
Analog output voltage (dark, each pixel)	E_e = 0		0.25	0.4	V
Output voltage (white) change with change in V_{DD}	V_{DD} = 5 V ±5%		±2%		
Dispersion of analog output voltage	See Note 4			±10%	
Linearity of analog output voltage	See Note 5	0.85		1.15	
Pixel recovery time	See Note 6		25	40	ms
Supply current	I_{DD} Avg		4	9	mA
High-level input current	V_I = V_{DD}			0.5	μA
Low-level input current	V_I = 0			0.5	μA
Input capacitance			5		pF

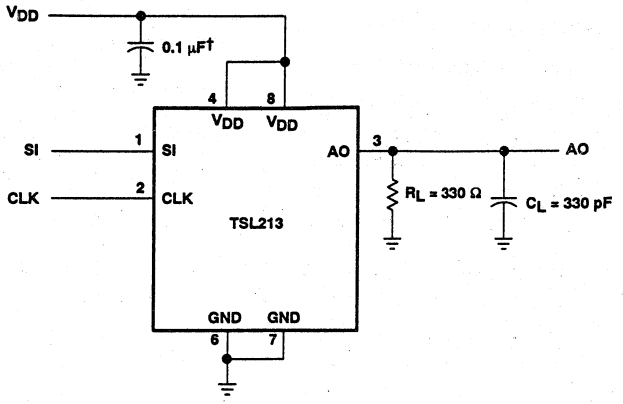
NOTES: 3. The input irradiance (E_e) is supplied by an LED array with λ_p = 565 nm.
4. Dispersion of analog output voltage is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test.
5. Linearity of analog output voltage is calculated by averaging over 64 pixels and measuring the maximum deviation of the voltage at 2 ms and 3.5 ms from a line drawn between the voltage at 2.5 ms and the voltage at 5 ms.
6. Pixel recovery time is the time required for a pixel to go from the analog-output-voltage (white, average over 64 pixels) level to the analog-output-voltage (dark, each pixel) level or vice versa after a step change in light input.

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 330 Ω, C_L = 330 pF, t_{int} = 5 ms, E_e = 20 μW/cm², f_{clock} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_s	Settling time	See Figure 2 and Note 7			1	μs
t_v	Valid time				1/2 f_{clock}	μs

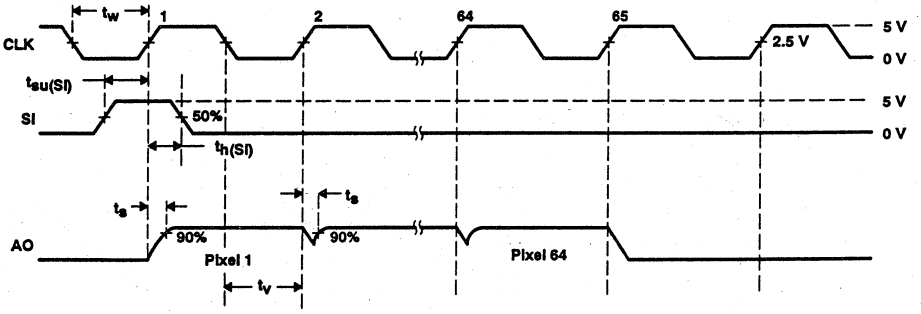
NOTE 7: Clock duty cycle is assumed to be 50%.

PARAMETER MEASUREMENT INFORMATION



† Supply bypass capacitor with short leads should be placed as close to the device as possible.

TEST CIRCUIT



OPERATIONAL WAVEFORMS

Figure 2. Test Circuit and Operational Waveforms

TYPICAL CHARACTERISTICS

NORMALIZED RESPONSIVITY
vs
WAVELENGTH OF INCIDENT LIGHT

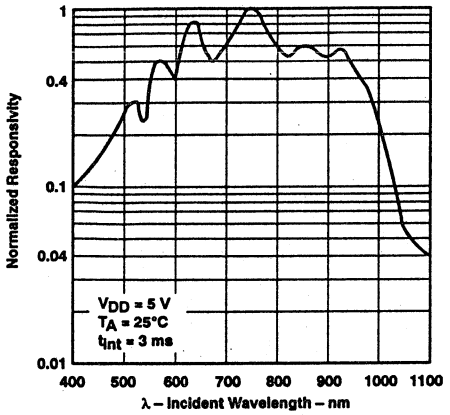


Figure 3

INTEGRATION TIME
vs
IRRADIANCE FOR CONSTANT AVERAGE ANALOG OUTPUT VOLTAGE

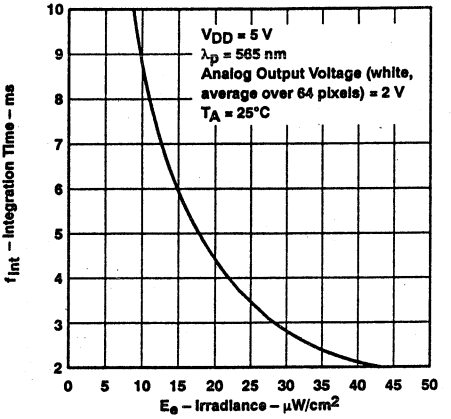


Figure 4

ANALOG OUTPUT VOLTAGE (DARK)
vs
INTEGRATION TIME

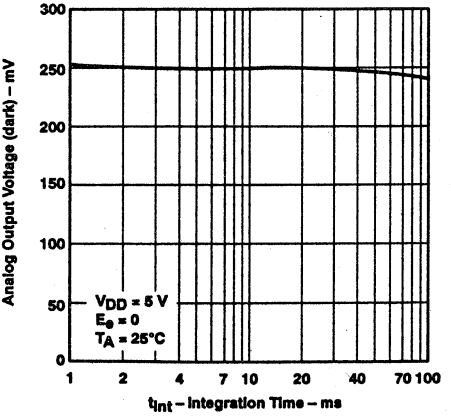


Figure 5

NORMALIZED OUTPUT VOLTAGE
vs
INTEGRATION TIME

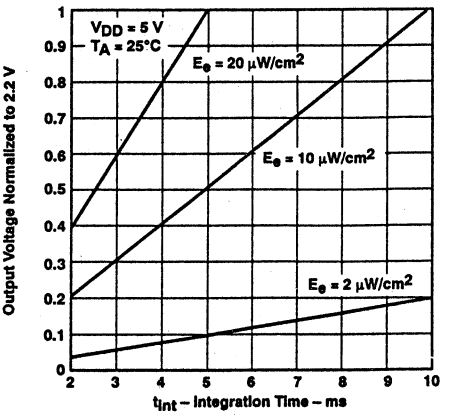
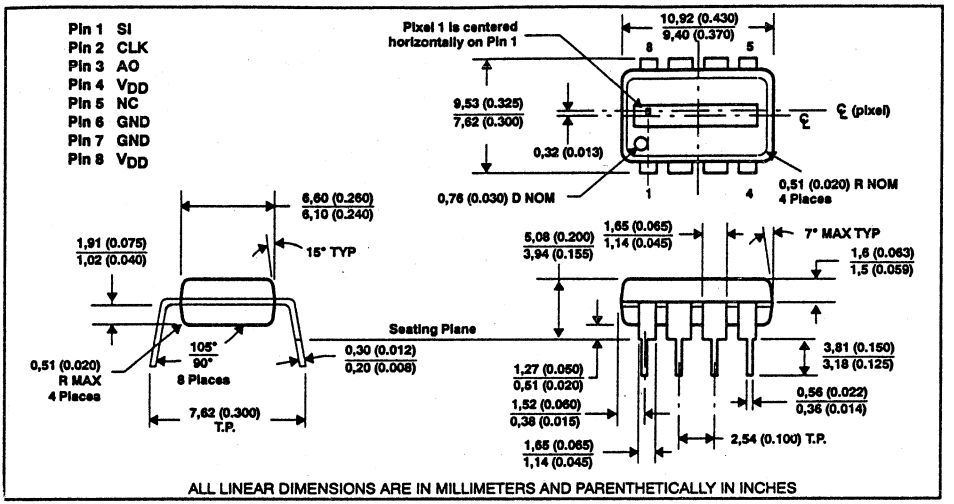


Figure 6

mechanical data

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated with an electrically nonconductive clear plastic compound.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

SOES007B – OCTOBER 1992 – REVISED MARCH 1994

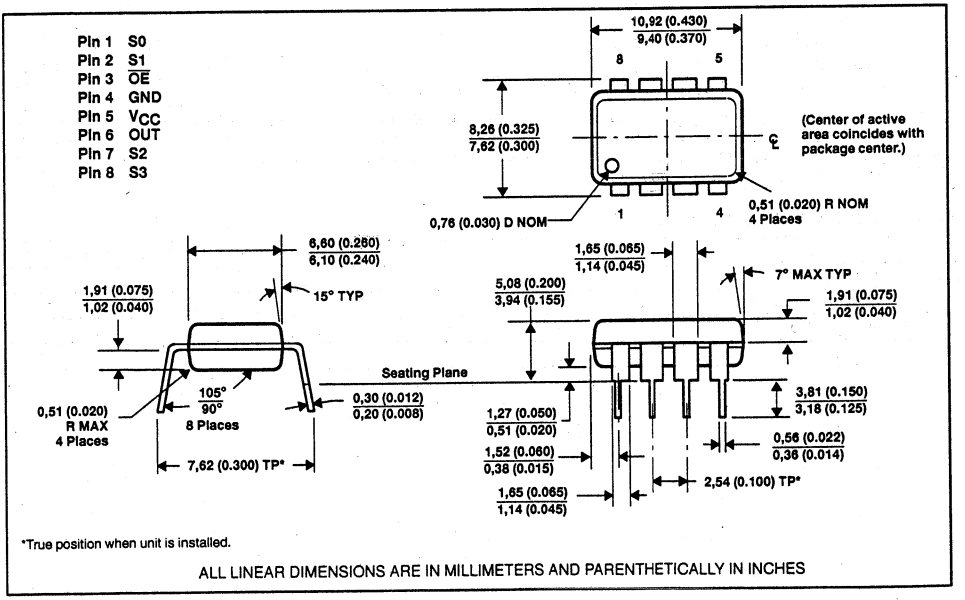
- **High-Resolution Conversion of Light Intensity to Frequency With No External Components**
- **Programmable Sensitivity and Full-Scale Output Frequency**
- **Communicates Directly With a Microcontroller**
- **Single-Supply Operation Down to 2.7 V, With Power-Down Feature**
- **Absolute Output Frequency Tolerance of ±5% (TSL230B)**
- **Nonlinearity Error Typically 0.2% at 100 kHz**
- **Stable 100 ppm/°C Temperature Coefficient**
- **Advanced LinCMOS™ Technology**

description

The TSL230, TSL230A, and TSL230B programmable light-to-frequency converters combine a configurable silicon photodiode and a current-to-frequency converter on single monolithic CMOS integrated circuits. The output can be either a pulse train or a square wave (50% duty cycle) with frequency directly proportional to light intensity. The sensitivity of the devices is selectable in three ranges, providing two decades of adjustment. The full-scale output frequency can be scaled by one of four preset values. All inputs and the output are TTL compatible, allowing direct two-way communication with a microcontroller for programming and output interface. An output enable ($\overline{OE}$) is provided that places the output in the high-impedance state for multiple-unit sharing of a microcontroller input line. The devices are available with absolute-output-frequency tolerances of ±5% (TSL230B), ±10% (TSL230A), or ±20% (TSL230). Each circuit has been temperature compensated for the ultraviolet-to-visible-light range of 300 nm to 700 nm. The devices are characterized for operation over the temperature range of −25°C to 70°C.

mechanical data

The TSL230, TSL230A, and TSL230B are packaged in a clear plastic 8-pin dual-in-line package. The photodiode area is typically 1.36 mm^2 (0.0029 in^2) (S0 = S1 = H).



*True position when unit is installed.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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Terminal Functions

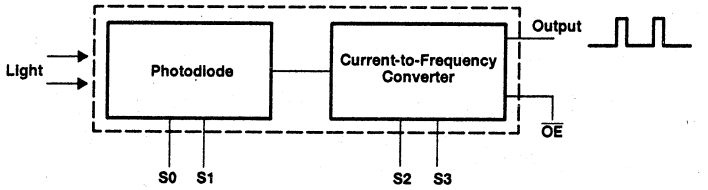
TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4		Ground
$\overline{OE}$	3	I	Enable for f_O (active low)
OUT	6	O	Scaled-frequency (f_O) output
S0, S1	1, 2	I	Sensitivity-select inputs
S2, S3	7, 8	I	f_O scaling-select inputs
V_{DD}	5		Supply voltage

Selectable Options

S1	S0	SENSITIVITY
L	L	Power Down
L	H	1×
H	L	10×
H	H	100×

S3	S2	f_O SCALING (divide-by)
L	L	1
L	H	2
H	L	10
H	H	100

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 6.5 V
Input voltage range, all inputs, V_I ..... −0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A ..... −25°C to 70°C
Storage temperature range ..... −25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.7	5	6	V
High-level input voltage, V_{IH}	V_{DD} = 4.5 V to 5.5 V	2		V_{DD}	V
Low-level input voltage, V_{IL}	V_{DD} = 4.5 V to 5.5 V	0		0.8	V
Operating free-air temperature range, T_A		−25		70	°C

electrical characteristics at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −4 mA	4	4.3		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		0.17	0.26	V
I_{IH}	High-level input current				1	µA
I_{IL}	Low-level input current				1	µA
I_{DD}	Supply current	Power-on mode		2	3	mA
		Power-down mode			10	µA
	Full-scale frequency†		1.1			MHz
	Temperature coefficient of output frequency	λ ≤ 700 nm, −25°C ≤ T_A ≤ 70°C		±100		ppm/°C
k_{SVS}	Supply voltage sensitivity	V_{DD} = 5 V ±10%		0.5		%/V

operating characteristics at V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TSL230			TSL230A			TSL230B			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_O	Output frequency	S0 = H, S1 = S2 = S3 = L, E_e = 130 mW/cm², λ_p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz
		E_e = 0, S0 = H, S1 = S2 = S3 = L		0.1	10		0.1	10		0.1	10	Hz
		S1 = H, S0 = S2 = S3 = L, E_e = 13 mW/cm², λ_p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz
		E_e = 0 S1 = H, S0 = S2 = S3 = L		0.13	10		0.13	10		0.13	10	Hz
		S0 = S1 = H, S2 = S3 = L, E_e = 1.3 mW/cm², λ_p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz
		E_e = 0, S0 = S1 = H, S2 = S3 = L		0.5	10		0.5	10		0.5	10	Hz
t_w	Output pulse duration	S2 = S3 = L	125		550	125		550	125		550	ns
		S2 or S3 = H		1/2f_O			1/2f_O			1/2f_O		s
	Nonlinearity‡	f_O = 0 MHz to 10 kHz		±0.1%			±0.1%			±0.1%		%F.S.
		f_O = 0 MHz to 100 kHz		±0.2%			±0.2%			±0.2%		%F.S.
		f_O = 0 MHz to 1 MHz		±0.5%			±0.5%			±0.5%		%F.S.
	Recovery from power down				100			100			100	µs
	Step response to full-scale step input		1 pulse of new frequency plus 1 µs									
	Response time to programming change		2 periods of new principal frequency plus 1 µs§									
	Response time to output enable ($\overline{OE}$)			50	150		50	150		50	150	ns

† Full-scale frequency is the maximum operating frequency of the device without saturation.
‡ Nonlinearity is defined as the deviation of f_O from a straight line between zero and full scale, expressed as a percent of full scale.
§ Principal frequency is the internal oscillator frequency, equivalent to divide-by-1 output selection.

TYPICAL CHARACTERISTICS

OUTPUT FREQUENCY
vs
IRRADIANCE

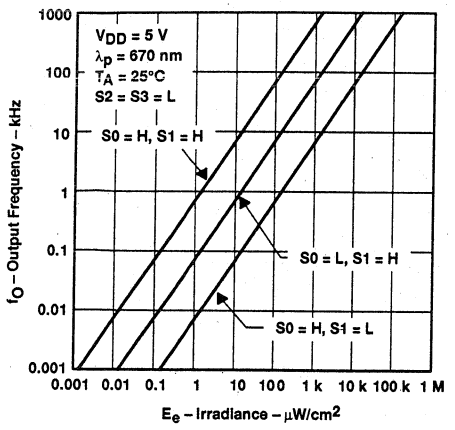


Figure 1

PHOTODIODE SPECTRAL RESPONSIVITY

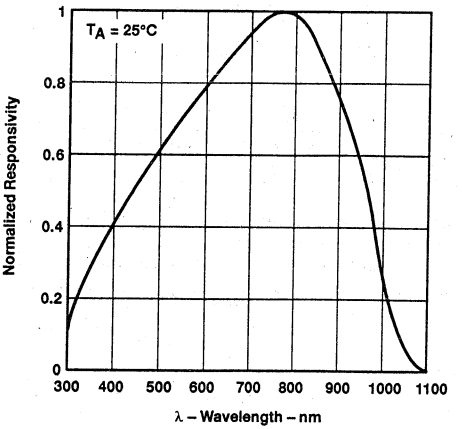


Figure 2

DARK FREQUENCY
vs
TEMPERATURE

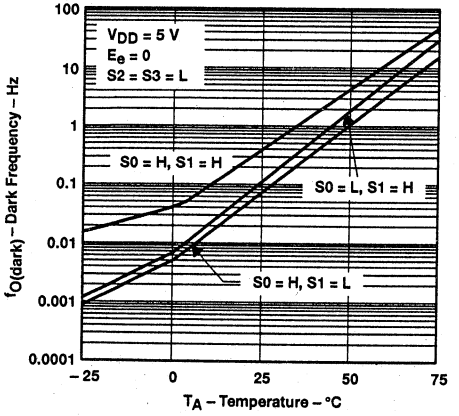


Figure 3

TEMPERATURE COEFFICIENT
OF OUTPUT FREQUENCY
vs
WAVELENGTH OF INCIDENT LIGHT

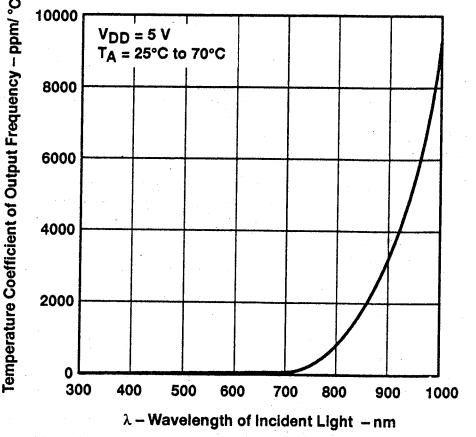


Figure 4

TYPICAL CHARACTERISTICS

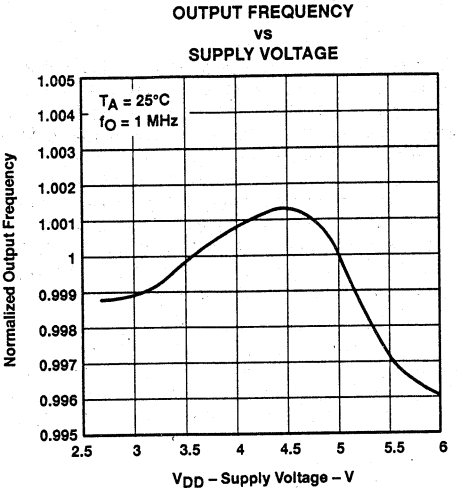


Figure 5

APPLICATION INFORMATION

power supply considerations

For optimum device performance, power-supply lines should be decoupled by a 0.01-µF to 0.1-µF capacitor with short leads.

output interface

The output of the device is designed to drive a standard TTL or CMOS logic input over short distances. If lines greater than 12 inches are used on the output, a buffer or line driver is recommended.

sensitivity adjustment

Sensitivity is controlled by two logic inputs, S0 and S1. Sensitivity is adjusted using an electronic iris technique – effectively an aperture control – to change the response of the device to a given amount of light. The sensitivity can be set to one of three levels: 1x, 10x or 100x, providing two decades of adjustment. This allows the responsivity of the device to be optimized to a given light level while preserving the full-scale output-frequency range. Changing of sensitivity also changes the effective photodiode area by the same factor.

APPLICATION INFORMATION

output-frequency scaling

Output-frequency scaling is controlled by two logic inputs, S2 and S3. Scaling is accomplished on chip by internally connecting the pulse-train output of the converter to a series of frequency dividers. Divided outputs available are divide-by 2, 10, 100, and 1 (no division). Divided outputs are 50 percent-duty-cycle square waves while the direct output (divide-by 1) is a fixed-pulse-width pulse train. Because division of the output frequency is accomplished by counting pulses of the principal (divide-by 1) frequency, the final-output period represents an average of n (where n is 2, 10 or 100) periods of the principal frequency. The output-scaling-counter registers are cleared upon the next pulse of the principal frequency after any transition of the S0, S1, S2, S3, or OE lines. The output goes high upon the next subsequent pulse of the principal frequency, beginning a new valid period. This minimizes the time delay between a change on the input lines and the resulting new output period in the divided output modes. In contrast with the sensitivity adjust, use of the divided outputs lowers both the full-scale frequency and the dark frequency by the selected scale factor.

The frequency-scaling function allows the output range to be optimized for a variety of measurement techniques. The divide-by-1 or straight-through output can be used with a frequency counter, pulse accumulator, or high-speed timer (period measurement). The divided-down outputs may be used where only a slower frequency counter is available, such as a low-cost microcontroller, or where period measurement techniques are used. The divide-by-10 and divide-by-100 outputs provide lower frequency ranges for high resolution-period measurement.

measuring the frequency

The choice of interface and measurement technique depends on the desired resolution and data acquisition rate. For maximum data-acquisition rate, period-measurement techniques are used.

Using the divide-by-2 output, data can be collected at a rate of twice the output frequency or one data point every microsecond for full-scale output. Period measurement requires the use of a fast reference clock with available resolution directly related to reference-clock rate. Output scaling can be used to increase the resolution for a given clock rate or to maximize resolution as the light input changes. Period measurement is used to measure rapidly varying light levels or to make a very fast measurement of a constant light source.

Maximum resolution and accuracy may be obtained using frequency-measurement, pulse-accumulation, or integration techniques. Frequency measurements provide the added benefit of averaging out random- or high-frequency variations (jitter) resulting from noise in the light signal. Resolution is limited mainly by available counter registers and allowable measurement time. Frequency measurement is well suited for slowly varying or constant light levels and for reading average light levels over short periods of time. Integration (the accumulation of pulses over a very long period of time) can be used to measure exposure, the amount of light present in an area over a given time period.

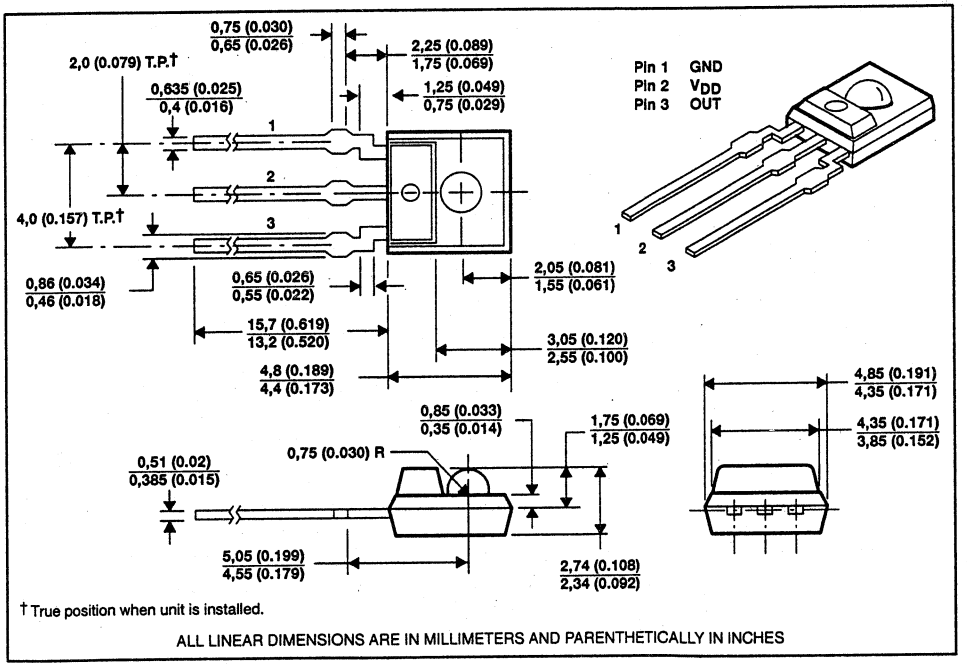
- High-Resolution Conversion of Light Intensity to Frequency With No External Components
- Communicates Directly With a Microcontroller
- Compact Three-Leaded Clear-Plastic Package
- Single-Supply Operation Down to 2.7 V
- Nonlinearity Error Typically 0.2% at 100 kHz
- Stable 100 ppm/°C Temperature Coefficient
- Advanced LinCMOS™ Technology

description

The TSL235 light-to-frequency converter combines a silicon photodiode and a current-to-frequency converter on a single monolithic CMOS integrated circuit. The output is a square wave (50% duty cycle) with frequency directly proportional to light intensity. Because it is TTL compatible, the output allows direct interface to a microcontroller or other logic circuitry. The device has been temperature compensated for the ultraviolet-to-visible light range of 300 nm to 700 nm and responds over the light range of 300 nm to 1100 nm. The TSL235 is characterized for operation over the temperature range of −25°C to 70°C.

mechanical data

The TSL235 is offered in a clear-plastic three-leaded package. The photodiode area is 1.36 mm^2 (0.0029 in^2).



† True position when unit is installed.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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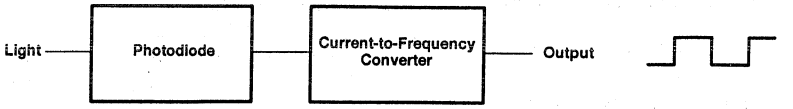
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 6.5 V
Operating free-air temperature range, T_A ..... −25°C to 70°C
Storage temperature range ..... −25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.7	5	6	V
Operating free-air temperature range, T_A	−25		70	°C

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −4 mA	4	4.3		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		0.17	0.26	V
I_{DD}	Supply current			2	3	mA
	Full-scale frequency‡		500			kHz
	Temperature coefficient of output frequency	$\lambda \leq 700$ nm, −25°C ≤ $T_A \leq$ 70°C		±100		ppm/°C
k_{SVS}	Supply-voltage sensitivity	V_{DD} = 5 V ±10%		0.5		%/V

operating characteristics at V_{DD} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_O	Output frequency	E_e = 375 μW/cm², λ_p = 670 nm	200	250	300	kHz
		E_e = 0		0.25	10	Hz
	Nonlinearity§	f_O = 0 kHz to 10 kHz		±0.1%		%F.S.
		f_O = 0 kHz to 100 kHz		±0.2%		%F.S.
	Step response to full-scale step input			1 pulse of new frequency plus 1 μs		

‡ Full-scale frequency is the maximum operating frequency of the device without saturation.

§ Nonlinearity is defined as the deviation of f_O from a straight line between zero and full scale, expressed as a percent of full scale.

TYPICAL CHARACTERISTICS

OUTPUT FREQUENCY
vs
IRRADIANCE

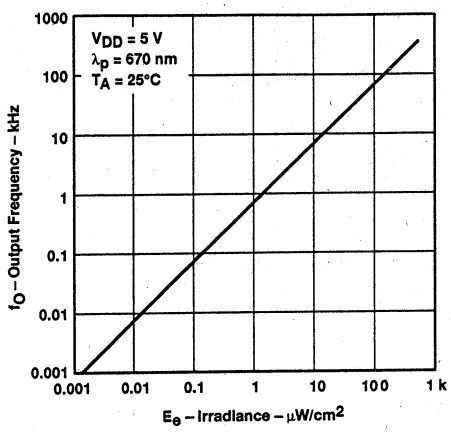


Figure 1

PHOTODIODE SPECTRAL RESPONSIVITY

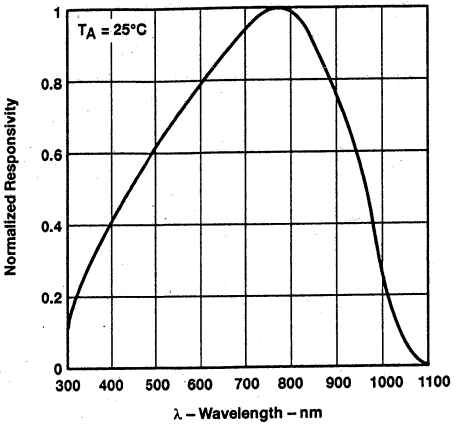


Figure 2

DARK FREQUENCY
vs
TEMPERATURE

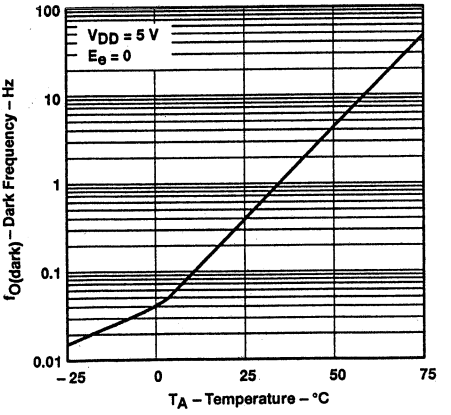


Figure 3

TEMPERATURE COEFFICIENT
OF OUTPUT FREQUENCY
vs
WAVELENGTH OF INCIDENT LIGHT

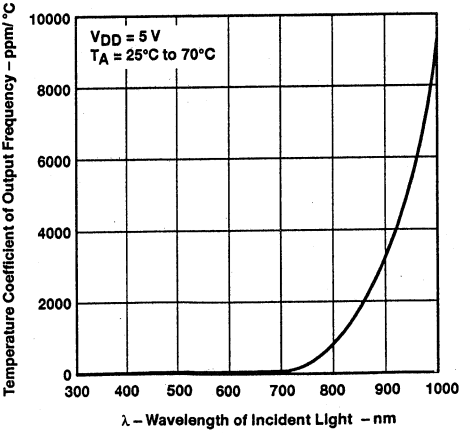


Figure 4

TYPICAL CHARACTERISTICS

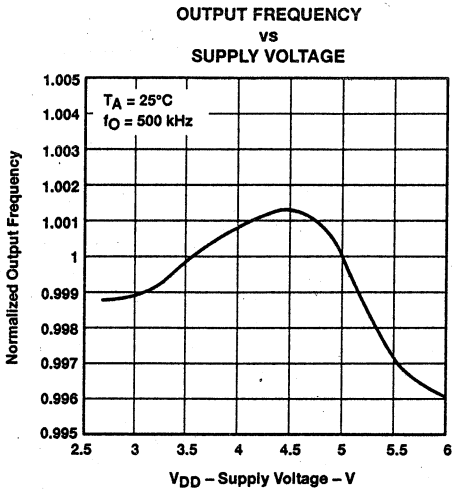


Figure 5

APPLICATION INFORMATION

power-supply considerations

For optimum device performance, power-supply lines should be decoupled by a 0.01-μF to 0.1-μF capacitor with short leads (see Figure 6).

output interface

The output of the device is designed to drive a standard TTL or CMOS logic input over short distances. If lines greater than 12 inches are used on the output, a buffer or line driver is recommended.

measuring the frequency

The choice of interface and measurement technique depends on the desired resolution and data-acquisition rate. For maximum data-acquisition rate, period-measurement techniques are used.

Period measurement requires the use of a fast reference clock with available resolution directly related to reference-clock rate. The technique is employed to measure rapidly varying light levels or to make a fast measurement of a constant light source.

Maximum resolution and accuracy may be obtained using frequency-measurement, pulse-accumulation, or integration techniques. Frequency measurements provide the added benefit of averaging out random- or high-frequency variations (jitter) resulting from noise in the light signal. Resolution is limited mainly by available counter registers and allowable measurement time. Frequency measurement is well suited for slowly varying or constant light levels and for reading average light levels over short periods of time. Integration, the accumulation of pulses over a very long period of time, can be used to measure exposure – the amount of light present in an area over a given time period.

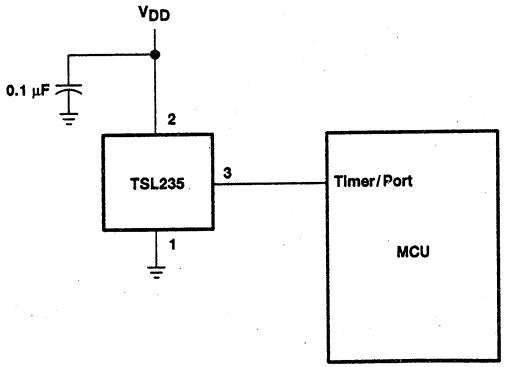


Figure 6. Typical TSL235 Interface to a Microcontroller

SOES004B–D3732, AUGUST 1991 – REVISED AUGUST 1992

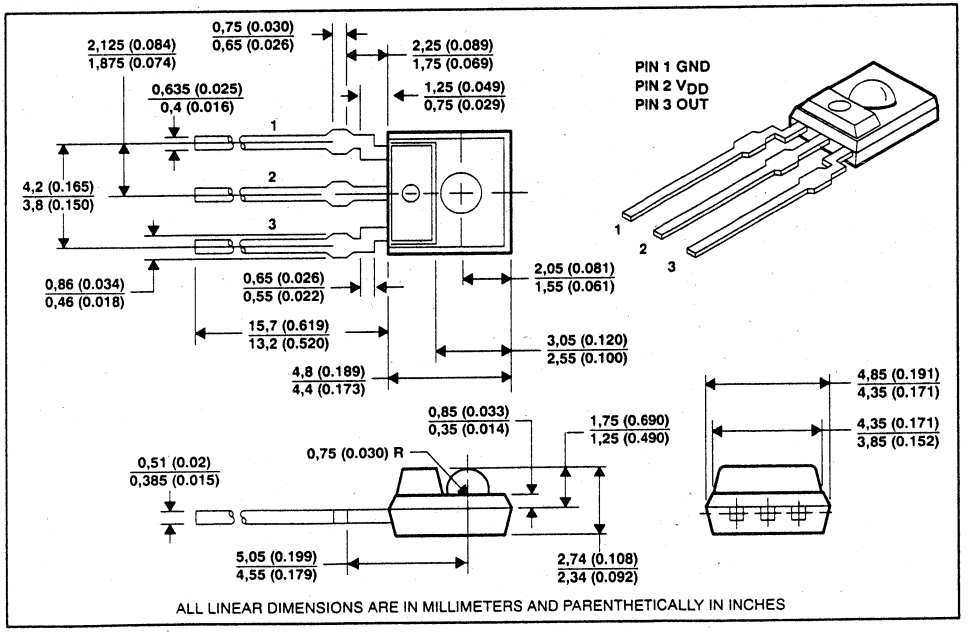
- **Monolithic Silicon IC Containing Photodiode, Operational Amplifier, and Feedback Components**
- **Converts Light Intensity to Output Voltage**
- **High Irradiance Responsivity Typically 80 mV/(μW/cm²) at λ_p = 880 nm (TSL250)**
- **Compact Three-Leaded Clear Plastic Package**
- **Low Dark (Offset) Voltage . . . 10 mV Max at 25°C, V_{DD} = 5 V**
- **Single-Supply Operation**
- **Wide Supply Voltage Range . . . 3 V to 9 V**
- **Low Supply Current . . . 800 μA Typical at V_{DD} = 5 V**
- **Advanced LinCMOS™ Technology**

description

The TSL250, TSL251, and TSL252 are light-to-voltage optical sensors each combining a photodiode and a transimpedance amplifier (feedback resistor = 16 MΩ, 8 MΩ, and 2 MΩ, respectively) on a single monolithic IC. The output voltage is directly proportional to the light intensity (irradiance) on the photodiode. The TSL250, TSL251, and TSL252 utilize Texas Instruments silicon-gate LinCMOS™ technology, which provides good amplifier offset-voltage stability and low power consumption.

mechanical data

The photodiode/amplifier chip is packaged in a clear plastic three-leaded package. The integrated photodiode active area is typically 1,0 mm² (0.0016 in²), 0.5 mm² (0.00078 in²), and 0.26 mm² (0.0004 in²) for the TSL250, TSL251, and TSL252, respectively.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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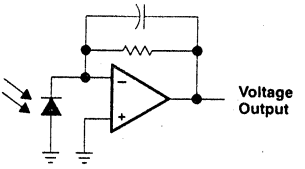
TEXAS INSTRUMENTS

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) ..... 10 V
Output current, I_O ..... ±10 mA
Duration of short-circuit current at (or below) 25°C (see Note 2) ..... 5 s
Operating free-air temperature range ..... −25°C to 85°C
Storage temperature range ..... −25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 240°C

NOTES: 1. All voltages are with respect to GND (pin 1).
2. Output may be shorted to either supply.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	9	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at V_{DD} = 5 V, T_A = 25°C, λp = 880 nm, R_L = 10 kΩ, (unless otherwise noted) (see Note 3)

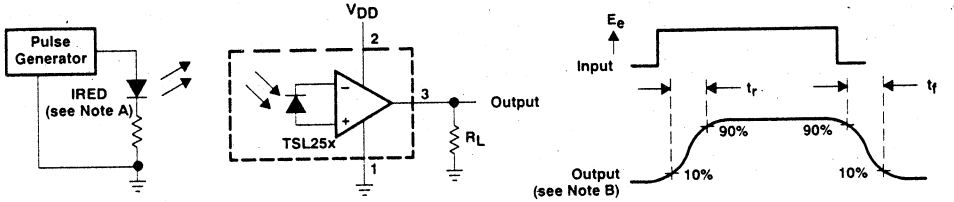
PARAMETER		TEST CONDITIONS	TSL250			TSL251			TSL252			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_D	Dark voltage	E_e = 0		3	10		3	10		3	10	mV
V_{OM}	Maximum output	E_e = 2 mW/cm²	3.1	3.5		3.1	3.5		3.1	3.5		V
V_O	Output voltage	E_e = 25 μW/cm²	1	2	3							V
		E_e = 45 μW/cm²				1	2	3				
		E_e = 285 μW/cm²							1	2	3	
	Temperature coefficient of output voltage (V_O)	E_e = 25 μW/cm², T_A = 0°C to 70°C		±1								mV/°C
		E_e = 45 μW/cm², T_A = 0°C to 70°C					±1					
		E_e = 285 μW/cm², T_A = 0°C to 70°C								±1		
N_e	Irradiance responsivity	See Note 4		80			45			7		mV/(μW/cm²)
I_{DD}	Supply current	E_e = 25 μW/cm²		900	1600							μA
		E_e = 45 μW/cm²					900	1600				
		E_e = 285 μW/cm²								900	1600	

NOTES: 3. The input irradiance E_e is supplied by a GaAlAs infrared-emitting diode with λ_p = 880 nm.
4. Irradiance responsivity is characterized over the range V_O = 0.05 to 3 V.

operating characteristics at T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS	TSL250			TSL251			TSL252			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Output pulse rise time	V_{DD} = 5 V, λ_p = 880 nm		360			90			7		µs
t_f	Output pulse fall time	V_{DD} = 5 V, λ_p = 880 nm		360			90			7		µs
V_n	Output noise voltage	V_{DD} = 5 V, f = 20 Hz		0.6			0.5			0.4		µV/√Hz

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORM

NOTES: A. The input irradiance is supplied by a pulsed GaAlAs infrared-emitting diode with the following characteristics: λ_p = 880 nm, t_r < 1 µs, t_f < 1 µs.
B. The output waveform is monitored on an oscilloscope with the following characteristics: t_r < 100 ns, Z_i ≥ 1 MHz, C_i ≤ 20 pF.

Figure 1. Switching Times

TYPICAL CHARACTERISTICS

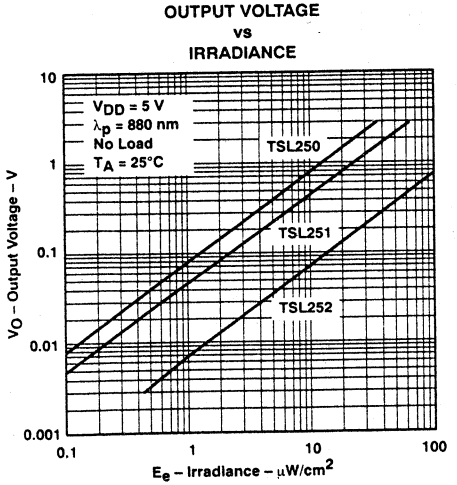


Figure 2

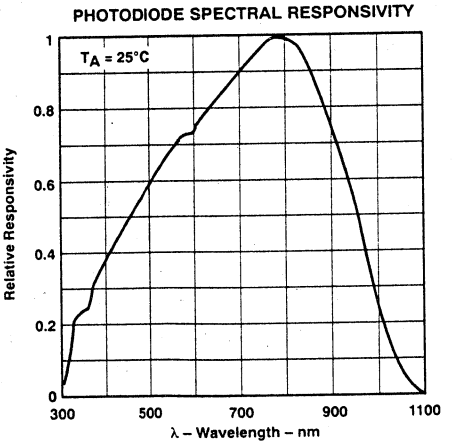


Figure 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

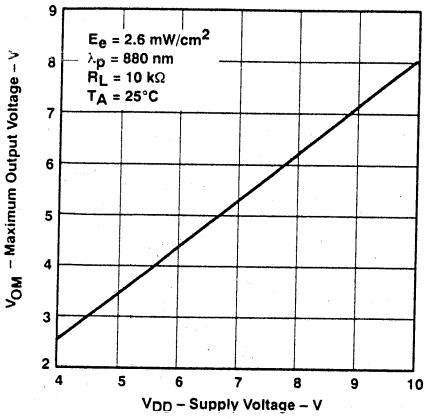


Figure 4

SUPPLY CURRENT
vs
OUTPUT VOLTAGE

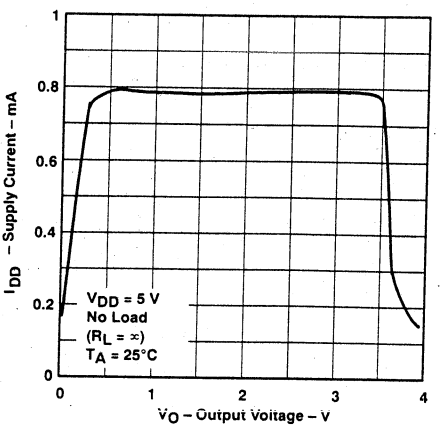


Figure 5

NORMALIZED OUTPUT VOLTAGE
vs
ANGULAR DISPLACEMENT

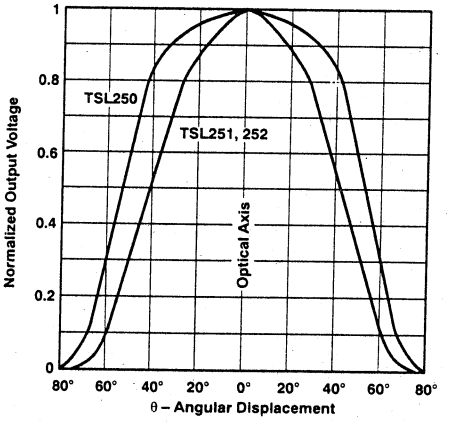


Figure 6

SOES008A – DECEMBER 1992 – REVISED FEBRUARY 1993

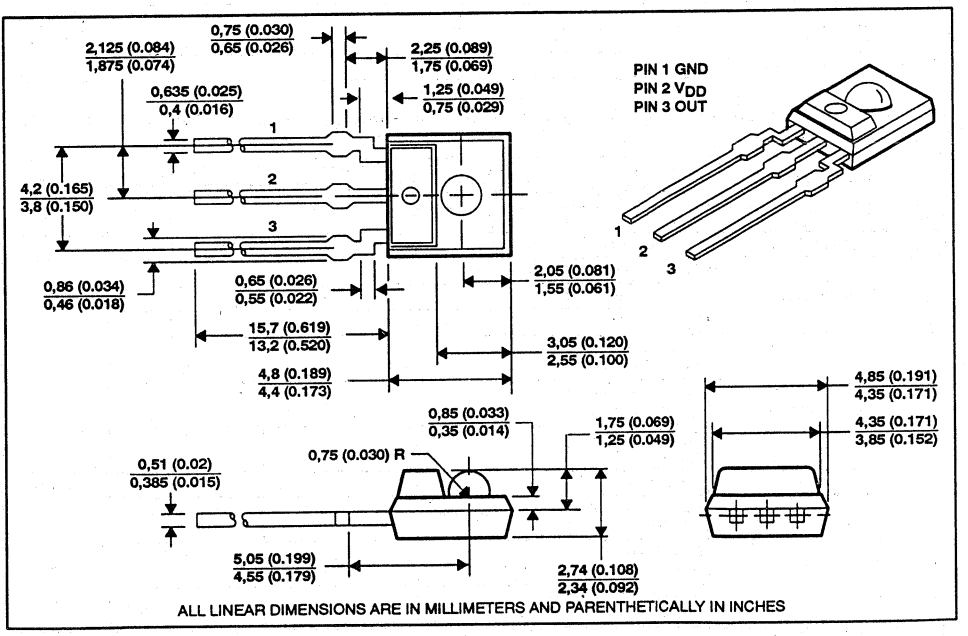
- **Integral Visible Light Cutoff Filter**
- **Monolithic Silicon IC Containing Photodiode, Operational Amplifier, and Feedback Components**
- **Converts Light Intensity to Output Voltage**
- **High Irradiance Responsivity Typically 42 mV/(μW/cm²) at λ_p = 940 nm (TSL260)**
- **Low Dark (Offset) Voltage . . . 10 mV Max at 25°C, V_{DD} = 5 V**
- **Single-Supply Operation**
- **Wide Supply Voltage Range . . . 3 V to 9 V**
- **Low Supply Current . . . 800 μA Typical at V_{DD} = 5 V**
- **Advanced LinCMOS™ Technology**

description

The TSL260, TSL261, and TSL262 are light-to-voltage optical sensors each combining a photodiode and a transimpedance amplifier (feedback resistor = 16 MΩ, 8 MΩ, and 2 MΩ, respectively) on a single monolithic integrated circuit. The output voltage is directly proportional to the infrared light intensity (irradiance) on the photodiode. The TSL260, TSL261, and TSL262 utilize Texas Instruments silicon-gate LinCMOS™ technology, which provides good amplifier offset-voltage stability and low power consumption.

mechanical data

The photodiode/amplifier chip is packaged in a black, infrared-transmissive plastic package. The integrated photodiode active area is typically 1,0 mm² (0.0016 in²), 0.5 mm² (0.00078 in²), and 0.26 mm² (0.0004 in²) for the TSL260, TSL261, and TSL262, respectively.



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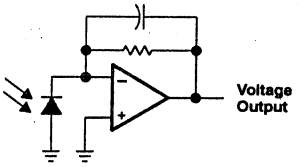
TEXAS INSTRUMENTS

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) ..... 10 V
Output current, I_O ..... ±10 mA
Duration of short-circuit current at (or below) 25°C (see Note 2) ..... 5 s
Operating free-air temperature range ..... −25°C to 85°C
Storage temperature range ..... −25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 240°C

NOTES: 1. All voltages are with respect to GND (pin 1).
2. Output may be shorted to either supply.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	9	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at V_{DD} = 5 V, T_A = 25°C, λp = 940 nm, R_L = 10 kΩ, (unless otherwise noted) (see Note 3)

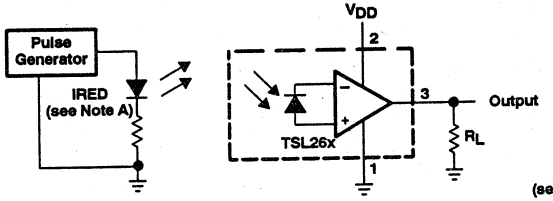
PARAMETER		TEST CONDITIONS	TSL260			TSL261			TSL262			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{DARK}	Dark voltage	E_e = 0		3	10		3	10		3	10	mV
V_{OM}	Maximum output	E_e = 2.6 mW/cm²	3.1	3.5		3.1	3.5		3.1	3.5		V
V_O	Output voltage	E_e = 48 µW/cm²	1	2	3							V
		E_e = 87 µW/cm²				1	2	3				
		E_e = 525 µW/cm²							1	2	3	
	Temperature coefficient of output voltage (V_O)	E_e = 48 µW/cm², T_A = 0°C to 70°C		±1								mV/°C
		E_e = 87 µW/cm², T_A = 0°C to 70°C					±1					
		E_e = 525 µW/cm², T_A = 0°C to 70°C								±1		
N_e	Irradiance responsivity	See Note 4		42			23			3.8		mV/(µW/cm²)
I_{DD}	Supply current	E_e = 48 µW/cm², No load		900	1600							µA
		E_e = 87 µW/cm², No load					900	1600				
		E_e = 525 µW/cm², No load								900	1600	

NOTES: 3. The input irradiance E_e is supplied by a GaAs infrared-emitting diode with λ_p = 940 nm.
4. Irradiance responsivity is characterized over the range V_O = 0.05 to 3 V.

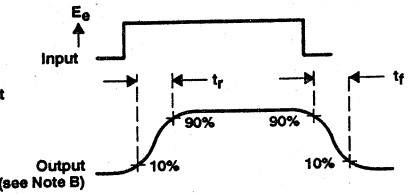
operating characteristics at T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS	TSL260			TSL261			TSL262			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Output pulse rise time	V_{DD} = 5 V, λ_p = 940 nm		360			90			7		µs
t_f	Output pulse fall time	V_{DD} = 5 V, λ_p = 940 nm		360			90			7		µs
V_n	Output noise voltage	V_{DD} = 5 V, f = 20 Hz		0.6			0.5			0.4		µV/√Hz

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: A. The input irradiance is supplied by a pulsed GaAs infrared-emitting diode with the following characteristics: λ_p = 940 nm, t_r < 1 µs, t_f < 1 µs.
B. The output waveform is monitored on an oscilloscope with the following characteristics: t_r < 100 ns, Z_i ≥ 1 MHz, C_i ≤ 20 pF.

Figure 1. Switching Times

TYPICAL CHARACTERISTICS

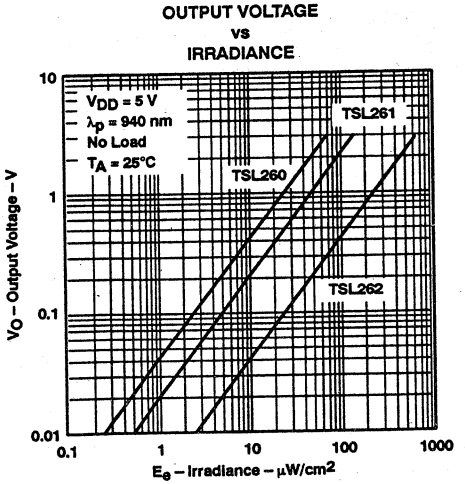


Figure 2

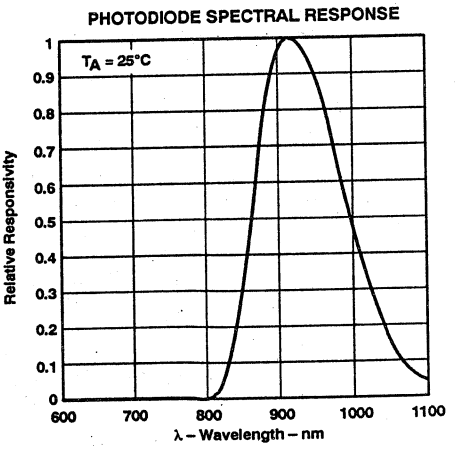


Figure 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

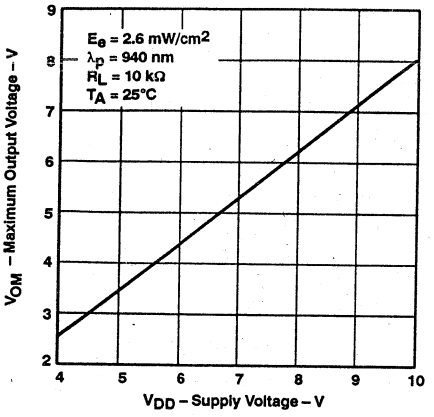


Figure 4

SUPPLY CURRENT
vs
OUTPUT VOLTAGE

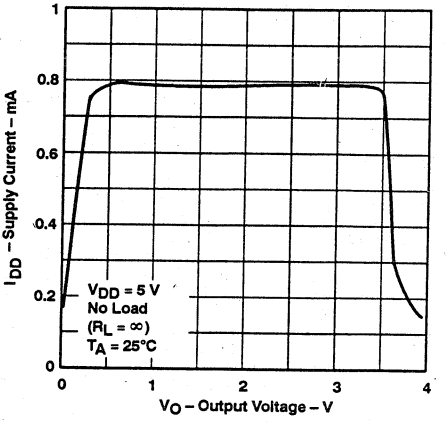


Figure 5

NORMALIZED OUTPUT VOLTAGE
vs
ANGULAR DISPLACEMENT

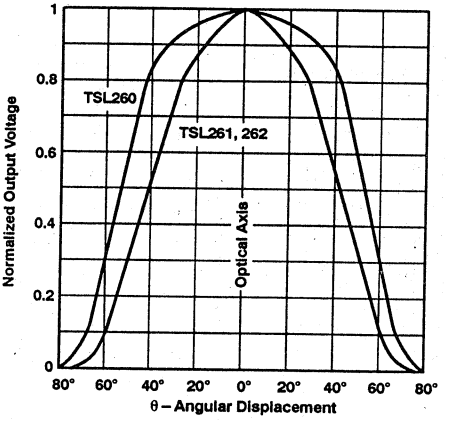
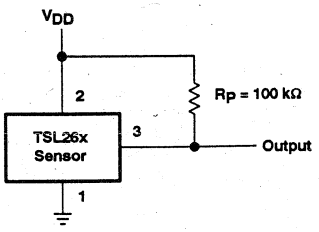


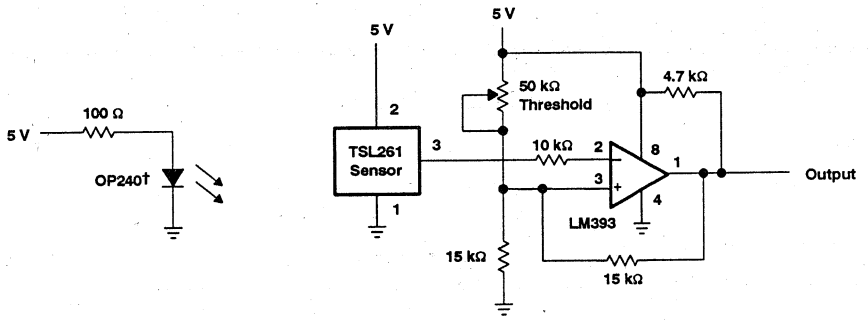
Figure 6

TYPICAL APPLICATIONS



NOTE: Pull-up resistor extends linear output range to near V_{DD} with minimal (several millivolts typical) effect on V_{DARK}; particularly useful at low V_{DD} (3 V to 5 V).

Figure 7. Pull Up for Increased V_{OM}

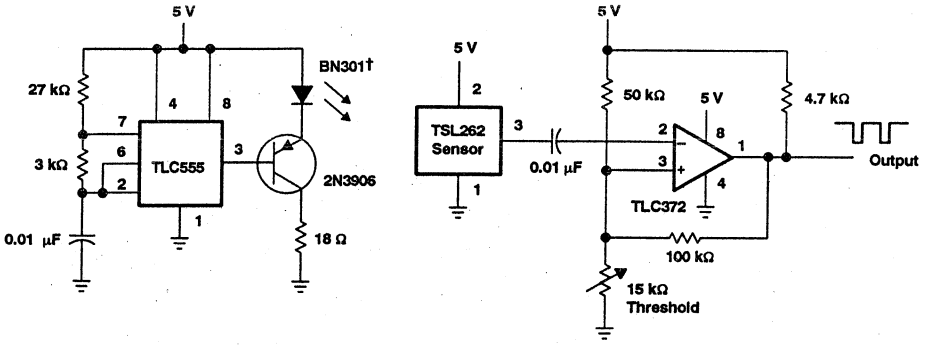


† OPTEK part number

NOTE: Output goes high when beam is interrupted; working distance is several inches or less. Intended for use as optical interrupter switch or reflective object sensor.

Figure 8. Short-Range Optical Switch With Hysteresis

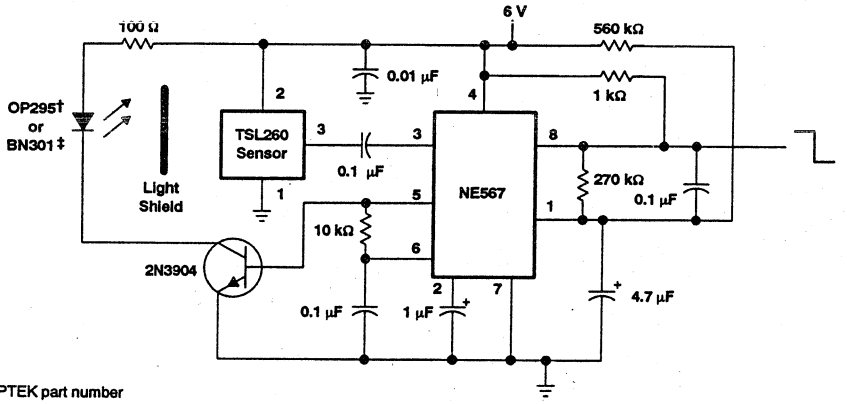
TYPICAL APPLICATIONS



† Stanley part number

NOTE: Output pulses low until beam is interrupted. Useful range is 1 ft to 20 ft; can be extended with lenses. This configuration is suited for object detection, safety guards, security systems, and automatic doors.

Figure 9. Pulsed Optical Beam Interrupter



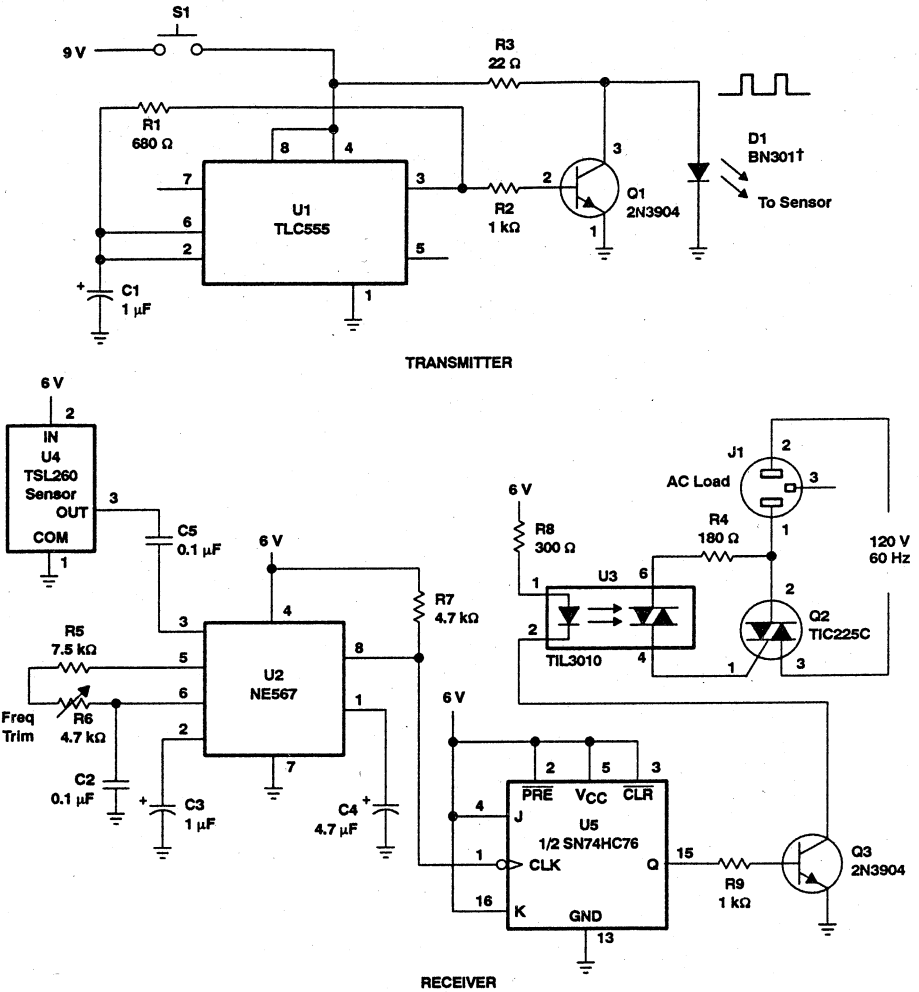
† OPTEK part number

‡ Stanley part number

NOTE: Output goes low when light pulses from emitter are reflected back to sensor. Range is 6 in to 18 in depending upon object reflectance. Useful for automatic doors, annunciators, object avoidance in robotics, automatic faucets, and security systems.

Figure 10. Proximity Detector

TYPICAL APPLICATIONS

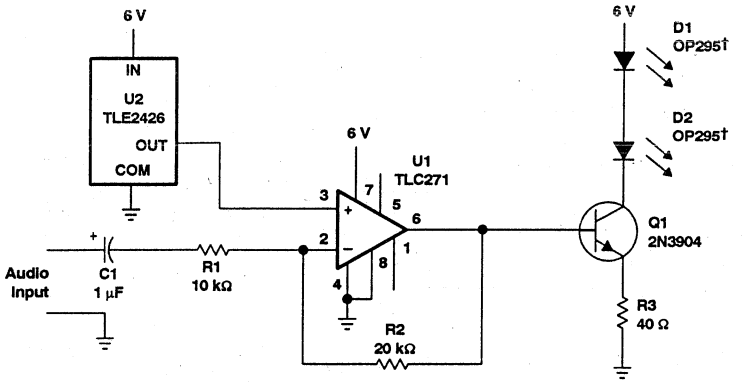


† OPTEK part number

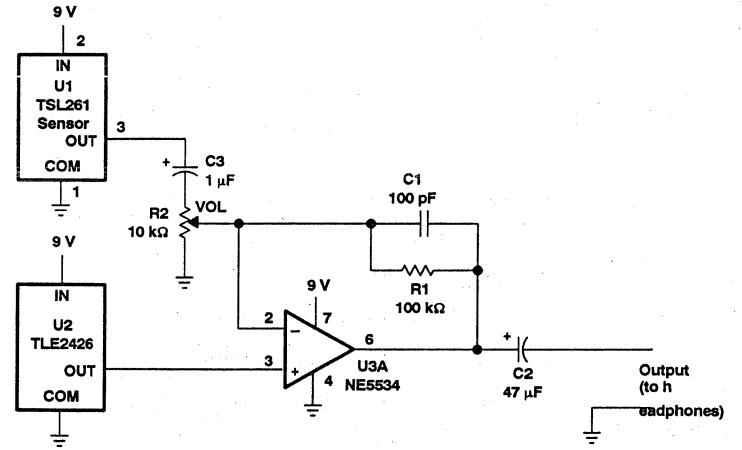
NOTE: Single-channel remote control can be used to switch logic or light dc loads by way of U5, pin 15, or ac loads by way of the optocoupler and triac as shown. Applications include ceiling fans, lamps, electric heaters, etc.

Figure 11. IR Remote Control

TYPICAL APPLICATIONS



TRANSMITTER



RECEIVER

† OPTEK part number

NOTE: Simple transmission of audio signal over short distances (<10 ft). Applications include wireless headphones, wireless telephone headset, and wireless headset intercom.

Figure 12. IR Voice-Band Audio Link

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